Simulation of a Transformer less Active Voltage Quality Regulator for Power Quality Improvement

N.Pruthvi Raj
M.Tech Student
Department of EEE,
Vignana Bharathi Institute of Technology,
Aushapur, Rangareddy,
Telangana State, India.

Ms.K.Mamatha
Assistant Professor
Department of EEE,
Vignana Bharathi Institute of Technology,
Aushapur, Rangareddy,
Telangana State, India.

Abstract:

The voltage sag compensator, based on a transformer-coupled series-connected voltage-source inverter, is among the most cost-effective solution against voltage sags. When voltage sags happen, the transformers, which are often installed in front of critical loads for electrical isolation, are exposed to the disfigured voltages and a dc offset will occur in its flux linkage. In this paper, a new topology of series-connected compensator is presented to mitigate long duration deep sags, and the compensation ability is highly improved with a unique shunt converter structure acting as a parasitic boost circuit that has been theoretically analyzed using open loop & closed loop control schemes. Additionally, the proposed active voltage quality regulator is a cost effective solution for long duration sags that are lower than 50% of the nominal voltage as it is transformer less compared with the traditional dynamic voltagerestorer.

Keywords: *Dynamic Voltage Restorer (DVR), Dynamic Sag Correction, Long Duration Deep Sag, Parasitic Boost Circuit, Series ConnectCompensator.*

I.INTRODUCTION

Electronic devices function properly as long as the voltage (or driving force) of the electricity feeding the device stays within a consistent range. There are several types of voltage fluctuations that can cause problems, including surges and spikes, sags, harmonic distortions, and momentary disruptions. Voltage sag is not a complete interruption of power; it is a temporary drop below 90 percent of the nominal voltage level. Most voltage sags do not go below 50 percent of the nominal voltage, and they normally last from 3 to 10 cycles—or 50 to 170 milliseconds. Voltage sags are probably the most significant power quality (PQ) problem facing industrial customers today, and they can be a significant problem for large commercial customers as well. There are two sources of voltage sags: external (on the utility's lines up to your facility) and internal (within your facility). Utilities continuously strive to provide the most reliable and consistent electric power possible. In the course of normal utility operations, however, many things can cause voltage sags. Storms are the most common cause of external sags and momentary interruptions in most areas of the U.S. A storm passing through an area can result in dozens of major and minor PQ variations, including sags. For example, consider how PQ would be affected by a lightning strike on or near a power line or by wind sending tree limbs into powerlines.

Other common causes of external voltage sags are ice storms, animals (particularly squirrels), and the

start- up of large loads at neighbouring facilities. Internal causesofvoltagesagscanincludestartingmajorloads

and grounding or wiring problems. If your facility is having frequent voltage sag problems, a good place to start is with your utility. Ask about the utility's statistics regarding performance in your area. You should also look into possible internal causes. But whether the causes are mainly external or internal, you should consider taking charge of the problem and working toward a cost effective solution for your facility. This obtained novel topology is called the transformer less active voltage quality regulator with the parasitic boost circuit (PB-AVQR), and it is capable of mitigating long duration deep voltage sags without increasing the cost, volume, and complexity compared with the traditional DySC topology. The dc-link voltage adaptive control method proposed is also applied in the PB AVQR to improve its operation efficiency. This paper starts with introducing the operating mode and working principles of the proposed configuration. Then, the parasitic boost circuit model is provided followed by the theoretical analysis to calculate its dc-linkvoltage.

II.TOPOLOGY ANDPRINCIPLE

As shown in Fig. 1, the PB-AVQR topology is mainly consists of five parts, including a static bypass switch (VT1, VT2), a half-bridge inverter (V1, V2), a shunt converter (VT3, VT4), a storage module(C1,C2), and a low-pass filter (Lf, Cf).The operating mode and applied control strategies are similar to what have been described. Under normal operating conditions, the static bypass switch is controlled to switch on and the normal grid voltage is delivered directly to the load side via this bypass switch. When an abnormal condition is detected,

the static bypass switch will be switched OFF and the inverter will be controlled to inject a desired missing voltage in series with the supply voltage to ensure the power supply of sensitive loads. There are totally two

different kinds of control strategies in the proposed PB- AVQR system. When the grid voltage is lower than the rated voltage, an in-phase control strategy will be adopted and a phase-shift control strategy will be applied when the supply voltage is higher than the nominalvoltage.

Working principle of the PB-AVQR is different compared with that of the DySC due to its unique shunt converter structure. When the proposed configuration is analyzed, both the operating states of the switches (V1, V2) and the trigger angles of the thyristors (VT1, VT2) should be taken into consideration. So, a simplified PB- AVQR (SPB-AVQR) circuit shown in Fig. 2 where two thyristors (VT3, VT4) in the proposed PB-AVQR are replaced by two diodes (D1, D2), is firstly introduced to better explain its working principles. The following analysis will be based on the SPB-AVQR which can be regarded as a special type ofPB-AVQR.
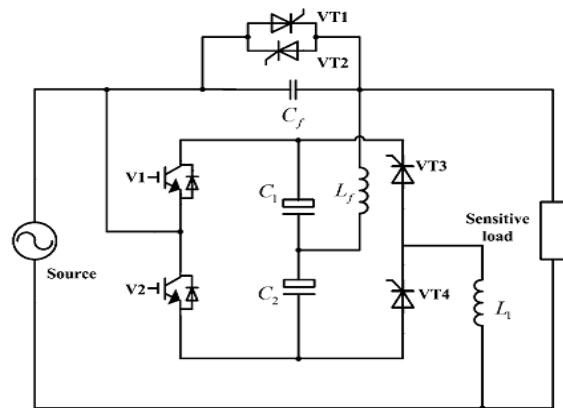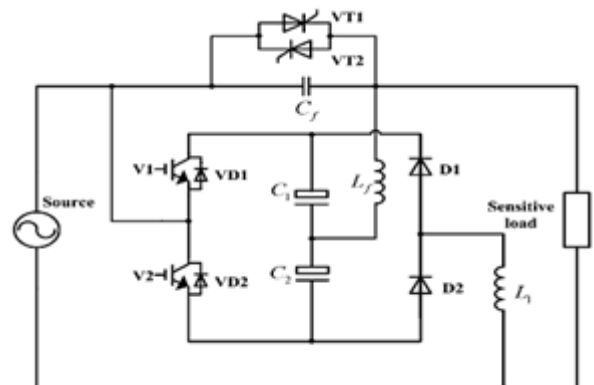

Fig.1.Proposed PB-AVQRtopology.

Fig.2.SPB-AVQRtopology.

The only difference between these two configurations is that the shunt converter of the PB-AVQR is controllable while the shunt converter of the SPB-AVQR is uncontrollable. That is to say, the dc-link voltage of the SPBAVQR represents the upper limit of thedc-link

voltage in the PB-AVQR structure. So, theoretical conclusions drawn with the SPB-AVQR are basically applicable to the PB-AVQR. As shown in Fig. 2, switches V1 and V2 are now also parts of the parallel circuit, which means that the dc-link voltage will be affected by the on/off status of the switches. So, the turn on and turn off conditions of the compensation process should be considered to understand the working principles about the parasitic boost circuit of the SPB-AVQR. Figs. 3 and 4 illustrate four different operating conditions of the SPB- AVQR within one switching cycle during the positive and negative half-cycle of the sinusoidal supply voltage separately. Both the compensation process and charging process can be explained based on these operating conditions.
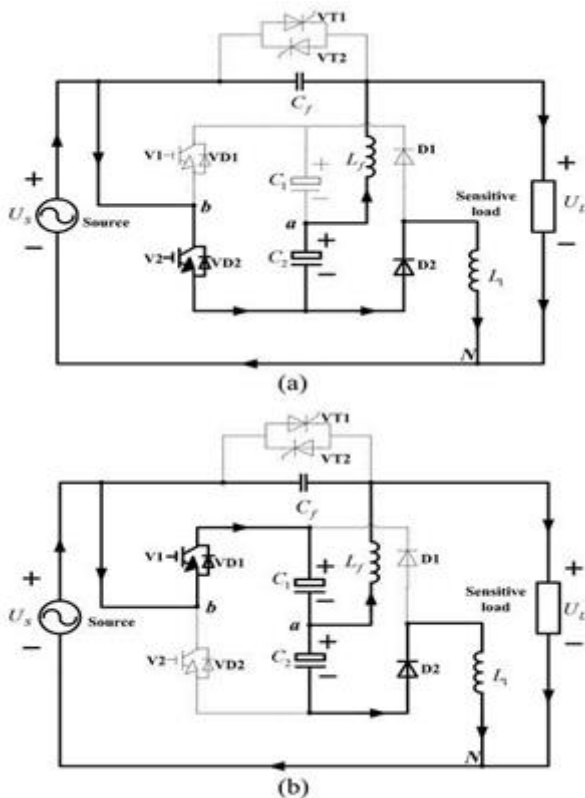

Fig.3. Operating conditions during positive half-cycle.

(a) V2 switched on.(b) V2 switchedoff.

In Figs. 3 and 4, the solid line means that there is current flowing through and arrows depict directions. Operating conditions during the positive half-cycle are illustrated in Fig. 3. When V2 is switched on, as shown in Fig. 3(a), the grid charges the inductor L1 via the diode D2 and the capacitorC2 discharges to maintain the load voltage. When V2 is switched off, as shown in Fig. 3. (b), the energy stored in the inductor during previous period is released to dc-link capacitors C1 and C2 through VD1 which is the anti parallel diode of V1. Operating conditions during the negative half-cycle are given inFig.4. When V1 is switched on, as shown in Fig.4 (a), the inductorL1is charged via the diode D1, and the load is compensated by the capacitor C1. When V1 is switched off, as shown in Fig. 4(b), the energy stored in L1 is released through VD2, which is the anti parallel diode of V2, to capacitorsC1 andC2. So, in each half-cycle of the grid, one capacitor of the dc-link discharges to provide the energy needed for the compensation, and this energy is actually obtained from the supply source via the charging process described earlier. Apparently, the charging circuit of the proposed configuration works exactly like a boost circuit and the dc-link voltage in this situation is controlled by the duty ratio of the twoswitches.
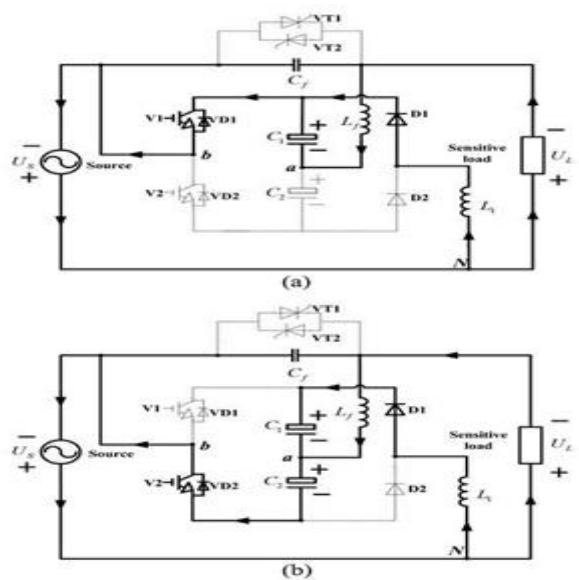

Fig. 4.Operating conditions during negativehalf-cycle.

(a) V1 switched on. (b) V1 switchedoff.

So, the compensation ability of the SPB-AVQR is theoretically unlimited as long as the grid is strong enough to provide the needed power. However, as the boost circuit is parasitic on the series inverter, and the two switches are actually controlled according to the missing voltage, there still exist some restrictions. The relationships between the dc-link voltage and other system parameters will be discussed in the next section.

In Figs. 3 and 4, two endpoints of the inverter are marked as a and b. Parts of the waveforms obtained at the inverter side and load side under four operating conditions are schematically shown in Fig.5, where UaN represents the voltage between a and N. As shown in Fig.6, when V1/V2 is switched on/off, the dc-link voltage will be added/subtracted to the supply voltage to get a switching pulse voltage UaN and the switching harmonics of UaN will be filtered by Lf and Cf to get a smooth load voltage. So, the load voltage will be maintained at its rated value if the inverter is properly controlled according to the required missing voltage duringsags.

III.MODELINGANDTHEORETICALANALYSIS

DC-link voltage is a key parameter to evaluate the compensation ability about a series compensation device since it decides the maximum value of the injected compensation voltage.

In this section, in order to evaluate the compensation ability of the proposed topology and verify its feasibility in mitigating long duration deep sags, relationships between the dc-link voltage and other system parameters will be derived based on the circuit model of the aforementioned operating conditions. As can be seen from Figs. 3and 4, working principles during the positive and negative half-cycle of the supply voltage are the same, so the following analysis will be focused on the situation in the positivehalf-cycle.
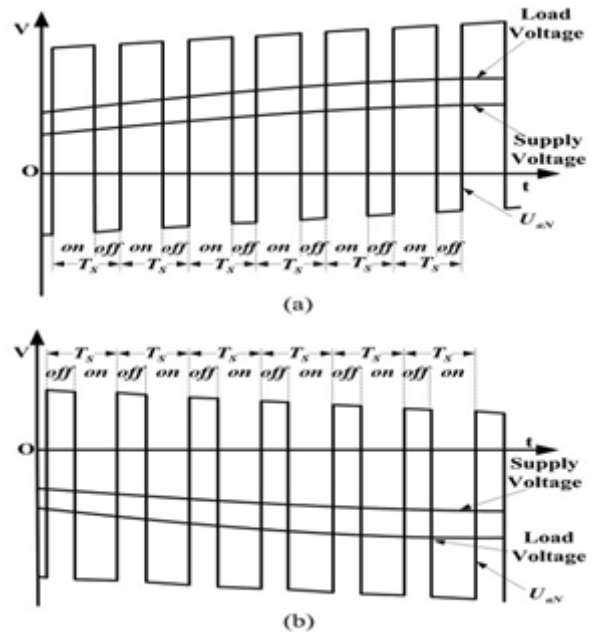

Fig. 5 Waveforms of supply voltage, load voltage, and UaN. (a) V2 on/off. (b) V1on/off.

The control strategy applied for voltage sags is in-phase compensation, so the energy needed to maintain the load voltage in one half-cycle can be expressed asfollows:

$$E_0 = \frac{T_0 \Delta V}{2 V_{\text{ref}}} P_0 \tag{1}$$

Where T0 is the grid voltage period time, Vref is the rated rms value of the load voltage, P0 is the rated load power, and ΔV is the rms value of the missing voltage.

In steady- state compensation, the energy needed for the compensation should completely be provided by the residential grid which is also the charging energy through the parasitic boost circuit in this case. So the charging energy provided during T0/2 referred to as E1 equals to E0. E0 can be easily obtained according to (1), but the calculation ofE1 involves with the operating conditions shown in Fig. 3. The simplified circuit model of Fig. 3is illustrated in Fig. 6, where compensation loop including the filter and the load is ignored and only the charging circuit isconsidered.
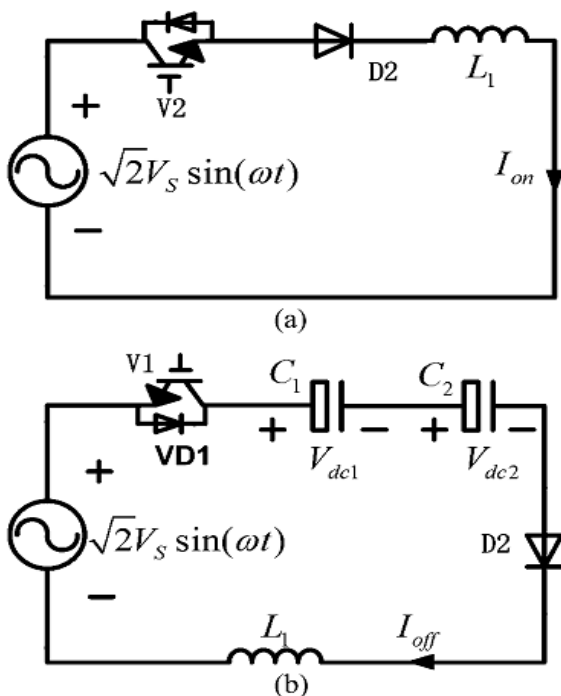
Fig.6. Simplified circuit model. (a) V2 turned on. (b) V2 turnedoff.

In Fig. 6, VS is the rms value of the supply voltage. Two state equations can be obtained based on Fig. 6 and written asfollows:

$$\begin{cases} L_1 \dfrac{dI_{\text{on}}}{dt} = \sqrt{2}V_S \sin(\omega t) \\ L_1 \dfrac{dI_{\text{off}}}{dt} = \sqrt{2}V_S \sin(\omega t) - V_{dc1} - V_{dc2} \end{cases} \tag{2}$$

According to the analysis will be significantly simplified if some realistic approximations are carried out. Then (2) can be discredited into (3) based on two following assumptions: C1 and C2 are well designed so thatVdc1 and Vdc2 can be regarded equal without considering their ripple voltages; the switching frequency is much higher than the line frequency that the supply voltage in the nth switching cycle can be treated as a constant value where tonnand toffnare, respectively, the turn-on and turn-off time of V2 in the nth switching cycle, Ts is the switching period, Vdc is the steady-state dc-link voltage, and ΔIonnor ΔIoffnrepresents the variation amount in charging current during tonnortoffn.

$$\begin{cases} L_1 \Delta I_{\text{onn}} = \sqrt{2}V_S \sin(\omega n T_s) t_{\text{onn}} \\ L_1 \Delta I_{\text{offn}} = [\sqrt{2}V_S \sin(\omega n T_s) - 2V_{dc}] t_{\text{offn}} \end{cases} \tag{3}$$

As the analysis is within the positive half-cycle of the grid, there exists a constraint: n≤T0/2Ts. Apparently, tonnand toffnhere are actually the inverter's duty cycle and they can be expressed as (4) when two-level symmetric regular-sampled PWM method isadopted

$$\begin{cases} t_{\text{onn}} = \dfrac{T_s}{2}\left[1 + \dfrac{\sqrt{2}\Delta V \sin(\omega n T_s)}{V_{dc}}\right] \\ t_{\text{offn}} = \dfrac{T_s}{2}\left[1 - \dfrac{\sqrt{2}\Delta V \sin(\omega n T_s)}{V_{dc}}\right] \end{cases} \tag{4}$$

The recursion formula of the charging current at the end of the nth switching cycle can be obtained by combining (3) and(4)

$$I_{\text{offn}} = I_{\text{off}(n-1)} + \dfrac{T_s}{L_1}[\sqrt{2}V_{\text{ref}} \sin(\omega n T_s) - V_{dc}] \tag{5}$$

Where Ioffnrepresents the charging current instantaneous value at the end of the nthswitching cycle and ΔIonncan be derived at the sametime

$$\Delta I_{\text{onn}} = \dfrac{\sqrt{2}T_s V_S \sin(\omega n T_s)}{2L_1}\left[1 + \dfrac{\sqrt{2}\Delta V \sin(\omega n T_s)}{V_{dc}}\right] \tag{6}$$

The energy stored in an inductor is related to the current that flows through it, so the charging energy provided by the grid via the parasitic boost circuit in the nthswitching cycle can be expressed and then rearranged asfollows:

$$E_{\text{inn}} = \dfrac{1}{2}L_1 \Delta I_{\text{onn}}^2 + L_1 I_{\text{off}(n-1)} \Delta I_{\text{onn}} \tag{7}$$

Ioff(n−1) in (7) can be superimposed according to the recursion formula shown in (5). Before the expression is given, there are some features about the charging current should be clarified: 1) the value of the charging current cannot be lower than zero as the current flowing through a diode is unidirectional; 2) the value of the charging current can either be zero or nonzero and its value always decreases after increasing in one half-cycle of the sinusoidal grid voltage. Then, the nonzero terms of the charging current can be derived asfollows:

$$I_{\text{off}(n-1)} = \sum_{k=n_0}^{n-1} \frac{T_s}{L_1} \left[\sqrt{2} V_{\text{ref}} \sin(\omega k T_s) - V_{\text{dc}} \right]$$

$$\text{(8)}$$

Where n0 is the initial superposition instant and Ioffnis always equal to zero when n is smaller than n0. So, n0 can be calculated according to (5) and expressed asfollows:

$$n_0 = \text{ceil}\left(\frac{T_0 \arcsin \frac{V_{\text{dc}}}{V_{\text{ref}}}}{2\pi T_s} \right)$$

$$\text{(9)}$$

Where ceil(•) represents the rounded up function and the arcsine function here ranges from 0 to π/2. Furthermore, when the charging current calculated by (8) decreases to the value no more than zero, n will reach its upper limit denoted byne. Substituting (6), (8), and (9) into (7), the energy provided by the supply in the nth switching cycle can be written asfollows:

$$E_{\text{in}n} = \frac{T_s^2 V_S^2 A^2}{4L_1}(1 + \sqrt{2}BA)^2 + \frac{\sqrt{2}T_s^2 V_S A}{2L_1 V_{\text{dc}}}$$

$$\times (V_{\text{dc}} + \sqrt{2}\Delta V A) \sum_{k=n_0}^{n-1} (\sqrt{2}V_{\text{ref}}C - V_{\text{dc}})$$

$$\text{(10)}$$

Where

$$A = \sin \omega n T_s$$
$$B = \frac{\Delta V}{V_{\text{dc}}}$$
$$C = \sin \omega k T_s$$

E1 now can be obtained if (10) is added with n ranging from 1to T0/2Ts. So, the overall energy balance equation can be written asfollows:

$$E_1 = \frac{T_s^2 V_S^2}{4L_1} \left(\sum_{n=1}^{\frac{T_0}{2T_s}} A^2 + 2\sqrt{2}B \sum_{n=1}^{\frac{T_0}{2T_s}} A^3 + 2B^2 \sum_{n=1}^{\frac{T_0}{2T_s}} A^4 \right)$$

$$+ \frac{T_s^2 \sqrt{2} V_S}{2L_1} \sum_{n=n_0}^{n_e} \left[(A + \sqrt{2}BA^2) \sum_{k=n_0}^{n-1} (\sqrt{2}V_{\text{ref}}C - V_{\text{dc}}) \right]$$

$$= \frac{T_0 \Delta V}{2V_{\text{ref}}} P_0 = E_0$$

$$\text{(11)}$$

The charging current peak value Imax is considered to arise at the switching cycle after the value of (8) reaches its upper limit. So Imax is expressed asfollows

$$I_{\max} = \frac{\sqrt{2}T_s V_S \sin(\omega n_{\max} T_s)}{2L_1}[1 + \sqrt{2}B\sin(\omega n_{\max} T_s)]$$

$$+ \sum_{n=n_0}^{n_{\max}} \frac{T_s}{L_1}(\sqrt{2}V_{\text{ref}}C - V_{\text{dc}})$$

$$\text{(12)}$$

Where nmax is the switching cycle when Ioffnreaches its maximum value and nmax can be written asfollows:

$$n_{\max} = \text{ceil}\left[\frac{T_0(\pi - \arcsin \frac{V_{\text{dc}}}{V_{\text{ref}}})}{2\pi T_s} \right]$$
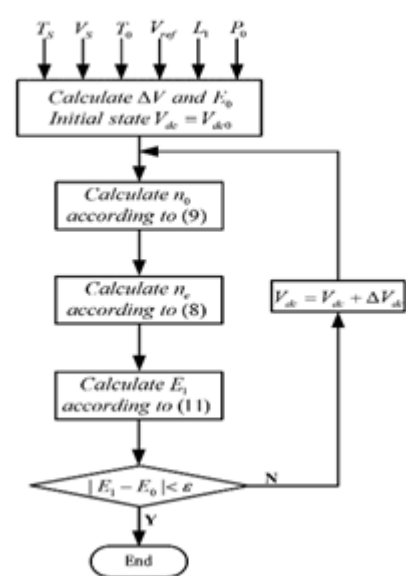
$$\text{(1}$$

Fig. 7. Flow chart for calculatingVdc.

So far, the main features of the SPB-AVQR topology can be described by (11) and (12). As shown in (11), the dc-link voltage is not only related to the supply voltage, but also associated with the charging inductance, load active power, and switching frequency. However, the dc- link voltage cannot be obtained directly from (11) as n0

and ne cannot be computed with unknown dc-link voltage. So, an iterative algorithm is applied to estimate the dc- link voltage, where Ts, VS, T0, Vref, L1, and P0 are all treated as constants. A flow chart of the adopted calculating method is illustrated in Fig. 7, where Vdc0 is the initial value for Vdc and ΔVdc is the iterative step. The algorithm is terminated if the error between E0 and E1 is smaller than the error

tolerance ε. Moreover, the charging current can be calculated by (12) and (13) as long as Vdcisobtained.

It presents that the steady-state charging current peak value increases with the decreasing of the supply voltage and it can be suppressed by increasing the charging inductance. Although conclusions drawn from the theoretical analysis for the SPB-AVQR can also be applied to the proposed PB-AVQR topology, there still exist some differences in their dc-link voltages. When the proposed PB-AVQR is discussed, the trigger pulse angle α for VT3 and VT4 should also be taken into consideration. In the PB-AVQR circuit, the charging process begins after the VT3 or VT4 is triggered, so the initial superposition instant n0 in (11) is now determined by α denoted byn1 and the energy balance equation is written asfollows

$$\frac{T_s^2 V_S^2}{4 L_1}\left(\sum_{n=n_1}^{n_e} A^2 + 2\sqrt{2}B\sum_{n=n_1}^{n_e} A^3 + 2B^2 \sum_{n=n_1}^{n_e} A^4\right)$$
$$+ \frac{T_s^2 \sqrt{2} V_S}{2 L_1}\sum_{n=n_1}^{n_e}\left[(A+\sqrt{2}BA^2)\sum_{k=n_1}^{n-1}(\sqrt{2}V_{\mathrm{ref}}C - V_{\mathrm{dc}})\right]$$
$$= \frac{T_0 \Delta V}{2 V_{\mathrm{ref}}} P_0 \qquad (14)$$

Here, ne is still determined by (8) as aforementioned and n1 can be derived asfollows:

$$n_1 = \mathrm{ceil}\left(\frac{\alpha T_0}{2\pi T_s}\right) \qquad (15)$$

Furthermore, the thyristors are triggered only once in each half-cycle and the current through them should be higher than the holding current to maintain the triggered state. So, α is required to meet the constraint expressed as follows:

$$\sqrt{2}V_{\mathrm{ref}}\sin\alpha > V_{\mathrm{dc}} \qquad (16)$$

The charging current peak value of the PB-AVQR can still be described by (12) as long asn0is substituted withn1. As can be seen from (14) and (15), the trigger pulse of the PB-AVQR will certainly affect its dc-link voltage and chargingcurrent.

IV. MATLAB/SIMULINKRESULTS
Here simulation is carried out in several load conditions, in that 1) Implementation of DySCtopology

2)Proposed Active Voltage Quality Regulator Topology,
3) Proposed Active Voltage Quality Regulator Topology with Non-Linear Load, 4) Proposed Active Voltage Quality Regulator Topology with Closed LoopController.

Case 1: Implementation of DySCTopology.

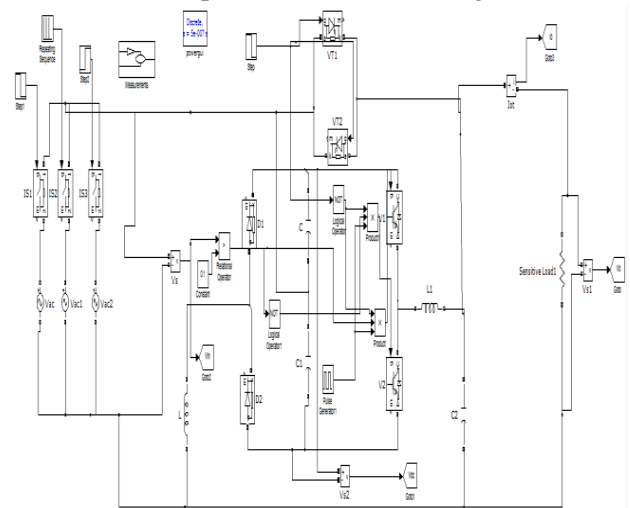Matlab/Simulink Model of DySC Topology by using Matlab/Simulink platform as shown inFig.8.

Fig.8. Matlab/Simulink Model of DySC Topology by using Matlab/Simulinkplatform.

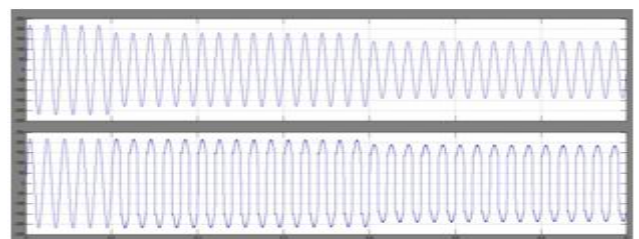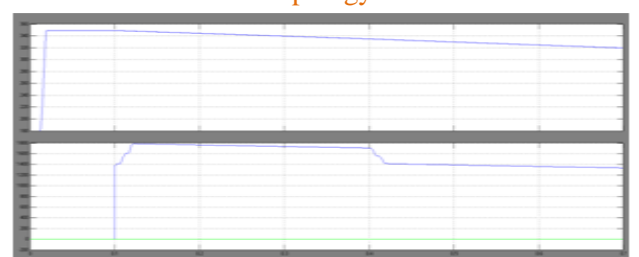Fig.9. Supply Voltage & Load Voltage of DySC Topology.

Fig.10. DC Link Voltage & Active, ReactivePower.

Fig. 9 shows the simulation results of the DySC topology voltage drops to 180 V at 0.1 s and then falls to 100 V at 0.4 s, when the supply voltage is 180V, the DySC can effectively compensate for the voltage sag; however, when the supply voltage drops to 100 V, the load voltage becomes not sinusoidal as the maximum injected compensation voltage is limited by the low steady-state dc-link voltage. Fig. 10 also indicates that the DySC can only mitigate deep sags for a few line cycles depending on the energy stored in dc-link capacitors as its steady-state dc-link voltage is always lower than the peak value of the supplyvoltage.

Case 2: Proposed Active Voltage Quality Regulator Topology.

Matlab/Simulink model of Proposed Active Voltage Quality Regulator Topology using Matlab/Simulink platform as shown inFig.12.
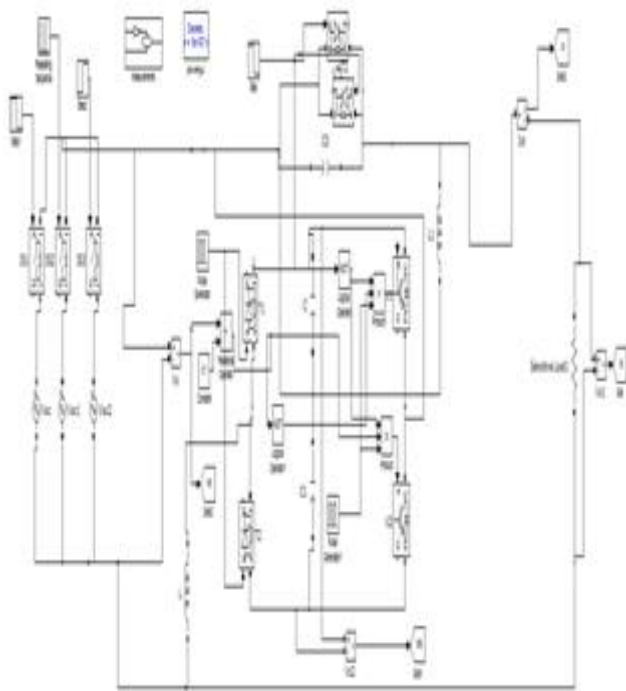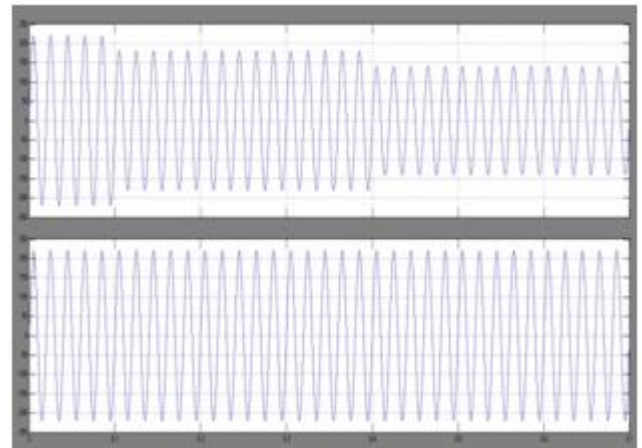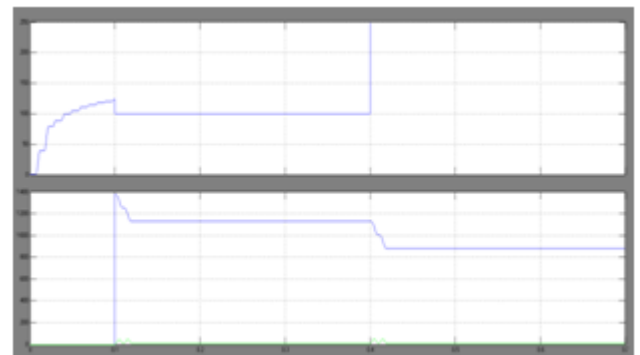

Fig.12 Matlab/Simulink model of Proposed Active Voltage Quality Regulator Topology using Matlab/Simulinkplatform.
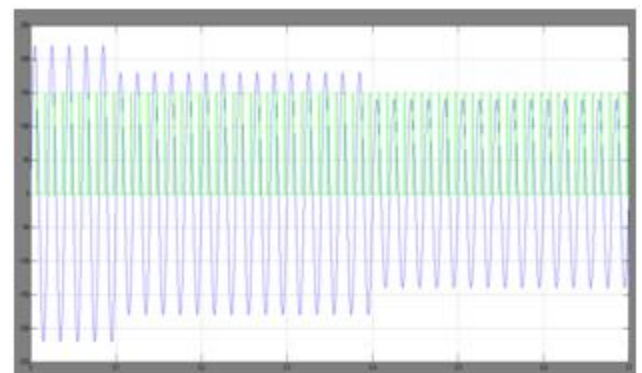
Proposed Active Voltage Quality Regulator Topology wave forms is shown inFig.13.

(a)Supply Voltage & LoadVoltage

(b)DC Link Voltage & Active, ReactivePower

(c)Input Voltage & Switching States Fig.13 (a) Supply Voltage & Load Voltage, (b) DC Link Voltage & P-Q Power, (c) Input Voltage & Switching States of Proposed Active Voltage Quality RegulatorTopology.

Case 3: Proposed Active Voltage Quality Regulator Topology with Non-LinearLoad.

Matlab/Simulink model of Proposed Active Voltage Quality Regulator Topology with Non-Linear Load using Matlab/Simulink platform as shown inFig.14.
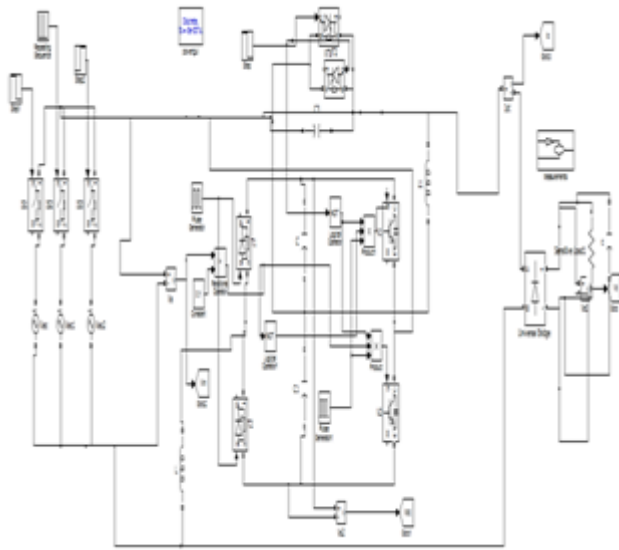

Fig.14. Matlab/Simulink model of Proposed Active Voltage Quality Regulator Topology with Non-Linear Load using Matlab/Simulinkplatform.
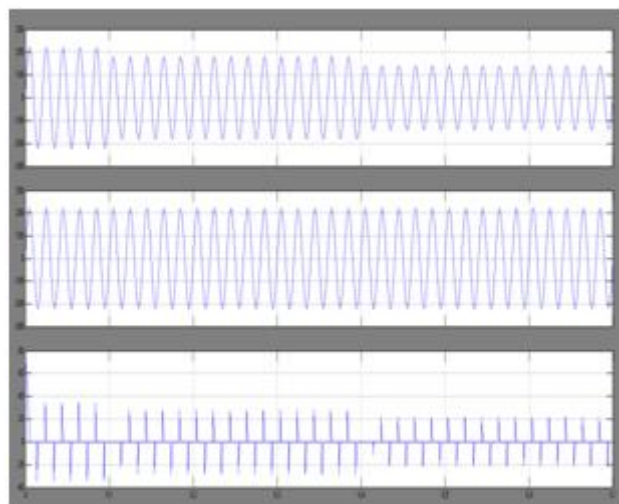

Fig.15. Input Voltage, Output Voltage, Input Current of Proposed Active Voltage Quality Regulator Topology with Non-Linear Load, due to non-linear diode bridge rectifier load attains the non-linear characteristics of voltage &current.

Proposed Active Voltage Quality Regulator Topology with Non-Linear Load as shown inFig.15.

Case 4: Proposed Active Voltage Quality Regulator Topology with Closed LoopController.

Matlab/Simulink Model of Proposed Active Voltage Quality Regulator Topology with Closed Loop Controller using Matlab/Simulink platform as shown inFig.16.
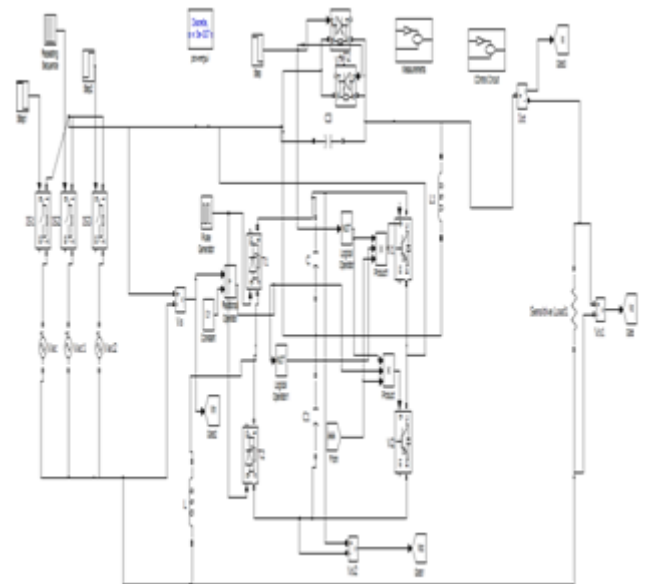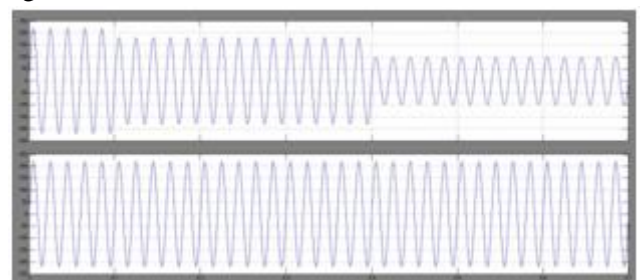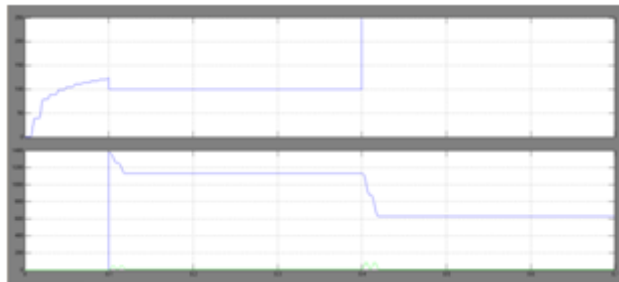

Fig.16. Matlab/Simulink Model of Proposed Active Voltage Quality Regulator Topology with Closed Loop Controller using Matlab/Simulinkplatform.
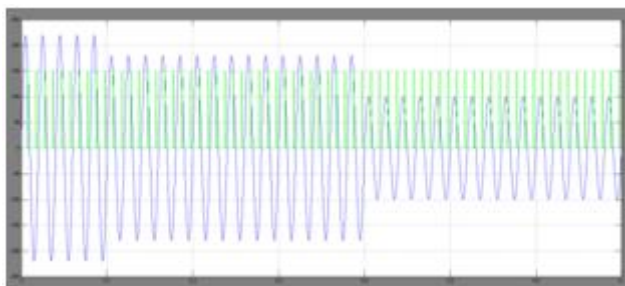
Proposed Active Voltage Quality Regulator Topology with Closed Loop Controller wave forms as shown in Fig.17.

(a)Supply Voltage & LoadVoltage

(b)DC Link Voltage & Active, ReactivePower

(c)Input Voltage & Switching States Fig.17.(a) Supply Voltage & Load Voltage, (b) DC Link Voltage & P-Q Power, (c) Input Voltage & Switching States of Proposed Active Voltage Quality Regulator Topology under Closed-LoopCondition.

V. CONCLUSION

This paper has presented a novel transformer less active voltage quality regulator with parasitic boost circuit operates under closed loop condition to mitigate long duration deep voltage sags with good stability factor and low error components.

The proposed PB-AVQR topology is derived from the DySC circuit and the compensation performance is highly improved without increasing the cost, weight, volume, and complexity. It is a relatively cost-effective solution for deep sags with long duration time compared with the traditional DVR topology with load-side-connected shunt converter as a series transformer is no longer needed. The working principle and circuit equations are given through theoretical analysis. The operating efficiency of the proposed PB- AVQR system also remains at a relatively high level as the dc-link voltage adaptive control method isadopted.

VI. REFERENCES

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Author Details

N. Pruthvi Raj M.Tech(Power Electronics And Electrical Drives) PursuingIinVIGNANA BHARATHI INSTITUTE OF TECHNOLOGY, Aushapuri, Ranga Reddy Dist , T.S, India.

Ms. K. Mamatha Assistant Professor Department Of Electrical & Electronic Engineering, VIGNANA BHARATHI INSTITUTE OF TECHNOLOGY, Aushapuri, Ranga Reddy DistT.S, India.She received the B.Tech Degree from Adishankara Institute of technology at GUDURU and M.Tech from JNTU Hyerabad with PE&ED. Her areas of interesting on, Power Systems Power Electronics and Electrical Drives