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A Relative Analysis of High Performance Stacking Power Gating Schemes Which Decreases Ground Bounce Noise

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Abstract:

The history of the understanding of semiconductors begins with experiments on the electrical properties of materials. The properties of negative temperature coefficient of resistance, rectification, and light-sensitivity were observed starting in the early 19th century. Power gating is a technique used in integrated circuit design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use. In addition to reducing stand-by or leakage power, power gating has the benefit of enabling Iddq testing. As technology scales into the nanometer regime ground bounce noise and noise immunity are becoming important metric of comparable importance to leakage current, active power, delay and area for the analysis and design of complex arithmetic logic circuits. In CMOS integrated circuit design there is a trade-off between static power consumption and technology scaling. Leakage power accounts for an increasingly larger portion of total power consumption in deep submicron technologies. Recently, the power density has increased due to combination of higher clock speeds, greater functional integration, and smaller process geometries. As a result static power consumption is becoming more dominant. This is a challenge for the circuit designers. However, the designers do have a few methods which they can use to reduce this static power consumption. But all of these methods have some drawbacks. In order to achieve lower static power consumption, one has to sacrifice design area and circuit performance. In this paper we perform A relative analysis of high performance stacking power gating schemes which decreases ground bounce noise.

Keywords:

Semiconductors, Power gating schemes, CMOS, Power density, Performance, Noise.

Introduction:

Semiconductors are crystalline or amorphous solids with distinct electrical characteristics. They are of high resistance - higher than typical resistance materials, but still of much lower resistance than insulators. Their resistance decreases as their temperature increases, which is behavior opposite to that of a metal. Finally, their conducting properties may be altered in useful ways by the deliberate introduction of impurities into the crystal structure, which lowers its resistance but also permits the creation of semiconductor junctions between differently-doped regions of the crystal. The behavior of charge carriers at these junctions is the basis of diodes, transistors and all modern electronics.Semiconductor devices can display a range of useful properties such as passing current more easily in one direction than the other, showing variable resistance, and sensitivity to light or heat. Because the electrical properties of a semiconductor material can be modified by controlled addition of impurities, or by the application of electrical fields or light, devices made from semiconductors can be used for amplification, switching, and energy conversion.The modern understanding of the properties of a semiconductor relies on quantum physics to explain the movement of electrons and holes in a crystal lattice. Doping greatly increases the number of charge carriers within the crystal. When a doped semiconductor contains mostly free holes it is called “p-type”, and when it contains mostly free electrons it is known as “n-type”. The semiconductor materials used in electronic devices are doped under precise conditions to control the concentration and regions of p- and n-type dopants. A single semiconductor crystal can have many p- and n-type regions; the p–n junctions between these regions are responsible for the useful electronic behavior.

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Power Gating:

Power gating affects design architecture more than clock gating. It increases time delays, as power gated modes have to be safely entered and exited. Architectural trade-offs exist between designing for the amount of leakage power saving in low power modes and the energy dissipation to enter and exit the low power modes. Shutting down the blocks can be accomplished either by software or hardware. Driver software can schedule the power down operations. Hardware timers can be utilized. A dedicated power management controller is another option.

An externally switched power supply is a very basic form of power gating to achieve long term leakage power reduction. To shut off the block for small intervals of time, internal power gating is more suitable. CMOS switches that provide power to the circuitry are controlled by power gating controllers. Outputs of the power gated block discharge slowly. Hence output voltage levels spend more time in threshold voltage level.

This can lead to larger short circuit current. Power gating uses low-leakage PMOS transistors as header switches to shut off power supplies to parts of a design in standby or sleep mode. NMOS footer switches can also be used as sleep transistors. Inserting the sleep transistors splits the chip's power network into a permanent power network connected to the power supply and a virtual power network that drives the cells and can be turned off.

Typically, high-Vt sleep transistors are used for power gating, in a technique also known as multi-threshold CMOS (MTCMOS). The sleep transistor sizing is an important design parameter.The quality of this complex power network is critical to the success of a power-gating design. Two of the most critical parameters are the IR-drop and the penalties in silicon area and routing resources. Power gating can be implemented using cell- or cluster-based (or fine grain) approaches or a distributed coarse-grained approach.

Power-gating parameters:

Power gating implementation has additional considerations for timing closure implementation. The following parameters need to be considered and their values carefully chosen for a successful implementation of this methodology.

Power gate size: The power gate size must be selected to handle the amount of switching current at any given time. The gate must be bigger such that there is no measurable voltage (IR) drop due to the gate. As a rule of thumb, the gate size is selected to be around 3 times the switching capacitance. Designers can also choose between header (P-MOS) or footer (N-MOS) gate. Usually footer gates tend to be smaller in area for the same switching current. Dynamic power analysis tools can accurately measure the switching current and also predict the size for the power gate.

Gate control slew rate: In power gating, this is an important parameter that determines the power gating efficiency. When the slew rate is large, it takes more time to switch off and switch-on the circuit and hence can affect the power gating efficiency. Slew rate is controlled through buffering the gate control signal.

Simultaneous switching capacitance: This important constraint refers to the amount of circuit that can be switched simultaneously without affecting the power network integrity. If a large amount of the circuit is switched simultaneously, the resulting "rush current" can compromise the power network integrity. The circuit needs to be switched in stages in order to prevent this.

Power gate leakage: Since power gates are made of active transistors, leakage reduction is an important consideration to maximize power savings.

Power gating methods:
Fine-grain power gating:

Adding a sleep transistor to every cell that is to be turned off imposes a large area penalty, and individually gating the power of every cluster of cells creates timing issues introduced by inter-cluster voltage variation that are difficult to resolve. Fine-grain power gating encapsulates the switching transistor as a part of the standard cell logic. Switching transistors are designed by either the library IP vendor or standard cell designer. Usually these cell designs conform to the normal standard cell rules and can easily be handled by EDA tools for implementation.The size of the gate control is designed considering the worst-case scenario that will require the circuit to switch during every clock cycle, resulting in a huge area impact. Some of the recent designs implement the fine-grain power gating selectively, but only for the low Vt cells.

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If the technology allows multiple Vt libraries, the use of low Vt devices is minimum in the design (20%), so that the area impact can be reduced. When using power gates on the low Vt cells the output must be isolated if the next stage is a high Vt cell. Otherwise it can cause the neighboring high Vt cell to have leakage when output goes to an unknown state due to power gating.

Coarse-grain power gating:

The coarse-grained approach implements the grid style sleep transistors which drives cells locally through shared virtual power networks. This approach is less sensitive to PVT variation, introduces less IR-drop variation, and imposes a smaller area overhead than the cell- or cluster-based implementations. In coarse-grain power gating, the power-gating transistor is a part of the power distribution network rather than the standard cell.Gate sizing depends on the overall switching current of the module at any given time.

Since only a fraction of circuits switch at any point of time, power gate sizes are smaller as compared to the fine-grain switches. Dynamic power simulation using worst-case vectors can determine the worst-case switching for the module and hence the size. The IR drop can also be factored into the analysis. Simultaneous switching capacitance is a major consideration in coarse-grain power gating implementation. In order to limit simultaneous switching, gate control buffers can be daisy chained, and special counters can be used to selectively turn on blocks of switches.

Isolation cells

Isolation cells are used to prevent short circuit current. As the name suggests, these cells isolate the power gated block from the normally-On block. Isolation cells are specially designed for low short circuit current when input is at threshold voltage level. Isolation control signals are provided by the power gating controller. Isolation of the signals of a switchable module is essential to preserve design integrity. Usually a simple OR or AND logic can function as an output isolation device. Multiple state retention schemes are available in practice to preserve the state before a module shuts down. The simplest technique is to scan out the register values into a memory before shutting down a module. When the module wakes up, the values are scanned back from the memory.

Retention registers:

When power gating is used, the system needs some form of state retention, such as scanning out data to a RAM, then scanning it back in when the system is reawakened. For critical applications, the memory states must be maintained within the cell, a condition that requires a retention flop to store bits in a table. That makes it possible to restore the bits very quickly during wakeup. Retention registers are special low leakage flip-flops used to hold the data of the main registers of the power gated block. Thus the internal state of the block during power down mode can be retained and loaded back to it when the block is reactivated. Retention registers are always powered up. The retention strategy is design dependent. A power gating controller controls the retention mechanism such as when to save the current contents of the power gating block and when to restore it back.

Stacking power gating technique:

In this technique, stacking sleep transistors are used to reduce the magnitude of peak current and voltage glitches in power rails i.e. ground bounce noise. In this technique, the leakage current is reduced by the stacking effect, turning both MSL1 and MSL2 sleep transistors off. Here, we apply the SELECT input in a manner by which the ground bounce noise is minimum this is achieved by adjusting the value of ΔT (this is the delay introduced to the SL signal using delayed buffer) which gives the summation of ground bounce noises of these two transistors minimum. When the value of ΔT is half of the oscillation period of the ground bounce noise then the positive peak of the ground bounce noise superimposes with the negative peak thereby bringing it closer to zero.

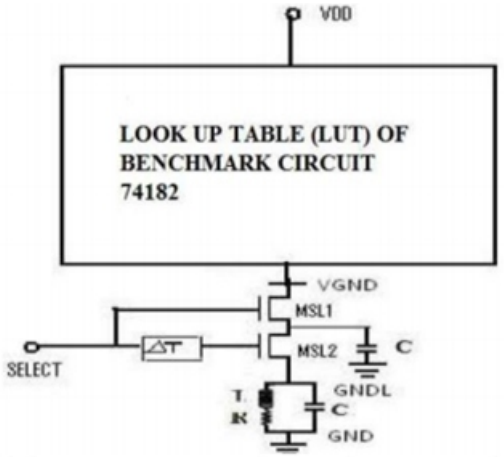

Fig: Look Up Table with stacking power gating technique.

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Diode based stacking power gating technique

If we incorporate the strategy which is operating the sleep transistor as a diode in stacking power gating leads diode based stacking power gating. Stacking sleep transistors (T1, T2) are used in diode based stacking power gating scheme shown in fig.3 reduce the magnitude of peak current and voltage glitches in power rails i.e. ground bounce noise. The diode based stacking power gating scheme consists of 5 parts:

1. Transistors T1, T2 are the sleep transistors which are high Vt transistors for less leakage current.
2. Transistor S1 is a control transistor used to make the sleep transistor S1 working as a diode during mode transition.
3. TG1 is the transmission gate.
4. Tn time delay provided for T1 and T2.
5. C2 is the capacitor inserted in the intermediate node VGND2.

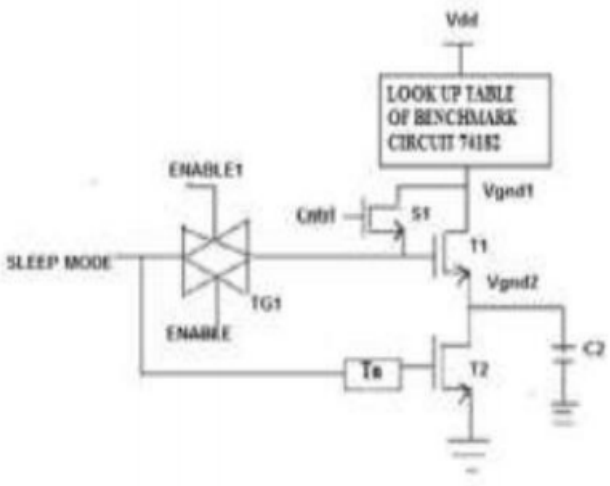

Fig. Lookup Table with diode based stacking power gating technique.

In this scheme, 3 strategies have been used to reduce the peak of ground bounce noise and leakage current.

1.Making the sleep transistor working as a diode during mode transition for some period of time due to this limitation in large transient hence reduction in the peak of ground bounce noise.

2.Isolating the ground for small duration during mode transition this was achieved by delay circuitry.

3.Turning ON the T2 transistor in linear region instead of saturation region to decrease the current surge was achieved by a capacitor placed in intermediate node.
Diode based staggered phase damping power gating technique

This technique can be understood by fig.below. The analyzed diode based staggered phase damping scheme consists of 5 parts:

1.Transistors T1, T2 are the sleep transistors which are high Vt transistors for less leakage current.
2.Transistors CT1, CT2 are the control transistors used to make the sleep transistors working as a diode during mode transition.
3. SG1, SG2 are transmission gates.
4. DIP-40 package pin ground bounce noise model connected beneath of the clusters.
5.Cluster1 and cluster2 denote logic blocks.

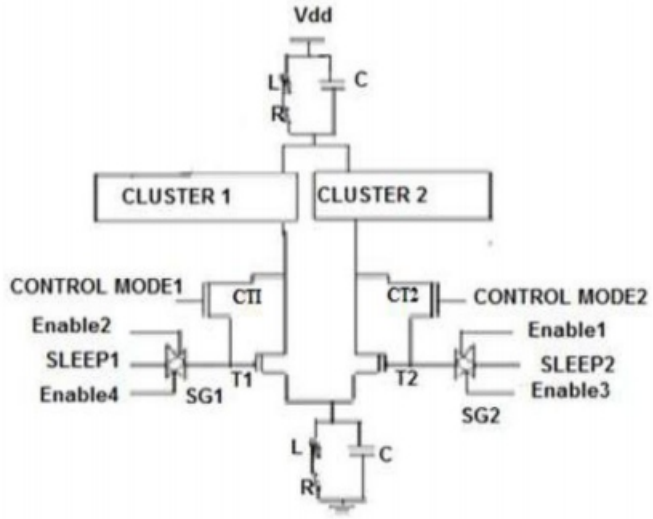

Fig: Look Up Table with diode based staggered phase damping power gating technique.

Comparative Analysis:

The complete simulation setup has been done with basic NAND gate including ground bounce noise model with stacking power gating scheme. Here the effectiveness of the stacking power gating scheme has been demonstrated using NAND gate circuits

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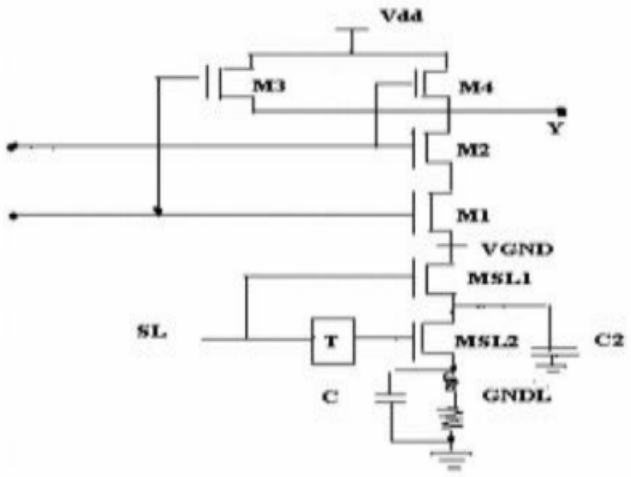

Fig.5. NAND gate circuit with stacking power gating scheme.

Leakage current has a strong exponential dependence on VGS and VGD, which leads to input sequence dependence. In the circuit, state of the transistors depends on the input vector. As in the case of 2- input NAND gate, pull down transistors both are turned ON when the input sequence is "1". Hence the leakage current in this case is maximum for 2- input NAND gate. When the input vector sequence is "00" pull down transistors are turned OFF due to stacking effect, hence the leakage current is reduced. All the mentioned results have been simulated under condition that all the logical inputs of NAND gate circuit are held at logic '1'. The worst case condition has been taken where leakage current is maximum, to show the effectiveness of the stacking power gating scheme. To show the improvement in leakage reduction, the stacking power gating scheme has been compared with conventional power gating scheme in terms of leakage current and power dissipation.The tradeoff between leakage current and power supply in power gating can be easily analyzed from the graph mentioned in the leakage current comparison of NAND gate without power gating scheme and with stacking power gating scheme (fig 6). The leakage current in standby mode is reduced by 87.14% over the conventional power gating scheme shows comparison of the average leakage power dissipation in standby mode over the duration of 10sec, for the conventional and stacking power gating schemes. It is analyzed that variation of leakage power dissipation with supply voltage is minimized in the stacking power gating schemes. Here a high performance stacking power gating schemes have been analyzed which minimizes the leakage power as well as control the ground bounce noise in transition mode.

The tradeoff between the ground bounce noise and wake-up latency has been explored for high performance power gating circuits. As recent trend is towards the nano-scale regime, power gating scheme is mostly used for reduction of leakage current. The ground bounce noise caused by the power gating structure is getting more prominent as the supply voltage is scaled down from 1.5V to 0.5V. The modified stacking power gating scheme reduces the leakage current by 87.14% and ground bounce noise by 76.28% compared to the conventional power gating structure. A comparative study is also done for leakage current and ground bounce noise reduction. In this Diode based stacking scheme is analyzed as the best among the existing schemes and leakage current is found to be least in stacking power gating scheme. This analysis provides an effective roadmap for high performance digital circuit designers who are interested to work with low power application in nanometer logic circuits. The penalty of using the stacking power gating scheme, diode based stacking power gating scheme which is also present in conventional power gating structure, is that the logic level of the circuitry is not retained during the sleep mode .Hence future works will be directed towards resolving this data retention issue.

Conclusion:

Stacking power gating technique has been analyzed and the conditions for the important design parameters. Minimum ground bounce noise have been derived. As recent trend is towards the nano-scale regime, power gating scheme is mostly used for reduction of leakage current. The ground bounce noise caused by the power gating structure is getting more prominent as the supply voltage is scaled down from 1.5V to 0.5V. The power consumption can be further reduced if the power supply system has the enhanced ability to adjust the output voltage level and low power in continuous manner. Research efforts are desired in developing such techniques. The penalty of using diode based staggered, diode based stacking power gating techniques or the conventional power gating structure are that the logic level of the circuitry is not retained during the sleep mode. Hence future works will be directed towards resolving this data retention issue.

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