ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Design of Parallel Prefix Adders Using Reversible Logic Gates

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Abstract:

The focus of this paper is the actual implementation of parallel prefix adders and verifies the functionality of the adder for arithmetic and logical operations used in processors and for D.S.P applications. The parallel prefix adders we mainly have are Parallel prefix adders (PPA) have the better delay performance. This paper investigates four types of PPA's (Kogge Stone Adder(KSA), Spanning Tree Adder (STA), BrentKung Adder (BKA) and Sparse Kogge Stone Adder (SKA)).Of all these adders we mainly focus on hybrid parallel prefix based components block instead of full adder circuits reversible gates are used such that high power consumption problems can be reduced.

Keywords:

parallel prefix adders, reversible logic gates ,peres gate,h.n.g gate,power ,residue number system,, Reverse converter.

I.INTRODUCTION:

In the world of battery-based and portable devices, the residue number system (RNS) can play a significant role due to its low-power features and competitive delay. The RNS can provide carry-free and fully parallel arithmetic operations [1], [2] for several applications, including digital signal processing and cryptography [3]–[6]. However, its real usage requires forward and reverse converters to be integrated in the existing digital systems. The reverse conversion,i.e., residue to binary conversion, is a hard and time-consuming operation [7]. Hence, the problem of designing high-performance reverse converters has motivated continuous research using twomain approaches to improve the performance of the converters:1) investigate new algorithms and novel arithmetic formulations to achieve simplified conversion formulas and 2) introduce new moduli sets, which can lead to more simple formulations.

Thereafter, given the final simplified conversion equations, they are computed using well-known adder architectures, such as carry-save adders (CSAs)and ripple and ripple-carry architectures, to implement carry-propagate adders (CPAs) and, more seldomly, fast and expensive adders such as the ones with carry-look ahead or parallel-prefix architectures. The binary addition is the basic arithmetic operation in digital circuits and it became essential in most of the digital systems including Arithmetic and Logic Unit (ALU), microprocessors and Digital Signal Processing (DSP). At present, the research continues on increasing the adder's delay performance. In many practical applications like mobile and telecommunications, the Speed and power performance improved in FPGAs is better than microprocessor and DSP's based solutions. Additionally, power is also an important aspect in growing trend of mobile electronics, which makes large-scale use of DSP functions. Because of the Programmability, structure of configurable logic blocks (CLB) and programming interconnects in FPGAs, Parallel prefix adders have better performance. The delays of the adders are discussed delay, power and area for the designed adders are presented and compared.

II. BACK GROUND:

The Chinese remainder theorem, or other related improved approaches and techniques [7] underlie the RNS reverse conversion,whose formulation can be directly mapped to ripple-carry adders (RCA). However, this leads to significant speed degradation, due to the linear increase of the delay in the RCA with the number of bits. Parallel-prefix adders can be used in the RNS reverse converters to bind the delay to logarithmic growth. However, in reverse converters,several parallel-prefix adders are usually required. Even when only one adder is used, the bit length of this adder is quite large.Consequently, this results in high power consumption notwithstanding its high speed. Therefore, in this section, two approaches that take advantage of the delay properties of the parallel

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prefix adders with competitive power consumption are introduced.Usually, one regular binary addition is required in reverse converterstructures to achieve the final binary representation. This final addition has an important effect in the total delay of the converter due to.

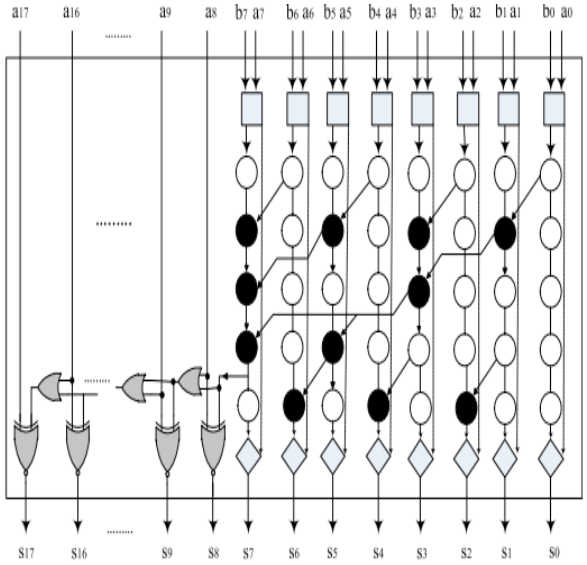

FIGURE 1:HRPX structure with BK prefix network:

The main reason for the high power consumption and area overhead of these adders is the recursive effect of generating andFig. 2. Modified excess-one unit.Fig. 3. HMPE structure.propagating signals at each prefix level. An optimized approach is proposed in [21], which uses an extra prefix level to add the output carry. However, this method suffers from high fan-out, which can make it usable only for small width operands. However, we could address this problem by eliminating the additional prefix level and using a modified excess-one unit instead.

In contrast to the BEC, this modified unit is able to perform a conditional increment based on control signals as shown in Fig. 2, and the resulted hybrid modular parallel-prefix excess-one (HMPE) adder is depicted in Fig. 3. The HMPE consists of two parts:

1) a regular prefix adder and 2) a modified excess-one unit. First,two operands are added using the prefix adder, and the result is conditionally incremented afterward based on control signals generated by the prefix section so as to assure the single zero representation.Summarizing, the HMPE is highly flexible, since it can be used with every prefix networks.

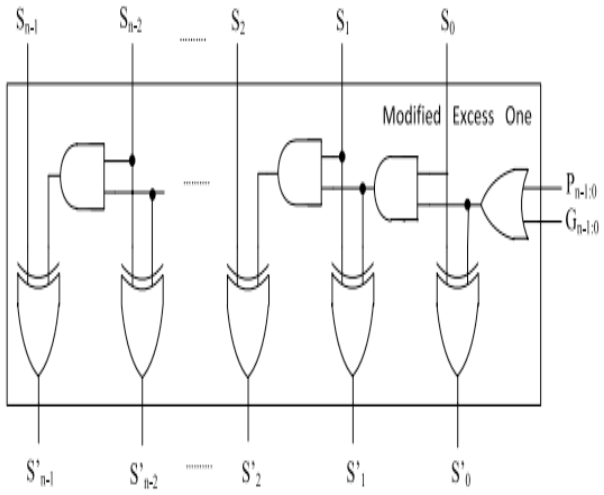

FIGURE 2:MODIFIED excess one unit

Hence, the circuit performance metrics such as area, delay, and power-consumption can be adjusted by selecting the desired prefix structure. On the other hand, the HRPX avoids the usage of a large size parallel-prefix adder with high powerconsumption, and also does not have the penalty of using the long carry-propagation chain of a RCA. PPA's basically consists of 3 stages

- Pre computation
- Prefix stage
- Final computation

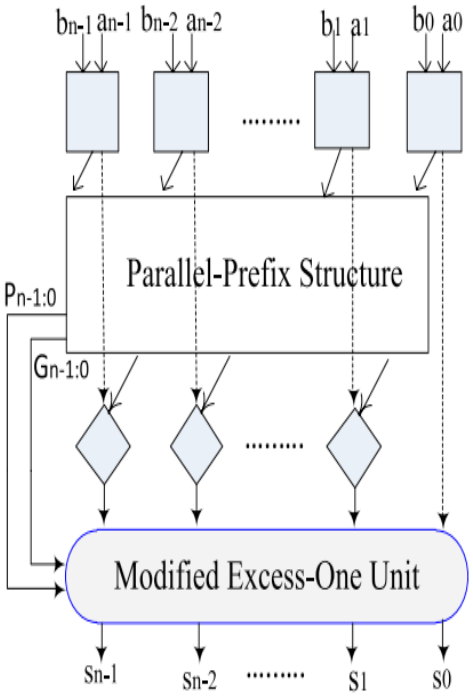

FIGURE 3:HMPE structure

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III. REVERSIBLE LOGIC GATES:

High-performance chips releasing large amounts of heat impose practical limitation on how far can we improve the performance of the system. Reversible circuits that conserve information, by un computing bits instead of throwing them away, will soon offer the only physically possible way to keep improving performance. Reversible computing will also lead to improvement in energy efficiency. Energy efficiency will fundamentally affect the speed of circuits such as nanocircuits and therefore the speed of most computing applications. To increase the portability of devices again reversible computing is required. It will let circuit element sizes to reduce to atomic size limits and hence devices will become more portable. Although the hardware design costs incurred in near future may be high but the power cost and performance being more dominant than logic hardware cost in today's computing era, the need of reversible computing cannot be ignored.

A. Reversible Function:

The multiple output Boolean function F(x1; x2; :::; xn) of n Boolean variables is called reversible if:
a. The number of outputs is equal to the number of inputs;
b. Any output pattern has a unique pre-image.
In other words, reversible functions are those that perform permutations of the set of input vectors

B. Reversible logic gate:

Reversible Gates are circuits in which number of outputs is equal to the number of inputs and there is a one to one correspondence between the vector of inputs and outputs. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs.

C. Ancilla inputs/ Constant inputs :

This refers to the number of inputs that are to be maintain constant at either 0 or 1 in order to synthesize the given logical function.

D. Garbage outputs:

Additional inputs or outputs can be added so as to make the number of inputs and outputs equal whenever necessary.

This also refers to the number of outputs which are not used in the synthesis of a given function. In certain cases these become mandatory to achieve reversibility. Garbage is the number of outputs added to make an n-input k-output function ((n; k) function) reversible. We use the words —constant inputs to denote the present value inputs that were added to an (n; k) function to make it reversible. The following simple formula shows the relation between the number of garbage outputs and constant inputs.
Input + constant input = output + garbage.

E. Quantum cost:

Quantum cost refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. The quantum cost of a circuit is the minimum number of 2*2 unitary gates to represent the circuit keeping the output unchanged. The quantum cost of a 1*1 gate is 0 and that of any 2*2 gate is the same, which is 1.

F. Flexibility :

Flexibility refers to the universality of a reversible logic gate in realizing more functions.

G. Gate Level :

This refers to the number of levels in the circuit which are required to realize the given logic functions.

H. Hardware Complexity :

This refers to the total number of logic operation in a circuit. Means the total number of AND, OR and EXOR operation in a circuit
The following are the important design constraints for reversible logic circuits.
•Reversible logic gates do not allow fan-outs.
•Reversible logic circuits should have minimum quantum cost.
•The design can be optimized so as to produce minimum number of garbage outputs.
•The reversible logic circuits must use minimum number of constant inputs.
•The reversible logic circuits must use a minimum logic depth or gate levels
Goals of reversible logic:
•1. Minimize the garbage outputs
•2. Minimize the constant inputs
•3. Minimize the total number of gates

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•4. Minimize the quantum cost

In the final stage computation instead of using full adders in the circuit we can use HNG gate.by using that slightly area gets increases but delay and power gets decreases.

HNG gate Architecture:

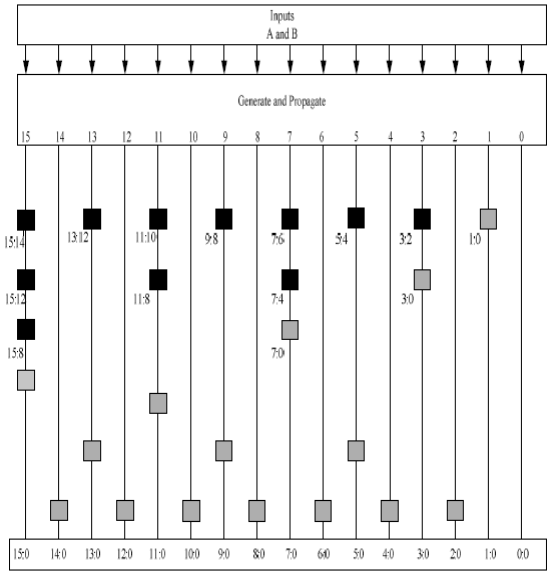
The reversible HNG gate can work singly as a reversible full adder. If the input vector IV = (A, B, Cin, 0), then the output vector becomes OV = (P=A, Q=Cin, R=Sum, S=Cout).

FIGURE 4:HNG gate:

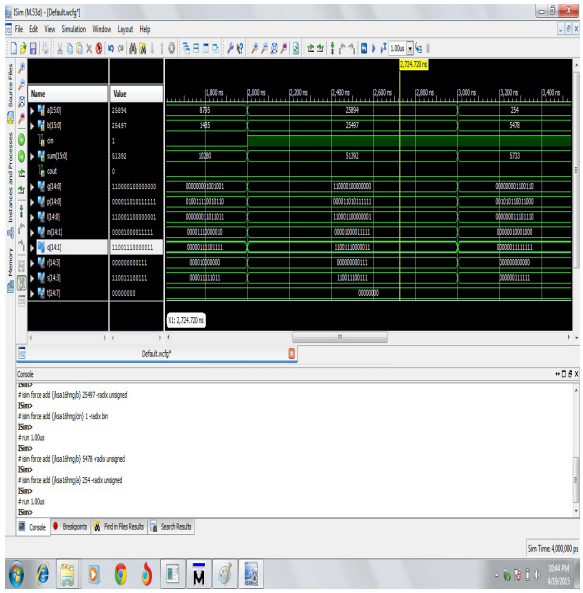
The most prominent application of reversible logic lies in quantum computers. A quantum computer will be viewed as a quantum network (or a family of quantum networks) composed of quantum logic gates; It has applications in various research areas such as Low Power CMOS design, quantum computing, nanotechnology and DNA computing. Quantum networks composed of quantum logic gates; each gate performing an elementary unitary operation on one, two or more two–state quantum systems called qubits. Each qubit represents an elementary unit of information; corresponding to the classical bit values 0 and 1. Any unitary operation is reversible and hence quantum networks effecting elementary arithmetic operations such as addition, multiplication and exponentiation cannot be directly deduced from their classical Boolean counterparts (classical logic gates such as AND or OR are clearly irreversible).Thus, quantum arithmetic must be built from reversible logical components . Reversible computation in a system can be performed only when the system comprises of reversible gates. A circuit/gate is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments.

An N*N reversible gate can be represented as
Iv=(I1,I2,I3,I4,……IN)
Ov=(O1,O2,O3,……ON).
Where Iv and Ov represent the input and output vectors respectively.
In quantum computing, by considering the need of reversible gates, a literature survey has been done and the mostly available reversible logic gates are presented in this paper.

1V PROPOSED CIRCUIT DIAGRAM:



V Results:



AREA CALCULATION:

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Device utilization summary:
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Selected Device : 3s100evq100-5

 Number of Slices:                       33  out of    960     3%
 Number of 4 input LUTs:                 58  out of   1920     3%
 Number of IOs:                          50
 Number of bonded IOBs:                  50  out of     66    75%
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AREA CALCULATION :

Name of the Adder	No. of Slices	No. of LUT's	No. of IO's	No. of IOB's	Delay(ns)
Brent Kung Adder	19	35	50	50	15.436
Reversible Brent Kung Adder	19	35	50	50	16.252

DELAY CALCULATIONS:

Name of the Adder	Area	Delay(pico seconds)	Power (nW)
Brent Kung Adder	786272	2617	31611171.994
Reversible Brent Kung Adder	786175	2567	31609616.964

POWER CALCULATION:
VI APPLICATION:

When multiple routers are used in interconnected networks, the routers exchange information about destination addresses, using a dynamic routing protocol. Each router builds up a table listing the preferred routes between any two systems on the interconnected networks. A router has interfaces for different physical types of network connections, (such as copper cables, fiber optic, or wireless transmission). It also contains firmware for different networking protocol standards.

VIII CONCLUSION:

A simple approach is proposed in this paper to reduce the delay and power of Parallel Prefix Adders. The delay of 16-bit Reversible Kogge Stone Adder is less when compared to all other adders and the power of Reversible Brent Kung Adder is less compared to all other adders. Thus Reversible kogge stone adder is used for high speed applications and Reversible brent kung adder is used for low power applications.

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