

VLSI Implementation of High Performance Reversible Comparator in DNA Computing

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Abstract:

Reversible Logic Plays a very important role in research fields like quantum computing, optical computing, nanotechnology, low power computing and DNA computing. Reversibility has become the most promising technology in digital circuit design to reduce energy loss. This problem of energy loss can be solving by using reversible circuits where conventional logic has failed. Reversible circuits consume less power by recovering bit loss from its unique input-output mapping. This paper presents two new reversible gates , one with the use of RC gate and other one using a derivative gate constructed from RC gate are used to design an n-bit binary comparator. This proposed circuit works correctly and gives better results compared to existing ones. It reduces the fundamental parameters like quantum cost, garbage output, delay and number of gates. The simulation results of proposed comparator offers higher performances than existing ones. The comparator is implemented using Verilog HDL and it is targeted for Xilinx Spartan3 EDK FPGA.

Key words: DNA computing, reversible logic circuits, delay

I. INTRODUCTION:

Most of network applications follow a layered approach to the system implementation. This systematic approach enables interaction between the contain of Front End Design and Back End design these days. While front end design involves digital design using HDL, design verification through simulation and other verification techniques like

design from gates and design for testability, backend design contains of CMOS library design and its imitation. It also covers the physical design and fault simulation. While Simple logic gates might be treated as SSI devices and multiplexers and parity encoders as MSI, the world of VLSI is much more diverse. Generally, the total design procedure follows a step by step approach in which each design step is followed by simulation before the hardware or moving on to the next step. In recent time every sort of computation is getting complex and researchers are facing huge challenges over billions of arithmetic operations per second. According to Gordon Moore, the transistor count and execution of logic circuits is doubled in every two years, this process will continue until semiconductor circuits reach to its physical limit. Thus execute ultra speed computation leads us to various kinds of computing technology such as Quantum Information Processing, DNA Computing, etc. But we live in a world of classical or irreversible architecture where unused energy is consumed due to power loss. This is because, Landauer proved erasure of each bit of information consumes at least $KT \times \ln 2$ joules of energy where K is the Boltzmann's constant and T is the absolute temperature at which the operation is being performed. In 1973, Bennet [2, 5] had shown that energy dissipation problem of VLSI circuits can be overcome by using reversible logic. This is so because reversible computation does not erase any bit of information and therefore it does not consumes any energy for computation. Generally, reversible logic performs Boolean operations having equal number of inputs and outputs where input states are uniquely mapped to individual output states or vice versa. Also

reversible logic should never permit feedbacks. Reversible logic does multiple operations per cycle without losing any input bits. As a result zero power consumption would be achieved if a logic circuit consists of reversible gates. Reversible logic can easily be operated for Fault Testing, Embedded Devices, Digital Signal Processing, Quantum Dot Cellular Automata, etc. Comparison of two binary numbers finds its wide application in general purpose microprocessors, communication systems, encryption devices, sorting networks, etc.

In the past decade, reversible logic has gained popularity among researchers in the VLSI domain. Power dissipation is one of the most important criteria in VLSI design where optimizing the amount of power dissipated is the main requirement in low power VLSI design. According to R. Landauer, a small amount of finite energy is always released in an irreversible operation in which bit(s) being erased. He commented that the energy released or dissipated in an irreversible computation is " $kT \ln 2$ " joules.

Reversible logic has the ability to reduce the amount of power being dissipated and finds extensive use in numerous other technologies such as quantum computing [1], nanotechnology, optical information processing [2], low power CMOS design [3], DNA computing and bioinformatics. In this logic, one to one mapping exists between the inputs and outputs, the number of inputs and outputs is equal, and inputs can be recovered from outputs. Reversible gates in circuits achieve no information loss and zero power consumption [5]. Minimizing number of gates, quantum cost, garbage outputs and constant outputs are very important in reversible logic [6].

The resemblance of two binary inputs numbers is a major application in microprocessor, encryption device, communication systems, sorting networks etc. The theorems and lemmas show the efficiency of reversible logic synthesis of n-bit comparator. This paper presents two new reversible gates, one with the use of RC gate called as RC-I and

other one using a derivative gate constructed from RC gate called as RC-II are used to design an n-bit binary comparator.

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DNA computing is a branch of computing which uses DNA, biochemistry, and molecular biology hardware, instead of the regular silicon-based computer technologies. DNA computing—or, more generally, biomolecular computing—is a fast-developing interdisciplinary area. Research and development in this area involves theory, experiments, and applications of DNA computing. The term "moletronics" has sometimes been used, but this term had already been used for an earlier technology, a then unsuccessful competition of the first integrated circuits; this term has also been used more generally, for molecular-scale technology.

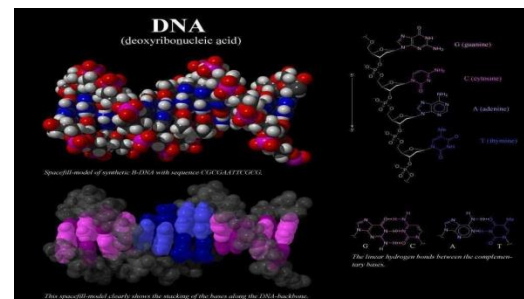


Fig 1. Image of DNA

DNA computing is a form of parallel computing in that it takes advantage of the many different molecules of DNA to try many different possibilities at once.^[14] For certain specialized problems, DNA computers are faster and smaller than any other computer built so far. Furthermore, particular mathematical computations have been demonstrated to work on a DNA computer. As examples, DNA molecules have been utilized to tackle the assignment problem and GPS mapping. Ar an Nayebi has provided a general implementation of Strassen's matrix multiplication algorithm on a

DNA computer, although there are problems with scaling. In addition, Caltech researchers have created a circuit made from 130 unique DNA strands, which is able to calculate the square root of numbers up to 15.

DNA computing does not provide any new capabilities from the standpoint of computability theory, the study of which problems are computationally solvable using different models of computation. For example, if the space required for the solution of a problem grows aggressively with the size of the problem (EXPSPACE problems) on von Neumann machines, it still grows aggressively with the size of the problem on DNA machines. For very large EXPSPACE problems, the amount of DNA required is too large to be practical.

Following are the main advantages of using DNA-based circuits over the existing silicon chips:

- In double strands DNA, the data density will be one base per square nanometer and this density will be over one million Gbits per square inch, where in typical high performance hard drive, the data density is about 7 Gbits per square inch [12-15].
- Base pair complementation gives a unique error correction mechanism that works like RAID 1 array.
- As many copies of the enzyme can work on many DNA molecules simultaneously. This is the power of DNA computing that can work in a massively parallel fashion.
- DNA is a stable molecule that never suffers from any changes (mutation) unless it faces harsh (very high temperature, corrosive agents etc) environment.
- Logic gates based on DNA can be preserved for a very long time (more than a decade) by maintaining and altering temperature up to certain point of temperature.

So, a DNA-based logic circuit will have self error recovery capability, and will take less space. Moreover, it will have faster read-write capability over existing gate and employ massive parallelism. As

DNA-based Toffoli gate inherits the properties of DNA-based circuit, it will perform better than existing Toffoli gate.

II. LITERATURE REVIEW

The literature survey presented in the following section has been categorized in different sub-sections for better understanding. The first few sections give a brief introduction reversible logic gates, garbage output, quantum cost are discussed below.

Reversible Logic

Reversibility can be explained by the basic idea of one to one mapping between the input and output where the number of input is equal to the number of output for the system. The one to one mapping requirement puts a restriction on the fan out of the system i.e. there cannot be more than one output associated with each input to preserve reversibility and thus, the resulting circuit must be acyclic. This can help us to reduce the overall energy dissipation of computations, which can in turn increase battery life or processing speed in heat-limited systems. It also restricts the design and implementation of systems which requires feedback from the output (as in the sequential circuits) because having a feedback loop in the system threatens the bijectivity of the system and thus, the reversibility of the system.

The simple reversible NOT gate is 1×1 gate and Toffoli is a 3×3 gate, Fredkin is a 3×3 gate

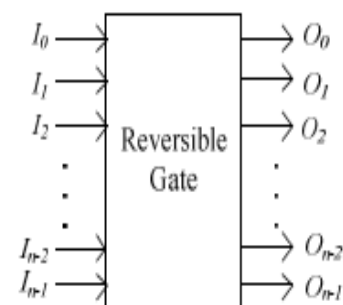


Fig 2 : $k \times k$ reversible gate

Garbage Output

The outputs which are not used in the reversible gates are known as garbage outputs which are needed to maintain the reversibility. For each garbage outputs heavy price is paid off.

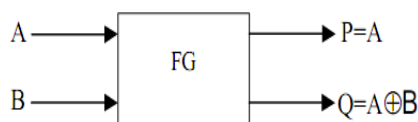


Fig 3: Feynman Gate

When a *Feynman gate* is used for *EX-OR* operation of two inputs, extra one output is generated at the output part in addition to the *EX-OR* output. This additional output is known as garbage output [4].

Quantum Cost

This refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1x1 or 2x2) required to realize the circuit. Quantum cost of *Feynman* gate is 2, *Toffoli* gate is 5 etc.

As far as the designs of single-bit comparator are concerned: In [8], the author used five reversible gates out of which two are NG, two FG and a single NLG gate. Also, the ancillary inputs used are 6 in number with a delay of 3 units and 3 garbage outputs. The author used a NLG gate whose quantum cost is justified to be 2 [6], due to which the total quantum cost of the single bit comparator circuit becomes 26. In [9], the author put forth a number of comparator designs but only two of those designs are taken in this work. The first design used PG, BJNG and FG gate, one each and delivers output with 5 ancillary inputs, 2 garbage outputs, delay of 3 units, and quantum cost of 10. The second design used one BJNG, one FG and two TG gates producing 2 garbage outputs, 5 ancillary inputs, and delay of 4 units. The circuit is designed with a quantum cost of 16. In [6], the researcher designed single-bit comparator using a single ZRQC module derived from ZRQG gate. The design is having a quantum cost of 7, single unit delay and single

garbage output. The work proposed a ZRQC module which happens to work as single-bit comparator using 2 ancillary inputs while the author has stated it to be 4 [6]. On the other hand, the designs of four-bit comparator specified:

In [8], the proposed four-bit reversible comparator design used 53 gates, 13 units delay, 23 garbage outputs and 59 ancillary inputs. The comparator design's quantum cost is not calculated in the work but it is argued to be 311 as mentioned in [6].

In [10], the design of four-bit reversible comparator was not directly obtained but by using the 8-bit quantum comparator design. The design is justified to be consisting of 32 reversible gates, delay of 15 units, 21 ancillary inputs, 18 garbage outputs, and a quantum cost of 90 [6].

Referring to [6], the author described the use of 4 ZRQC1 modules, 6 Peres gates and 6 Feynman Gates making it a total of 16 reversible gates. Besides, the design produced 20 ancillary inputs, 11 units delay, 17 garbage outputs and total quantum cost of 50 units. The previous efficient design of a single-bit comparator has two ancillary inputs and single garbage output utilizing 7 units of quantum cost and that of a four-bit reversible comparator, delivers 50 units of quantum cost.

III. PROPOSED METHODOLOGY

Here, we proposed high performance reversible n-bit binary comparator. The comparator compares the magnitude of two binary numbers to determine whether they are equal, greater or less than the other. We usually compare from most significant bit (MSB) to least significant bit (LSB). So we can divide the n-bit comparator circuit into two parts: MSB comparator is used to compare MSB and to propagate comparing results from less to least significant bit we use two new reversible gates namely RC-I and RC-II gates are used to design a comparator.

In MSB comparator, we generate Q_n , R_n and S_n by using our proposed *MSB comparator gate*. On the other hand, *RC gates* propagates those Q_n , R_n and S_n with help of $(A > B)$ and $(A < B)$, (where A , B are two binary comparator input) to calculate Q_{n-1} , R_{n-1} , S_{n-1} . Similar procedures carry on to generate Q_1 , R_1 , S_1 .

Since it is binary n -bit comparator we need one MSB Comparator and $n-1$ RC gates.

One-bit comparator using Peres and BJJ gate

Reversible one bit comparator is implemented with Feynman gate and Peres gate and BJJ gate as shown in fig.17. The number of garbage outputs are two and represented as G1 and G2, it uses three constant inputs one logic '0' and two logic '1' [11].

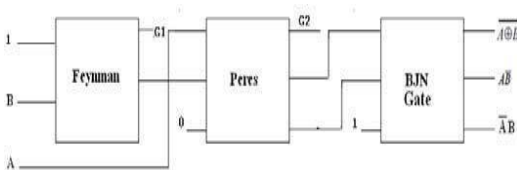


Fig.4. one bit comparator using Peres gate

Reversible MSB comparator

The MSB comparator circuit works with two binary inputs and sets two constant inputs as 0 and 1. It gives three outputs based on their inputs. lb, gb and eb are the outputs from the MSB comparator. The MSB comparator circuit is derived from BJS gate. The MSB comparator circuit is shown below in figure 3. These MSB comparator output is fed into the next level, where $(n-1)$ th bits have also compared.

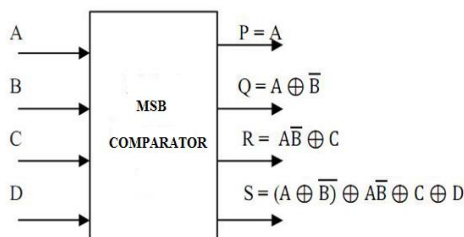


Figure 5. MSB Comparator

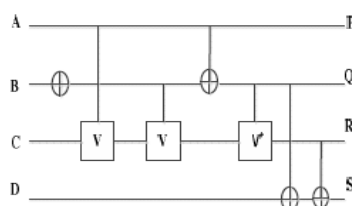


Fig 6 : Quantum realization of NPG

RC-I and RC-II gates:

First generates followings: $(A_{n-1} > B_{n-1})$ and $(A_{n-1} < B_{n-1})$, where- $(A_{n-1} > B_{n-1}) = (A_{n-1} B_{n-1}')$ and $(A_{n-1} < B_{n-1}) = (A_{n-1} B_{n-1})' \oplus (A_{n-1} \oplus B_{n-1})'$. Then, using above bits, it generates- $Q_{n-1} = (R_{n-1} \oplus S_{n-1})'$, $R_{n-1} = (A_{n-1} > B_{n-1}) Q_{n-1} \oplus R_n$ and $S_{n-1} = (A_{n-1} < B_{n-1}) Q_{n-1} \oplus S_n$. Similar procedures are continued to the LSB. The RC-I gate is a reversible gate which is shown in figure 5 and the RC-II gate is also reversible gate which a derivative gate constructed from RC-I gate which is shown in figure 2.

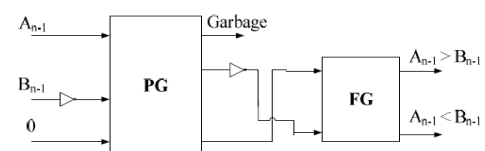


Fig 7: RC - I Gate

The RC-I gate can be constructed by using existing reversible gates like Peres, Feynman gates. The RC-I gate contains one Peres gate and Feynman gate shown in fig. The RC-II gate is derivative gate constructed from RC-I gate. It contains two PG and two FG and Not gate.

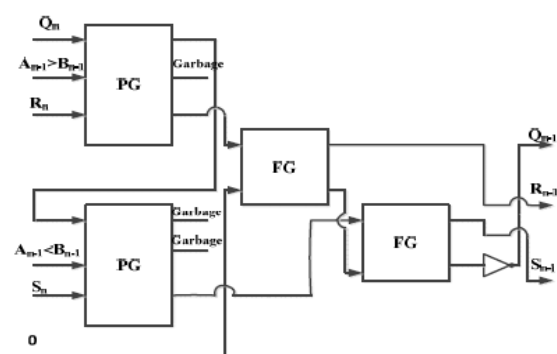


Fig 8 : RC-II gate

A circuit formation of two cells for the highest order bit and the lower order bits should be sufficient to manifest the 2-bit to n -bit circuits, where n is any positive integer greater than two ($n \geq 2$). A 2-bit circuit has two bits- most significant and least significant. For

greater than two bit circuit, it has at least two bits-*MSB* and *LSB*. A circuit comprised of two cells (one for the *most significant bit* and other for the *least significant bits*), can be used to construct n -bit circuits where $n \geq 2$. So, it verifies the above statement.

Input		Output		
A	B	$(A > B)$	$A < B$	$A = B$
0	0	0	0	1
0	1	0	1	0
1	0	1	0	0
1	1	0	0	1

Table 1: Truth table of 1-bit comparator circuit

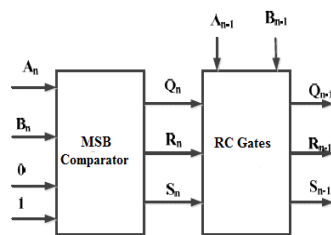


Fig 9: n-bit comparator circuit

VI. RESULTS

The simulation results for 1-bit, 2-bit, 3-bit and 4-bit reversible binary comparator using tanner and H spice tools to simulate the output. The comparative study on the existing one-bit comparator and the proposed one-bit comparator are depicted as shown in Figures below.

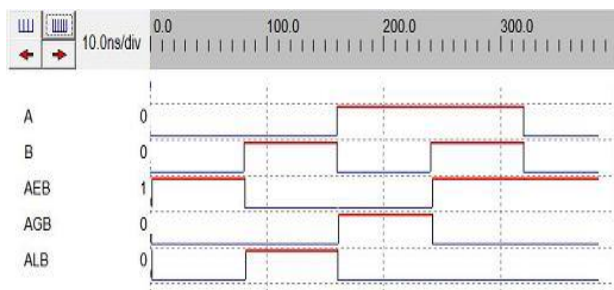


Fig 10: Simulation Result of Reversible 1-bit Comparator

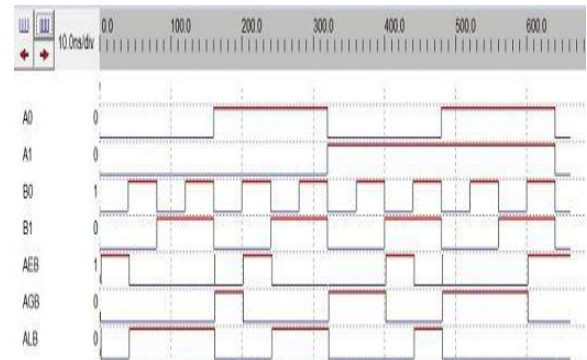


Fig 11: Simulation Result of Reversible 2-bit Comparator

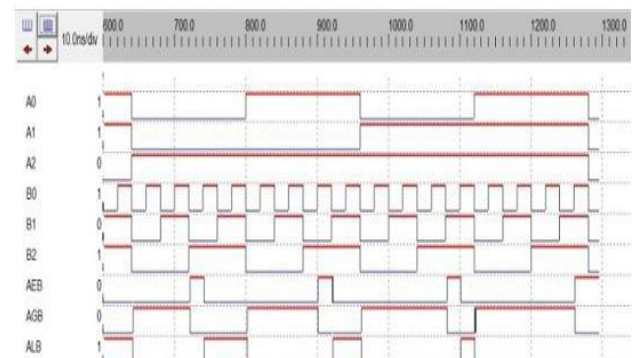


Fig12: Simulation Result of Reversible 3-bit Comparator

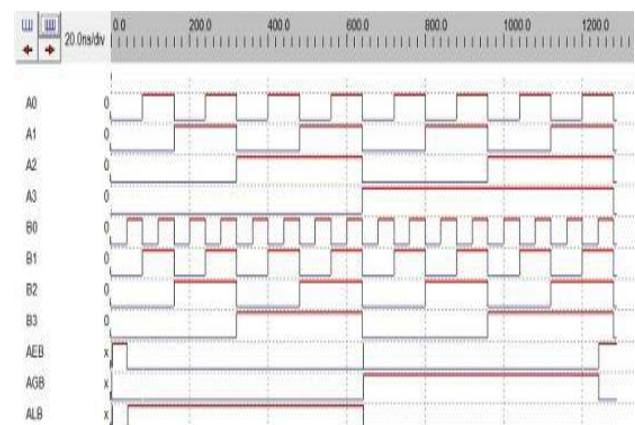


Fig 13: Simulation Result of Reversible 4-bit Comparator

IV CONCLUSION:

The existed paper presents an optimized reversible comparator circuits which are used in research fields like quantum computing, optical computing, nanotechnology, low power computing and DNA computing. We have proposed design of the reversible comparator in DNA computing. The comparator circuit in the proposed work is more effectively utilized than previous literature works. However, this improvement in the design comes at the cost of one extra line count. A novel design for the comparator is then presented which proves to be more efficient as compared to the previous literature works in terms of parameters like quantum cost and gate count. We have realized a new approach to design DNA-based reversible comparator, where both inputs and outputs are DNA bases and computations are performed using several biochemical operations. Proposed DNA-based comparator using reversible gates holds the properties of the original one. Finally, a DNA-based reversible composite circuit has shown using proposed gate, which creates the possibility to simulate any other composite reversible circuit using proposed gate.

Reversibility has become the most promising technology in digital circuit design to reduce energy loss. The design is very useful for the future computing techniques like ultra-low power digital circuits and quantum computers. It is shown that the proposal is highly optimized in terms of number of reversible logic gates, number of garbage outputs, number of constant inputs and number of transistor count. The performance parameters are optimized in comparison with the existing comparator designs

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