ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Analysis of FPGA Based CDMA Trans-Receivers

Shivani S
PG Scholar,
Department of ECE,
Sree Nidhi Institute of Science & Technology,
Hyderabad, India.

S.P.V Subba Rao
Professor,
Department of ECE,
Sree Nidhi Institute of Science & Technology,
Hyderabad, India.

Abstract:

Conventional communication systems such as TDMA and FDMA are becoming inadequate for some applications in today's communication requirements. A new technology called CDMA was used in 1957 to replace the mentioned technologies. The idea of this technology is to transmit signals simultaneously through a linear band limited channel without inter channel or inter symbol interference. CDMA utilizes a spread spectrum technique in which a spreading signal is uncorrelated to the signals and has a large bandwidth which is used to spread the narrow band message signal. In the proposed work, simulation of the functionality of CDMA system is realized on Xilink ISE platform. Here, Gold Code generator is used to generate the PN sequences and Turbo Encoder is used to generate the Convolution codes. At the receiver section, Viterbi algorithm is used to decode the Convolution Codes.The simulation results show the working of CDMA transmitter and receiver on VHDL platform. Implementation of proposed system is targeted on Virtex 5 FPGA.

Keywords:

Gold code generator, Turbo encoder, OVSF, Spreding Code, Virtex 5.

I. INTRODUCTION:

Cellular technology has grown tremendously both in terms of traffic and the services it offers. The mobile telecommunication industry has been facing the problem to provide a technology that should be able to support a variety of services ranging from voice communication with a bit rate of few Kbps to wireless multimedia in which bit rate up to 2 Mbps. This tremendous growth has also been fueled by the recent improvements in the capacity of wireless links due to the use of multiple access techniques. The idea is to transmit signals simultaneously through a linear band limited channel without inter channel or inter symbol interference.

To design multi channel transmission, it must concentrate on reducing cross talk between adjacent channels.
One of the most promising cellular standards is IS-95A code division multiple access (CDMA) system. The advantages of IS-95A CDMA standard over other standards are optimum subscriber station power management, bandwidth recycling, efficient power control, multilayer diversity and compatibility. The forward link frequency is in the range of (869-894) MHz and reverse link frequency is in the range of (824- 849) MHz. In the mobile communication transmission from the base station to mobile receiver are on the forward link and the transmission from the mobile user to the base station are on the reverse link. VHDL implementation of DS-CDMA transmitter and receiver has been proposed in this thesis. In this project pseudo noise code is generated by using Gold Code generator. Code signal is called as chip signal. The chips modulated by the carrier using a digital modulation technique BPSK.

The carrier is generated by using the technique discrete digital frequency synthesizer. CDMA base stations must be able to discriminate this different code sequences in order to distinguish one transmission from other .This discrimination is accomplished by means of a matched code filter .A matched code filter is a filter whose frequency spectrum is exactly designed to match the frequency spectrum of the input signal. Here matched code filter generating the pseudo noise code, generated noise code is correlated with the received code and detecting original data. In the recent years the CDMA on FPGA platform has attracted attention of academic research and industry. The Spartan TM-3E family of Field-Programmable Gate Arrays (FPGAs) is specifically broadband designed to meet the needs of high volume, cost-sensitive consumer electronic applications. The five-member family offers densities ranging from 100,000 to 1.6 million system gates. Because of their exceptionally low cost, Spartan -3E FPGAs are ideally suited to a wide range of consumer electronics applications, including access, home networking, display/ projection, and digital television equipment.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

II.MULTIPLE ACCESS TECHNIQUES:

Multiple access is a technique where many subscribers or local stations can share the use of a communication channel at the same time or nearly so despite the fact originate from widely different locations. A channel can be thought of as merely a portion of the limited radio resource, which is temporarily allocated for a specific purpose, such as someone's phone call. A multiple access method is a definition of how the radio spectrum is divided into channels and how the channels are allocated to the many users of the system. Since there are multiple users transmitting over the same channel, a method must be established so that individual users will not disrupt one another. There are three basic schemes

1. Frequency Division Multiple Access (FDMA)
2. Time Division Multiple Access (TDMA)
3. Spread Spectrum Multiple Access (SSMA)

- Frequency Hopped Multiple Access (FHMA)
- Code Division Multiple Access (CDMA)

1.Frequency Division Multiple Access (FDMA):

Each user is allocated a unique frequency band or channel. These channels are assigned on demand to users who request service. In Frequency Division Duplexing, the channel has two frequencies – forward channel & reverse channel. During the period of the call, no other user can share the same frequency band. If the FDMA channel is not in use, then it sits idle and cannot be used by other users to increase or share capacity. Receiver only has to know the frequency to tune in to.

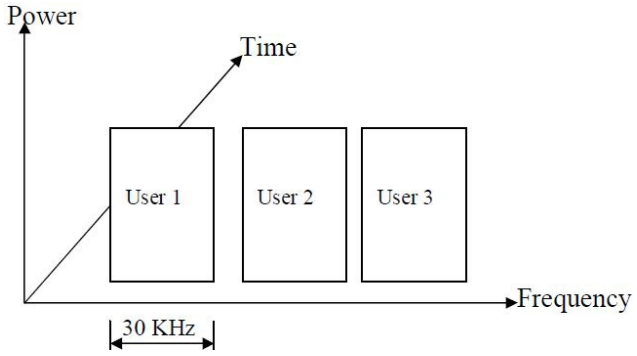


Figure 1: FDMA channel allocation

2.Time Division Multiple Access (TDMA) :

TDMA allows access to entire frequency bandwidth but for a limited amount of time. All senders use same frequency in at different time. If two transmissions overlaps, known as co-channel interference. Precise clock synchronization required.

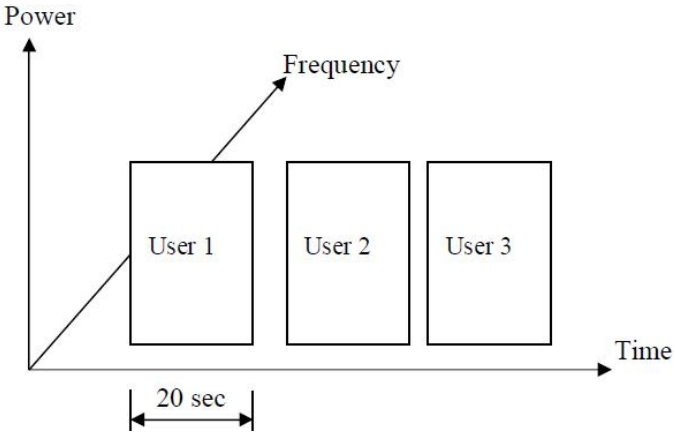


Figure 2: TDMA channel allocation

3.Spread Spectrum Multiple Access (SSMA)

Spread spectrum multiple access (SSMA) uses signals which have a transmission bandwidth that is several orders of magnitude greater than the minimum required RF bandwidth. A pseudo-noise (PN) sequence converts a narrowband Signal to a wideband noise-like signal before transmission. SSMA also provides immunity to multipath interference and robust multiple access capability. SSMA is not very bandwidth efficient when used by a single user. However, since many users can share the same spread spectrum bandwidth without interfering with one another. Spread spectrum systems become bandwidth efficient in a multiple user environment. It is exactly this situation that is of interest to wireless system designers. There are two main types of spread spectrum multiple access techniques; frequency hopped multiple access (FH) and direct sequence multiple access (DS). Direct sequence multiple access is also called code division multiple access (CDMA). There are three types of spread spectrum techniques by which the bandwidth of the signal can be spread. They are

•Frequency hopping (FH): The signal is rapidly switched between different frequencies within the hopping bandwidth pseudo-randomly, and the receiver knows beforehand where to find the signal at any given time.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

•Time hopping (TH): The signal is transmitted in short bursts pseudo-randomly, and the receiver knows before hand when to expect the burst.
•Direct sequence (DS): The digital data is directly coded at a much higher frequency. The code is generated pseudo-randomly, the receiver knows how to generate the same code, and correlates the received signal with that code to extract the data.

III.IMPLENTATION DESIGN OF DS-CDMA TRANSMITTER:

Block diagram for implementing the CDMA Transmitter is shown below:

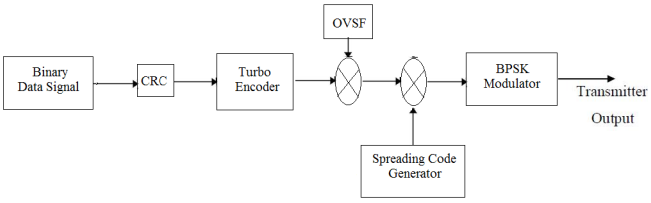


Figure 3: DS-CDMA Transmitter block diagram

In DS-CDMA transmitter, the input data bits are spread by Gold Code generator. The spreading is actually done by multiplying the data bits with that of the Gold Code generated. The frequency of Gold Code is higher than the Data signal. After spreading, the Data signal is modulated and transmitted. There are several schemes available for modulation, viz. BPSK, QPSK, M-QAM etc. The most widely used modulation scheme is the BPSK. The main reason is that the BPSK offers acceptable BER while transmitting signals of relatively low energy.In this design, BPSK modulation is used to modulate and transmit the spreader signal.

A.Design of Cyclic Redundancy Check:

The CRC is an efficient technique for determining and detecting the errors during digital transmission of the data signals. In this technique, the data signal is appended with a check word say,r. This combination of signal is processed across the transmitter and is then transmitted. For example, consider the message signal, M=110011.Let P represents the combination of 1's and 0's for which check word is generated. Let P=11001. CRC principle is used on the polynomials, hence M (x) = x 5 + x 4 + x+ 1, and, x (x) = x4 + x 3 + 1.

Modulo-2 arithmetic operation is performed on M(x) and P(x). The resultant of this operation is considered as the check word, r.

B.Design of Turbo Encoder:

A turbo code is formed from the parallel concatenation of two codes separated by an interleaver. The fundamental turbo code encoder is built using two identical recursive systematic convolutional (RSC) codes with parallel concatenation. An RSC encoder is typically r = 1/2 and is termed as component encoder. The two component encoders are separated by an interleaver. The main purpose of the interleaver is to randomize bursty error patterns so that it can be correctly decoded. It also helps to increase the minimum distance of the turbo code. Only one of the systematic outputs from the two component encoders is used, because the systematic output from the other component encoder is just a permuted version of the chosen systematic output.

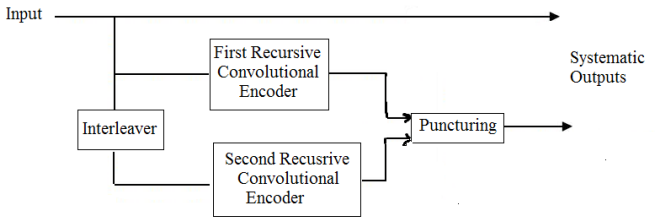


Figure 4: Turbo Encoder with puncturing

Puncturing is a technique used to increase the code rate. A rate 1=3 encoder is converted to a rate 1=2 encoder by multiplexing the two coded streams. The multiplexer can choose the odd indexed outputs from the output of the upper RSC encoder and its even indexed outputs from the lower one.

C.Design of OVSF:

To preserve the orthogonality between different channels in the communication systems,OVSF codes are generated.The coded data is first spreaded over the Orthogonal Variable Spread Factor (OVSF) code. The OVSF code is generated with the help of an OVSF tree. Each stage of the tree has a different Spreading Factor.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

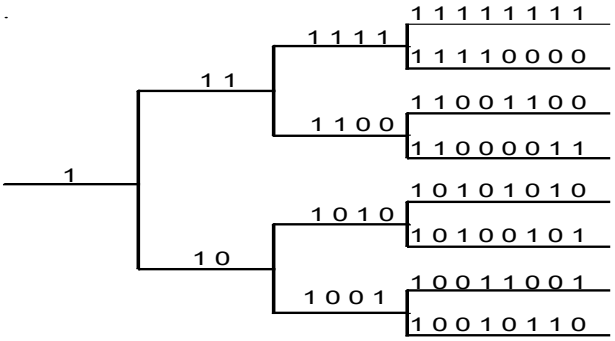


Figure 5: OVSF code tree

For each Spreading Factor, there are an equal number of possible codes. Figure 5 shows an example of the OVSF code.

D.Design of Spreading Code generator:

The important block of DS-CDMA communication system is the PN sequence generator. A Pseudo-random Noise (PN) sequence/code is a binary sequence that exhibits randomness properties but has a finite length and is therefore deterministic. The PN sequence generator can be implemented using LFSR's to generate several types of PN sequences. Two types of PN sequence generators implemented in this project. They are ML sequences and gold codes.Maximal length sequence are LFSR based PN sequence generators which can produce the maximum possible length sequence. For n bit size shift registers the PN sequence length will be 2n-1 bits.Gold codes are obtained by combining two PN sequences and modulo-2 adding, or XORing, the output together. Figure 1 shows the basic block diagram of LFSR based on shift register. The feedback from different shift register which influence the input is called taps. This feedback arrangement can be expressed in finite field arithmetic as a polynomial mod 2. The period of sequence is 2n-1, where n is number of shift register. Tapping is provided according to following equation. For eg: First ML sequence g1 is given by X5 +X2 +1 and second ML sequence g2 is given by X5 +X4 +X3 +X2 +1 .

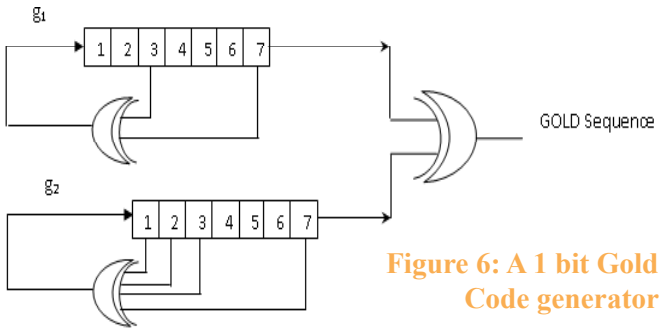


Figure 6: A 1 bit Gold Code generator

Generated Gold Code sequence:

SEED USED	GOLD CODE OBTAINED
10000	0 0 0 0 0 0 0 1 1 0 1 1 1 1 0 1 1 0 1 0 0 0 1 1 1 1 1 1 0 1 0
10110	0 0 0 0 0 0 1 1 0 0 1 1 0 0 0 1 0 0 0 0 1 0 0 0 1 0 1 1 1 1 1
11000	0 0 0 0 0 0 1 0 1 1 0 0 0 1 1 0 1 1 1 0 0 1 0 0 0 0 0 1 1 1 0

E.Design of Modulator:

Modulation is the process of changing some characteristics of a carrier wave in proportion to the signal to be transmitted. A general equation for a sine wave is:

$e(t)=EC \sin(2\pi fc\, t + Q)$ (1)

where, e(t) is instantaneous amplitude of the sine wave as a function of time.

EC = Peak amplitude of the sine wave.

fc =Frequency of the sine wave in hertz.

t= Time in seconds.

Q= Phase in radians.

Equation one suggests that there are only 3 ways; the sine wave can be changed:

- The amplitude Ec.
- The frequency fc .
- The phaseQ .

It is also possible to change more than one of these quantities simultaneously. In digital communications, it is common practice to change both the amplitude and the phase angle to obtain higher data rates. It should be noted that once a carrier is modulated, it becomes a complete waveform containing more than one frequency components and therefore would require an appropriate channel that can carry all frequency components of this complex modulated signal. The signal occupies a BW and the channel must have sufficient BW.

BPSK uses one of the digital modulation techniques, i.e.., Phase Shift Keying (PSK). In this phase of the carrier varies according to binary inputs keeping amplitude and frequency constant. Carrier signal modulates according to spreaded binary data as shown below

$$S(t) = \begin{cases} A \sin(2\pi fct) & \text{for a binary 1} \\ -A \sin(2\pi fct) & \text{for a binary 0} \end{cases}$$

A "0" represent a 0 degree reference phase and "1" represents a carrier shift of 180°.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

IV.DESIGN OF CDMA RECEIVER:

In DS-CDMA receiver, the input to the system is the BPSK modulated signal. This signal would have been affected by noise and other interference in the communication channel. So, a filter is used to remove the Guassian noise and the extracted signal is thus demodulated used the Costas loop.The DS-SS CDMA receiver should be designed carefully to reproduce the data signal with least error.

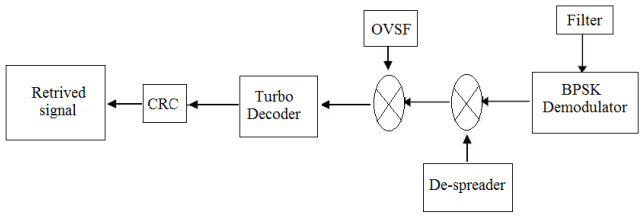


Figure 7: Block diagram of DS-CDMA receiver

The BPSK modulated input signal is multiplied by the locally generated carrier wave by the oscillator. The demodulated signal contains the message signal as well as the spreading code. The despreading of the message takes place exactly opposite to the spreading method. Here each n-bit is represented by its equivalent one bit of message. OVSF codes are used to despread the signal once again which provides orthogonality and also supports multi rate data applications.The decoder used is based on Viterbi algorithm. The Viterbi algorithm is based on maximum likelihood decoding technique. Using Viterbi algorithm,in high rate convolution codes, the probability of transitions is very high which gives rise to the large dynamic power dissipation.

To solve this problem, the number of transitions has to be reduced which can be done by reducing the number of states. This principle is the basis of T-Algorithm in which the least likely states are discarded; those states cannot participate in next cycle computations. To find the least likely states, this algorithm compares the difference between the state metric and the optimal path metric of every state with the threshold, states whose difference greater than the threshold are considered as the least likely states. The straight forward implementation of T-Algorithm requires three stages of 4-input comparator, one adder for branch metric computation, one 4-input comparator and one 2-input comparator for the calculation of best path metric from 8 incoming path metric.

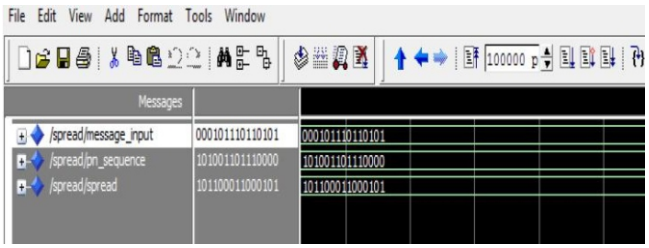
The output from the turbo decoder is divided by the polynomial, which is same as the one used at transmitter. If the remainder is zero it indicates that there is no transmission error else there is a transmission error.In this design, since transmitter and receiver uses common clock on the same FPGA board, the delay in the receiver is considered and modeled appropriately.

No specific synchronization technique is used. The multiplied output will have higher frequency components and channel noise as well. The high frequency components are eliminated using a suitable Low Pass Filter. The filtered low frequency component will have distortion in the signal. Hence a suitable 'Decision Device' is used to smoothen to binary sequence.

V.Simulation Results of All the modules:

A.Simulation waveform for Spreading Code:

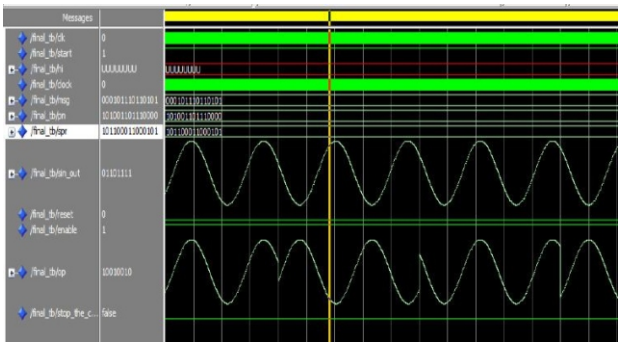
The below waveforms is obtained after spreading the message input. The XOR gate is used to spread the message input. The generated Gold code sequences and message inputs are given to XOR gate and the resulted output is spreader version of input message. I have taken message input as 000101110110101 and Gold Code sequence as 101001101110000. The Spreader device's output bits are obtained as 101100011000101.



B.Simulation waveform for BPSK Modulator:

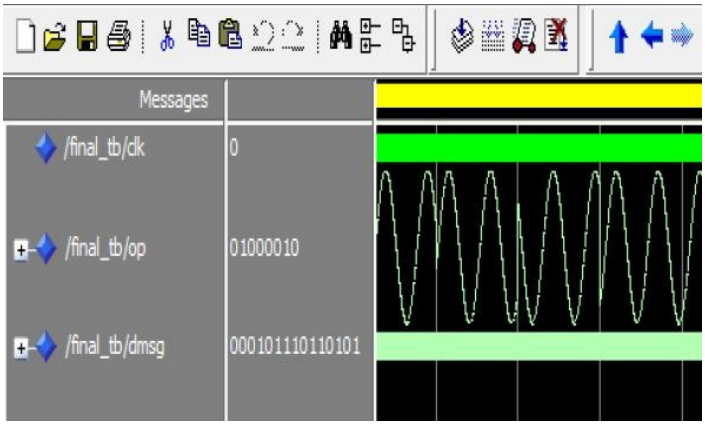
The BPSK modulator output is obtained as shown below. In the BPSK modulator, phase of the carrier is changed according to spreaded binary data bits, keeping amplitude and frequency constant. If spreader bit is 1 then sine wave is obtained else if spreader bit is 0 then phase shifted version of sine wave is obtained.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal



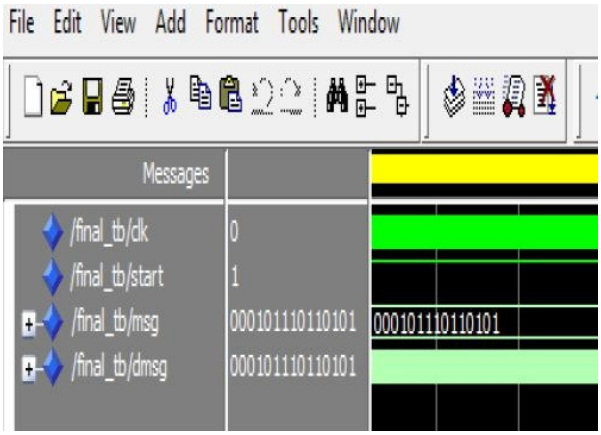
C.Simulation waveform for BPSK DeModulator:

The BPSK demodulator output is obtained as shown below. In this demodulator receives BPSK signal and compares this signal with local oscillator that is used at transmitter. After comparison if both received and carrier are in phase then it will be coded as 1 else, if both signals are out of phase then it will be coded as 0.



D.Comparison of transmitted and received data bit streams:

The comparison can be done between transmitted bits and received data bit streams as shown below. The comparison is done after receiving the entire transmitted signal so that received signal is demodulated completely. In the below figure yellow marker indicates the completion of demodulation. So at this instant comparison is done and obtained error free transmission and reception of message.



VI.CONCLUSION:

In this project, CDMA transmitter and receiver are designed using the turbo encoder instead of the convention practice of using Convolution Encoder. At the receiver section using the Viterbi algorithm with pipeline concept has tremendously improved the speed of the system. The power consumption for the existing work and the proposed work has also improved to a noticeable level. Also, this setup has been tested for any arbitrary chosen data stream, where these data has been transmitted through implemented transmitter and then received by implemented receiver. A comparison has been done between the transmitted and received data and satisfactory results have been achieved with least bit error rate. Increasing the number of bits using the same topology, it is possible to reach the standard rates specified for CDMA. Implementation of a CDMA communication system with DSSS technique in VHDL has the following advantages

•The design is fully reconfigurable
•The number of bits and Gold Code sequence can be changed very easily Useful for both FPGA and ASIC implementations

VII. FUTURE SCOPE:

This proposed project can be further extended to implement with multiple transmitters and receivers. It can be implemented with different modulation techniques like QPSK,PSK and a comparative analysis of the bit error rate can also be determined. Various advanced techniques can also be implemented to improve and reduce the multipath interference effect. The concept can be extended to design the Global Positioning System which is CDMA system. Frequency hopping spread spectrum technique can also be implemented and compared.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

VIII.REFERENCES:

[1]B.Sreedevi, V.Vijaya, CH.Kranthi Rekh,"FPGA implementation of DSSS-CDMA transmitter and receiver for adhoc networks", IEEE Symposium on computers and informatics 2011.

[2]M.K. Simon, D.Divsalar and D.Raphaehi "Improved parallel interference cancellation for CDMA", IEEE Trans.Commun..vol. 46 Feb 1998.

[3]Gold,R., "Optimal Binary Sequences for Spread Spectrum Multiplexing", IEEE Trans. Infor. Theory, Oct.,1967.

[4]R.Sarojini, Ch.Rambabu "Design & Implementation of DSSS-CDMA transmitter and Receiver for reconfigurable Links using FPGA", International Journal of Recent Technology and Engineering (IJRTE). ISSN: 2277-3878, Vol-1, Issue-3, August 2012.

[5]Bramha Swaroop Tripathi and Monika Kapoor"Review on DSSS-CDMA transmitter and receiver for ad hoc network using VHDL implementation", International Journal of Advances in Engineering & Technology,(IJAET) Jan. 2013

[6]Sanjay kumar Jaiswal, Kumkum verma, Dheeraj Jain, "Design of DS-CDMA transceiver using BPSK Modulation and Demodulation", World Applied Science Journal 16: 09-04-2012 ISSN 1818-4952.

[7]John G. Proakis and Masoud Salehi. "Communications Systems Engineering", 2nd edition Prentice Hall, Inc. Englewood Cliffs, New Jersey 1994, page 729-768.

[8]V.A.Chandrasetty, "VLSI Design: A practical Guide for FPGA and ASIC Implementation", Springer Briefs in Electrical and computer Engineering, DOI 10.1007/978-1-4614-1120-8_2.page 17-25.

[9]Jouko Vankka "Direct Digital Synthesizers: Theory, Design and Applications", November 2000 ISBN 951-22-5232-5 SSN 1455-8440 page 23-26.

[10]Timothy Ellis "The Implementation of a CDMA System on an FPGA-based Software Radio", University of Natal, December 2000, page 16-19.o