ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

A Three Phase Cascaded H-Bridge Multi Level Inverter fed Induction Motor Drive with Fewer Switches

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Abstract:

A new topology of cascaded multilevel converter is proposed. The proposed topology is based on a cascaded connection of single-phase sub multilevel converter units and full-bridge converters. Compared to the conventional multilevel converter, the number of dc voltage sources, switches, installation area, and converter cost is significantly reduced as the number of voltage steps increases. In order to calculate the magnitudes of the required dc voltage sources, three methods are proposed. Then, the structure of the proposed topology is optimized in order to utilize a minimum number of switches and dc voltage sources, and produce a high number of output voltage steps. The prior H-bridge based multilevel inverter can increase the number of output voltage levels by adding switch components and DC input voltage sources. If it employs seven switches and three DC sources, the number of output voltage levels becomes seven. Although its THD characteristics are improved. To mitigate this problem, we propose an efficient PWM switching method for the prior H-bridge based multilevel inverter. The operation and performance of the proposed a single-phase 31-level converter with multilevel converter is verified by MATLAB/ SIMULINK.

I. INTRODUCTION:

Over many years, Induction motor drives have been popularly used for variable speed control applications in industries. This is because the induction motor is simple in construction and requires less maintenance. In recent times, multilevel inverters (MLI) are gaining popularity and widely used for induction motor drive applications [1-3]. It is especially used for medium to high voltage and high current drive applications. There are many advantages of multilevel inverters as compared to conventional inverters.

Main advantages are low total harmonics distortion (THD), low switching losses, good power quality and reduced electromagnetic interference (EMI). Main feature of multilevel inverter is that it reduces voltage stress on each component [4-8]. The topologies of multilevel inverters are classified into three types. They are flying capacitor, diode clamped and H-bridge cascaded multilevel inverters. Cascaded H-bridge (CHB) multilevel inverter is one of the most popular inverter topology used in high-power medium voltage (MV) drives. It is composed of a multiple units of single-phase H-bridge power cells.

In practice, the number of power cells in a CHB inverter is mainly determined by its operating voltage and manufacturing cost. Cascaded H-bridge multilevel inverter requires the least number of components for the same voltage level as compared to all three types of inverter [9-11]. The growth of multilevel inverter caused development of various modulation schemes.The most common initial application of multilevel converters has been in traction, both in locomotives and track-side static converters. More recent applications have been for power system converters for VAR compensation and stability enhancement, active filtering, high-voltage motor drive, high-voltage dc transmission and most recently for medium voltage induction motor variable speed drives.

Many multilevel converter applications focus on industrial medium-voltage motor drives, utility interface for renewable energy systems, Flexible AC Transmission System (FACTS) and traction drive systems.In recent years, multilevel inverters have received more attention in industrial applications, such as motor drives, static VAR compensators and renewable energy systems. Compared to the traditional two-level voltage source inverters, the stepwise output voltage is the major advantage of multilevel inverters.

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II. PROPOSED TOPOLOGY:

In Fig.1, two new topologies are proposed for a seven-level inverter. As shown in. 1, the proposed topologies are obtained by adding two unidirectional power switches and one dc voltage source to the H-bridge inverter structure. In other words, the proposed inverters are comprised of six untidier tonal power switches (Sa, Sb, SL,1, SL,2, SR,1, and SR,2) an two dc voltage sources (VL,1 andVR,1). In this paper, these topologies are called developed H-bridge. As shown in Fig.1, the simultaneous turn-on of SL,1 and SL,2(orSR,1and SR,2).

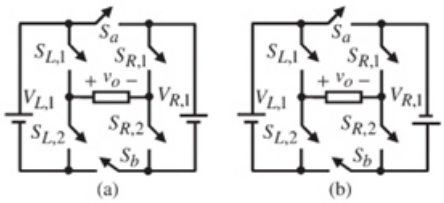

Fig.1.Proposed seven-level inverters. (a) First proposed topology. (b) Second Proposed topology.

TABLE I:OUTPUT VOLTAGES OF THE PROPOSED SEVEN-LEVEL INVERTERS

No.	$S_{L,1}$	$S_{L,2}$	$S_{R,1}$	$S_{R,2}$	S_a	S_b	v_o (Fig. 1(a))	v_o (Fig. 1(b))
1	1	0	0	1	0	1	$V_{L,1}$	$V_{L,1}$
2	1	0	0	1	1	0	$V_{R,1}$	$-V_{R,1}$
3	1	0	1	0	0	1	$V_{L,1}-V_{R,1}$	$V_{L,1}+V_{R,1}$
4	1	0	1	0	1	0	0	0
	0	1	0	1	0	1		
5	0	1	1	0	1	0	$-V_{L,1}$	$-V_{L,1}$
6	0	1	1	0	0	1	$-V_{R,1}$	$V_{R,1}$
7	0	1	0	1	1	0	$-(V_{L,1}-V_{R,1})$	$-(V_{L,1}+V_{R,1})$

Causes the voltage sources to short-circuit. Therefore, the simultaneous turn-on of the mentioned switches must be avoided. In addition, Sa and Sb should not turn on, simultaneously. The difference in the topologies illustrated in Fig.1 is in the connection of the dc voltage sources polarity. Table I shows the output voltages of the proposed inverters for different states of the switches. In this table, 1 and 0 indicate the ON- and OFF-states of the switches, respectively. As it is obvious from Table I, if the values of the dc voltage sources are equal, the number of voltage levels decreases to three. Therefore, the values of dc voltage sources should be different to generate more voltage levels without increasing the number of switches and dc voltage sources. Considering Table I, to generate all voltage levels (odd and even) in the proposed topology shown in Fig.1(a), the magnitudes of VL,1 and VR,1 should be considered 3puand 1pu, respectively. Similarly, for the topology shown in Fig.1 (a), the magnitudes of VL, 1and-VR, 1 should be considered 2pu and 1pu, respectively. Considering the aforementioned explanations, the total cost of the proposed topology in Fig.1(b) is low because dc voltage sources with low magnitudes are needed. By developing the seven-level inverter shown in Fig.1 (b), the 31-level inverter shown in Fig.2 can be proposed. This topology consists of ten unidirectional power switches and four dc voltage sources. According to Fig. 2, if the power switches of (SL,1,SL,2), (SL,3,SL,4), (SR,1,SR,2), and (SR,3,SR,4)turn on simultaneously, the dc voltage sources of VL,1, VL,2, VR,1, and VR,2 will be short-circuited, respectively. Therefore, the simultaneous turn-on of these switches should be avoided. In addition, Sa and Sb should not turn on simultaneously. It is important to note that the 31-level topology can be provided through the structure presented in Fig.1(a), where the only difference will be in the polarity of the applied dc voltage sources. By developing the proposed 31-level inverter. This topology

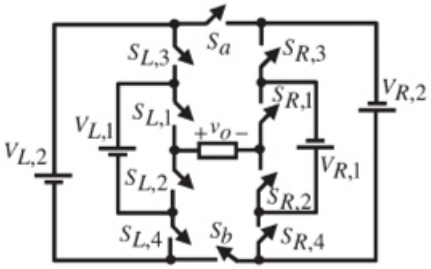

Fig.2. Proposed 31-level inverter.

$$N_{\text{step}} = 2^{2n+1} - 1 \quad (1)$$

$$N_{\text{switch}} = 4n + 2 \quad (2)$$

$$N_{\text{source}} = 2n \quad (3)$$

$$V_{o,\max} = V_{L,n} + V_{R,n}. \quad (4)$$

The other important parameters of the total cost of a multilevel inverter for evaluation are the variety of the values of dc voltage sources and the value of the blocking voltage of the switches. As the variety of dc voltage sources and the value of the blocking voltage of the switches are low, the inverter's total cost decreases [20]. The number of variety of the values of dc voltage sources (Variety) is given by

$$N_{\text{variety}} = 2n. \quad (5)$$

The following pattern is utilized to calculate the maximum magnitude of the blocking voltage of the power switches. As shown in Fig.1 (b), the blocking voltage of SR, 1and SR,2 are calculated as follows:

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
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$$V_{SR,1} = V_{SR,2} = V_{R,1} \quad (6)$$

WhereVSR,1 andVSR,2 indicate the maximum blocking voltages ofSR,1andSR,2, respectively. The blocking voltage of SL, 1andSL, 2are as follows

$$V_{SL,1} = V_{SL,2} = V_{L,1} \quad (7)$$

WhereVSL, 1andVSL, 2indicate the maximum blocking voltages of SL, 1andSL,2, respectively. Therefore, the maximum blocking voltage of all switches in the proposed seven-level inverter (Vblock,1)is calculated as follows

$$V_{block,1} = V_{SR,1} + V_{SR,2} + V_{SL,1} + V_{SL,2} + V_{Sa} + V_{Sa} = 4(V_{R,1} + V_{L,1}). \quad (8)$$

Considering Fig.2, the maximum blocking voltage of the switches is as follows

$$V_{SR,1} = V_{SR,2} = V_{R,1} \quad (9)$$

$$V_{SR,3} = V_{SR,4} = V_{R,2} - V_{R,1} \quad (10)$$

$$V_{SL,1} = V_{SL,2} = V_{L,1} \quad (11)$$

$$V_{SL,3} = V_{SL,4} = V_{L,2} - V_{L,1} \quad (12)$$

$$V_{Sa} = V_{Sb} = V_{R,2} + V_{L,2}. \quad (13)$$

Therefore, the maximum blocking voltage of all switches of the proposed 31-level inverter (Vblock, 2) is as follows

$$V_{block,2} = V_{SR,1} + V_{SR,2} + V_{SR,3} + V_{SR,4} + V_{SL,1} + V_{SL,2} + V_{SL,3} + V_{SL,4} + V_{Sa} + V_{Sb} = 4(V_{R,2} + V_{L,2}). \quad (14)$$

Similarly, the maximum blocking voltage of all switches of the 127-level inverter is calculated as follow

$$V_{block,3} = 4(V_{R,3} + V_{L,3}). \quad (15)$$

Finally, the maximum blocking voltage of all the switches of the general topology (Vblock, n) is calculated as follows:

$$V_{block,n} = 4(V_{R,n} + V_{L,n}). \quad (16)$$

III. PERFORMANCE OF THE INDUCTION MOTOR:

The sinusoidally-distributed flux density wave produced by the stator magnetizing currents sweeps past the rotor conductors, it generates a voltage in them.

The result is a sinusoidally-distributed set of currents in the short-circuited rotor bars. Because of the low resistance of these shorted bars, only a small relative angular velocity, r, between the angular velocity, s, of the flux wave and the mechanical angular velocity of the two-pole rotor is required to produce the necessary rotor current. The relative angular velocity, r, is called the slip velocity. The interaction of the sinusoidally-distributed air gap flux density and induced rotor currents produces a torque on the rotor. The typical induction motor speed-torque characteristic is shown in Figure.

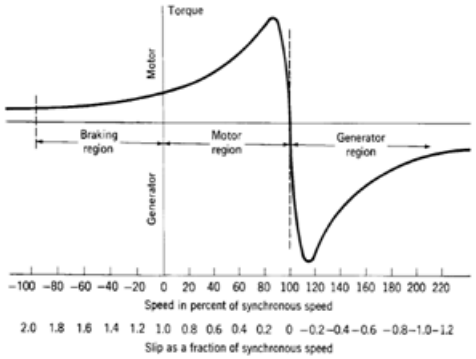

Fig.3, speed-torque characteristics of induction motor. An induction motor (IM) is a type of asynchronous AC motor where power is supplied to the rotating device by means of electromagnetic induction. An electric motor convert's electrical power to mechanical power in its rotor. There are several ways to supply power to the rotor. In a DC motor this power is supplied to the armature directly from a DC source, while in an induction motor this power is induced in the rotating device.

An induction motor is sometimes called a rotating transformer because the stator (stationary part) is essentially the primary side of the transformer and the rotor (rotating part) is the secondary side. Induction motors are widely used, especially poly phase induction motors, which are frequently used in industrial drives. When induction motors are given supply,

$$I_a = (Ea-Eb)/Ra \quad \text{As initially } E_b = 0$$

Motor draws a very high current initially; due to which voltage dip will forms, which show the effect on the power system network. In order to avoid such problems a effective controlled APF is placed without effecting the power quality or the motor performance characteristics.

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IV.MATLAB/SIMULINK RESULTS:

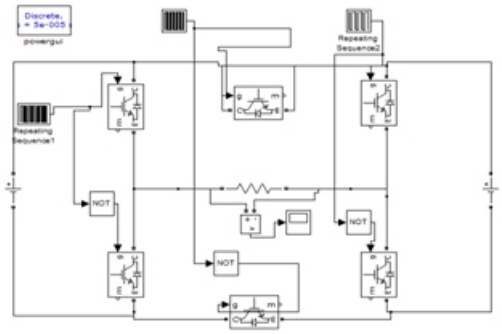

Fig.4.simulink circuit for 7 level inverter

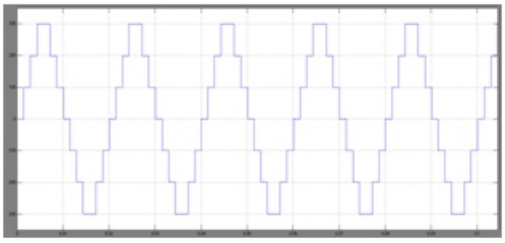

Fig.5.Simulation results for 7 level inverter

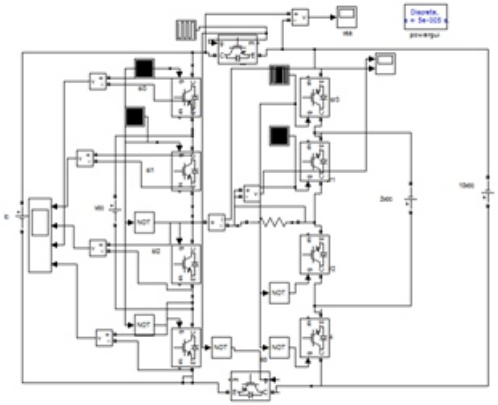

Fig.6.Simulation results for 31 level inverter

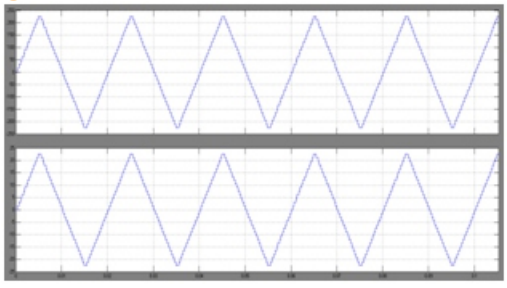

Fig.7.Simulation results voltage and current for 31 level inverter

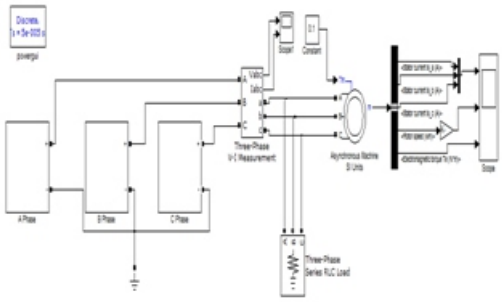

Fig.8. Simulink circuit induction motor fed 31 level inverter

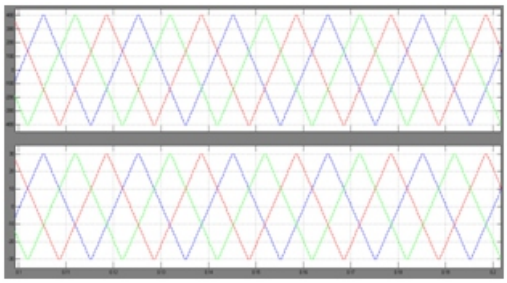

Fig.9.Simulation results for three phase voltage and current

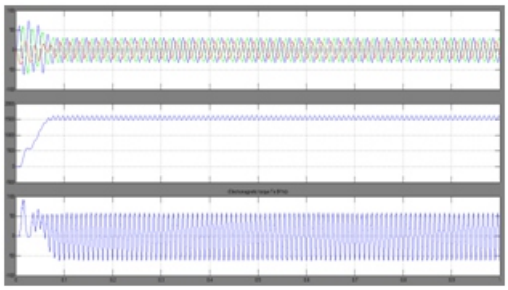

Fig.10. Simulation results for motor characteristics

IV.CONCLUSION:

In this paper, two basic topologies have been proposed for multilevel inverters to generate seven voltage levels at the output. The basic topologies can be developed to any number of levels at the output where the 31-level and general topologies are consequently presented. In addition, a new algorithm to determine the magnitude of the dc voltage sources has-been proposed. The proposed general topology was compared with the different kinds of presented topologies in literature from different points of view. According to the comparison re salts, the proposed topology requires a lesser number of IGBTs, power diodes, driver circuits, and dc voltage sources. Moreover, the magnitude of the blocking voltage of the switches is lower than that of conventional topologies. However, the proposed topology has a higher number of varieties of dc voltage sources in comparison with the others.

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International Journal & Magazine of Engineering, Technology, Management and Research
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The proposed topology was verified through the matlab/ Simulink platform for 31-level inverter with induction motor drive.

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