Main advantages are low total harmonics distortion (THD), low switching losses, good power quality and reduced electromagnetic interference (EMI). Main feature of multilevel inverter is that it reduces voltage stress on each component [4-8]. The topologies of multilevel inverters are classified into three types. They are flying capacitor, diode clamped and H-bridge cascaded multilevel inverters. Cascaded H-bridge (CHB) multilevel inverter is one of the most popular inverter topology used in high-power medium voltage (MV) drives. It is composed of a multiple units of single-phase H-bridge power cells.

In practice, the number of power cells in a CHB inverter is mainly determined by its operating voltage and manufacturing cost. Cascaded H-bridge multilevel inverter requires the least number of components for the same voltage level as compared to all three types of inverters [9-11]. The growth of multilevel inverter caused development of various modulation schemes. The most common initial application of multilevel converters has been in traction, both in locomotives and track-side static converters. More recent applications have been for power system converters for VAR compensation and stability enhancement, active filtering, high-voltage motor drive, high-voltage dc transmission and most recently for medium voltage induction motor variable speed drives.

Many multilevel converter applications focus on industrial medium-voltage motor drives, utility interface for renewable energy systems, Flexible AC Transmission System (FACTS) and traction drive systems. In recent years, multilevel inverters have received more attention in industrial applications, such as motor drives, static VAR compensators and renewable energy systems. Compared to the traditional two-level voltage source inverters, the stepwise output voltage is the major advantage of multilevel inverters.
II. PROPOSED TOPOLOGY:

In Fig.1, two new topologies are proposed for a seven-level inverter. As shown in Fig.1, the proposed topologies are obtained by adding two unidirectional power switches and one dc voltage source to the H-bridge inverter structure. In other words, the proposed inverters are comprised of six untidiest power switches (Sa, Sb, SL,1, SL,2, SR,1, and SR,2) and two dc voltage sources (VL,1 and VR,1). In this paper, these topologies are called developed H-bridge. As shown in Fig.1, the simultaneous turn-on of SL,1 and SL,2(or SR,1 and SR,2).

![Fig.1: Proposed seven-level inverters. (a) First proposed topology. (b) Second proposed topology.](image)

TABLE I: OUTPUT VOLTAGES OF THE PROPOSED SEVEN-LEVEL INVERTERS

<table>
<thead>
<tr>
<th>No.</th>
<th>SL,1</th>
<th>VL,1</th>
<th>SL,2</th>
<th>VL,2</th>
<th>SR,1</th>
<th>VR,1</th>
<th>SR,2</th>
<th>VR,2</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
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<tr>
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<td>0</td>
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<td>0</td>
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</tr>
<tr>
<td>3</td>
<td>1</td>
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<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Causes the voltage sources to short-circuit. Therefore, the simultaneous turn-on of the mentioned switches must be avoided. In addition, Sa and Sb should not turn on simultaneously. The difference in the topologies illustrated in Fig.1 is in the connection of the dc voltage sources polarity. Table I shows the output voltages of the proposed inverters for different states of the switches. In this table, 1 and 0 indicate the ON- and OFF-states of the switches, respectively. As it is obvious from Table I, if the values of the dc voltage sources are equal, the number of voltage levels decreases to three. Therefore, the values of dc voltage sources should be different to generate more voltage levels without increasing the number of switches and dc voltage sources. Considering Table I, to generate all voltage levels (odd and even) in the proposed topology shown in Fig.1(a), the magnitudes of VL,1 and VR,1 should be considered 3pu and 1pu, respectively. Similarly, for the topology shown in Fig.1 (a), the magnitudes of VL,1 and VR,1 should be considered 2pu and 1pu, respectively. Considering the aforementioned explanations, the total cost of the proposed topology in Fig.1(b) is low because dc voltage sources with low magnitudes are needed. By developing the seven-level inverter shown in Fig.1 (b), the 31-level inverter shown in Fig.2 can be proposed. This topology consists of ten unidirectional power switches and four dc voltage sources. According to Fig.2, if the power switches of (SL,1,SL,2), (SL,3,SL,4), (SR,1,SR,2), and (SR,3,SR,4) turn on simultaneously, the dc voltage sources of VL,1, VL,2, VR,1, and VR,2 will be short-circuit, respectively. Therefore, the simultaneous turn-on of these switches should be avoided. In addition, Sa and Sb should not turn on simultaneously. It is important to note that the 31-level topology can be provided through the structure presented in Fig.1(a), where the only difference will be in the polarity of the applied dc voltage sources. By developing the proposed 31-level inverter. This topology

![Fig.2: Proposed 31-level inverter.](image)

\[ N_{\text{step}} = 2^{n+1} - 1 \]  
\[ N_{\text{switch}} = 4n + 2 \]  
\[ N_{\text{source}} = 2n \]  
\[ V_{o,\text{max}} = V_{L,n} + V_{R,n}. \]  

The other important parameters of the total cost of a multilevel inverter for evaluation are the variety of the values of dc voltage sources and the value of the blocking voltage of the switches. As the variety of dc voltage sources and the value of the blocking voltage of the switches are low, the inverter’s total cost decreases [20]. The number of variety of the values of dc voltage sources (Variety) is given by

\[ N_{\text{variety}} = 2n. \]

The following pattern is utilized to calculate the maximum magnitude of the blocking voltage of the power switches. As shown in Fig.1 (b), the blocking voltage of SR,1 and SR,2 are calculated as follows:
\[ V_{SR,1} = V_{SR,2} = V_{R,1} \]  
(6)

Where \( V_{SR,1} \) and \( V_{SR,2} \) indicate the maximum blocking voltages of \( SR_1 \) and \( SR_2 \), respectively. The blocking voltage of \( SL_1 \) and \( SL_2 \) are as follows

\[ V_{SL,1} = V_{SL,2} = V_{L,1} \]  
(7)

Where \( V_{SL_1} \) and \( V_{SL_2} \) indicate the maximum blocking voltages of \( SL_1 \) and \( SL_2 \), respectively. Therefore, the maximum blocking voltage of all switches in the proposed seven-level inverter (Vblock, 1) is calculated as follows

\[ V_{\text{block,1}} = V_{SR,1} + V_{SR,2} + V_{SL,1} + V_{SL,2} + V_{Sa} + V_{Sb} = 4(V_{R,1} + V_{L,1}). \]  
(8)

Considering Fig. 2, the maximum blocking voltage of the switches is as follows

\[ V_{SR,1} = V_{SR,2} = V_{R,1} \]  
(9)

\[ V_{SR,3} = V_{SR,4} = V_{R,2} - V_{R,1} \]  
(10)

\[ V_{SL,1} = V_{SL,2} = V_{L,1} \]  
(11)

\[ V_{SL,3} = V_{SL,4} = V_{L,2} - V_{L,1} \]  
(12)

\[ V_{Sa} = V_{Sb} = V_{R,2} + V_{L,2}. \]  
(13)

Therefore, the maximum blocking voltage of all switches of the proposed 31-level inverter (Vblock, 2) is as follows

\[ V_{\text{block,2}} = V_{SR,1} + V_{SR,2} + V_{SR,3} + V_{SR,4} + V_{SL,1} + V_{SL,2} + V_{SL,3} + V_{SL,4} + V_{Sa} + V_{Sb} = 4(V_{R,2} + V_{L,2}). \]  
(14)

Similarly, the maximum blocking voltage of all switches of the 127-level inverter is calculated as follows

\[ V_{\text{block,3}} = 4(V_{R,3} + V_{L,3}). \]  
(15)

Finally, the maximum blocking voltage of all the switches of the general topology (Vblock, n) is calculated as follows:

\[ V_{\text{block,n}} = 4(V_{R,n} + V_{L,n}). \]  
(16)

III. PERFORMANCE OF THE INDUCTION MOTOR:

The sinusoidally-distributed flux density wave produced by the stator magnetizing currents sweeps past the rotor conductors, it generates a voltage in them.

\[ V_{SR,1} = V_{SR,2} = V_{R,1} \]  
(6)

Where \( V_{SR,1} \) and \( V_{SR,2} \) indicate the maximum blocking voltages of \( SR_1 \) and \( SR_2 \), respectively. The blocking voltage of \( SL_1 \) and \( SL_2 \) are as follows

\[ V_{SL,1} = V_{SL,2} = V_{L,1} \]  
(7)

Where \( V_{SL_1} \) and \( V_{SL_2} \) indicate the maximum blocking voltages of \( SL_1 \) and \( SL_2 \), respectively. Therefore, the maximum blocking voltage of all switches in the proposed seven-level inverter (Vblock, 1) is calculated as follows

\[ V_{\text{block,1}} = V_{SR,1} + V_{SR,2} + V_{SL,1} + V_{SL,2} + V_{Sa} + V_{Sb} = 4(V_{R,1} + V_{L,1}). \]  
(8)

Considering Fig. 2, the maximum blocking voltage of the switches is as follows

\[ V_{SR,1} = V_{SR,2} = V_{R,1} \]  
(9)

\[ V_{SR,3} = V_{SR,4} = V_{R,2} - V_{R,1} \]  
(10)

\[ V_{SL,1} = V_{SL,2} = V_{L,1} \]  
(11)

\[ V_{SL,3} = V_{SL,4} = V_{L,2} - V_{L,1} \]  
(12)

\[ V_{Sa} = V_{Sb} = V_{R,2} + V_{L,2}. \]  
(13)

Therefore, the maximum blocking voltage of all switches of the proposed 31-level inverter (Vblock, 2) is as follows

\[ V_{\text{block,2}} = V_{SR,1} + V_{SR,2} + V_{SR,3} + V_{SR,4} + V_{SL,1} + V_{SL,2} + V_{SL,3} + V_{SL,4} + V_{Sa} + V_{Sb} = 4(V_{R,2} + V_{L,2}). \]  
(14)

Similarly, the maximum blocking voltage of all switches of the 127-level inverter is calculated as follows

\[ V_{\text{block,3}} = 4(V_{R,3} + V_{L,3}). \]  
(15)

Finally, the maximum blocking voltage of all the switches of the general topology (Vblock, n) is calculated as follows:

\[ V_{\text{block,n}} = 4(V_{R,n} + V_{L,n}). \]  
(16)
IV. MATLAB/SIMULINK RESULTS:

Fig. 4. Simulink circuit for 7 level inverter

Fig. 5. Simulation results for 7 level inverter

Fig. 6. Simulation results for 31 level inverter

Fig. 7. Simulation results voltage and current for 31 level inverter

Fig. 8. Simulink circuit induction motor fed 31 level inverter

Fig. 9. Simulation results for three phase voltage and current

Fig. 10. Simulation results for motor characteristics

IV. CONCLUSION:

In this paper, two basic topologies have been proposed for multilevel inverters to generate seven voltage levels at the output. The basic topologies can be developed to any number of levels at the output where the 31-level and general topologies are consequently presented. In addition, a new algorithm to determine the magnitude of the dc voltage sources has been proposed. The proposed general topology was compared with the different kinds of presented topologies in literature from different points of view. According to the comparison results, the proposed topology requires a lesser number of IGBTs, power diodes, driver circuits, and dc voltage sources. Moreover, the magnitude of the blocking voltage of the switches is lower than that of conventional topologies. However, the proposed topology has a higher number of varieties of dc voltage sources in comparison with the others.
The proposed topology was verified through the matlab/ Simulink platform for 31-level inverter with induction motor drive.

REFERENCES:


