ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

BIST Architecture for Testing UART Synchronization on FPGA

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Abstract:
Testing of VLSI chips is changing into significantly complicated day by day as a result of increasing exponential advancement of NANO technology. BIST may be a style technique that enables a system to check mechanically itself with slightly larger system size. During this paper, the simulation result performance achieved by BIST enabled UART design through VHDL programming is enough to compensate the additional hardware required in BIST design. This system generate random check pattern exploitation the LFSR checks this mechanism also to be used to check the design chip itself. So the main advantage of this testing is that it reduces the complexness thereby will increase the operational speed, potency in conjunction with relevant price reduction. Also in this method the conjunction with operation, maintenance of the system is verified using Spartan 3A kit.

Keywords: - BIST Architecture, UART Tx, UART Rx, LFSR, VLSI testing.

I. INTRODUCTION

Testing of integrated circuits (ICs) is of crucial importance to confirm a high level of quality in product practicality in each commercially and in camera made merchandise. The impact of testing affects areas of producing also as those concerned in style. This want to realize a top quality level should be tempered with the value and time concerned during this method. In VLSI we've testing issues like input combinatorial issues, gate to I/O pin magnitude relation issues, take a look at generation issues, light-emitting diode the designer to spot reliable.

Take a look at ways and solve this issues.teh insertion of special take a look at electronic equipment on the VLSI circuits that enables economical take a look at ways. This has been self-addressed by the requirement for style for testability (DFT) and thus the requirement for BIST. It tests the circuit or system performs itself thus it's named as “self-test". BIST is AN on-chip take a look at logic that's utilized to check the useful logic of a chip, by it. Thanks to the speedy increase within the style quality, BIST has become a serious style thought in DFT ways and is changing into progressively vital in today’s state of the art SoCs. A properly designed BIST is in a position to offset the value of additional take a look at hardware whereas at identical time making certain the dependability, reduces maintenance value and testability.

In parallel communication the value still as quality of the system will increase because of concurrent transmission of data bits on multiple wires. Serial communication alleviates this downside and emerges as effective technique in several applications for long distance communication because it reduces the signal distortion attributable to its straightforward structure. Universal Asynchronous Receiver Transmitter (UART) may be a kind of serial communication protocol. The Universal Asynchronous Receiver Transmitter (UART) may be a fashionable and widely-used device for digital communication within the field of telecommunication. Its several blessings like simple resources, reliable performance, robust anti jamming capability, straightforward to work and notice so on The UART may be a giant scale computer circuit that contains all the software system programming

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necessary to completely control the port of a laptop (Personnel computer).

UART performs parallel-to-serial conversion on information character received from the host processor into serial information stream, and serial-to-parallel conversion on serial information bits received from serial device to the host processor. It additionally adds the start and stop bit to the info for synchronization. Additionally to the fundamental job of changing information from parallel to serial for transmission and from serial to parallel on reception, a UART can sometimes give extra circuits for signals that can be accustomed indicate the state of the transmission media and to manage the flow of information within the event that the remote device isn't ready to just accept additional information

II. BIST ARCHITECTURE

BIST architecture consists of a take a look at Pattern Generator (TPG), the circuit to be tested (CUT), some way to investigate the results (TRA), and some way to compress those results (BCU) and also LFSR for simplicity and handling. CUT could be designed as memory device architecture for testing the faults. The fault address can be detected and it could compare to the comparator for the analysis of the all relevant circuits

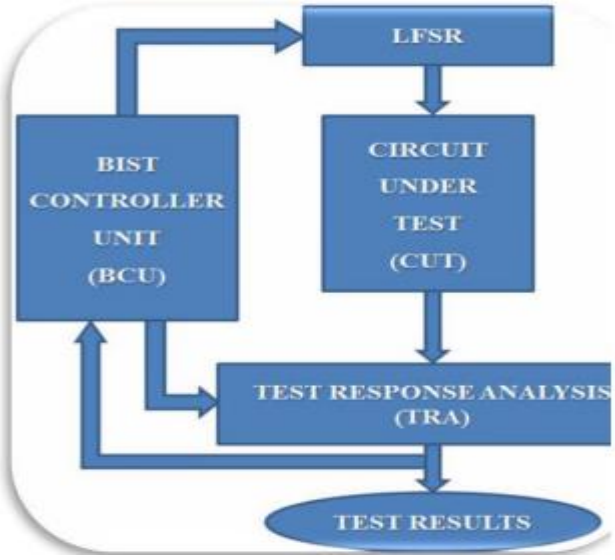

Figure 1: Block diagram of BIST architecture

The LFSR generates the feedback values from the each and every flip-flop for the new CUT architecture. The level of this recognition could be difficult to identify the fault and it could be having time consuming process. The process can be adoptable for the all authorized and the unauthorized data's. The BIST controller can be easily controlled as a device details for the novel architecture for the further details. The test response analysis could be considered for the UART transmitting and the receiving data's form the each bits. The test results can be detecting the fault address and then it consumes all the details as a database and identifies the fault address and shows the details. This could be as a process of simulation level waveform.

III. UART ARCHITECTURE

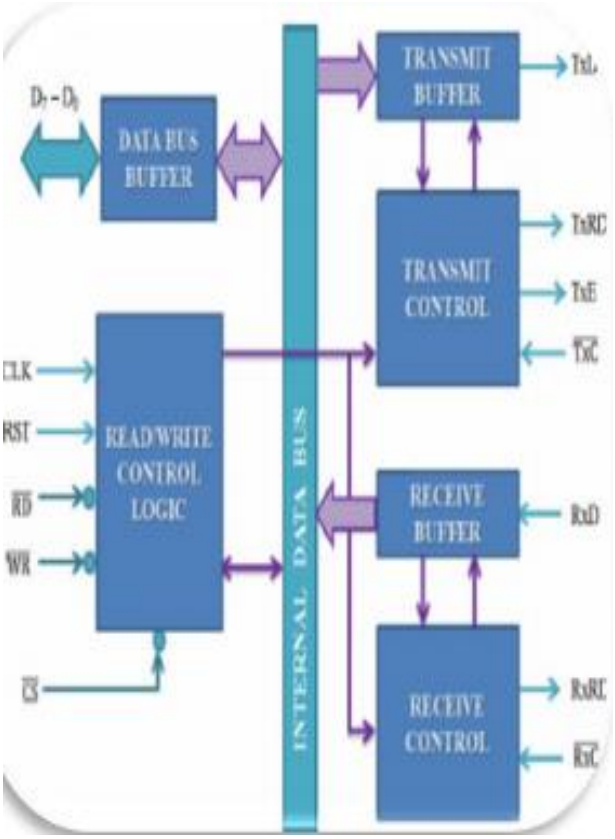

Figure 2: Block diagram of UART Architecture

The UART architecture contains the transmitter and the receiver. This could be contain and loads the buffer data for all the read and write operation. The data

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transfers through this serial communication to get the proper information about the outputs.

A. UART TRANSMITTER

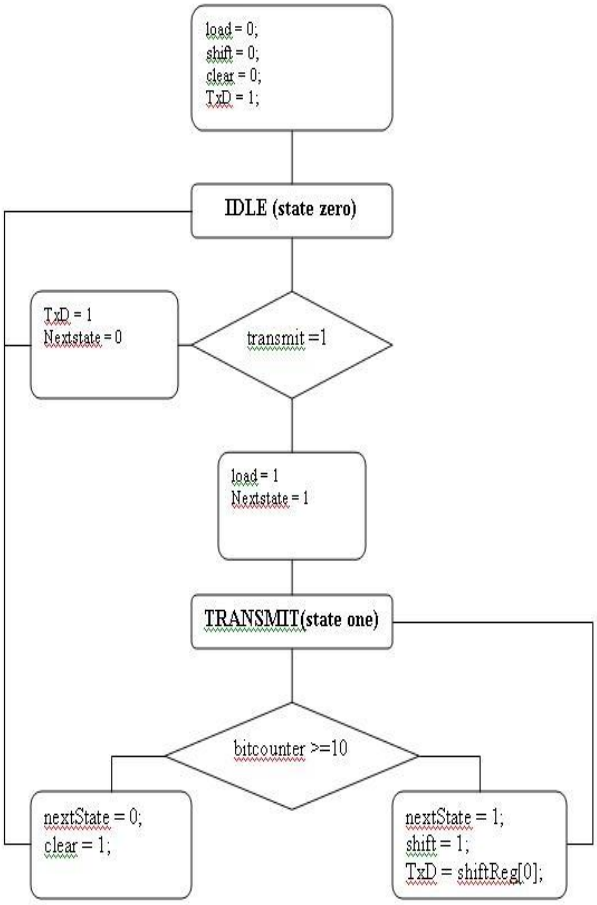

Figure 3: design flow of UART Transmitter

B. UART RECEIVER

The received serial information is out there on the RXIN pin. The received information is applied to the sampling logic block. The receiver temporal order and management is employed for synchronization of clock signal between transmitter and receiver. The receiver sampling is sixteen times thereto of the transmitter information measure rate. Within the design of UART receiver (fig. 7), initially the logic line (RxD) is highWhenever it goes low sampling and logic block can take four samples of that bit and if all four square measure same it indicates the start of a frame.

IV. Simulation Results

The UART BIST architecture simulation can be done through the Xilinx ISE using VERILOG HDL.

Fig 4.transmitter at initial state the above result when rst is on state the whole controls will be in initial state .when the rstos off and the transmit is in on state.rxd is always 1 when it does receive any data

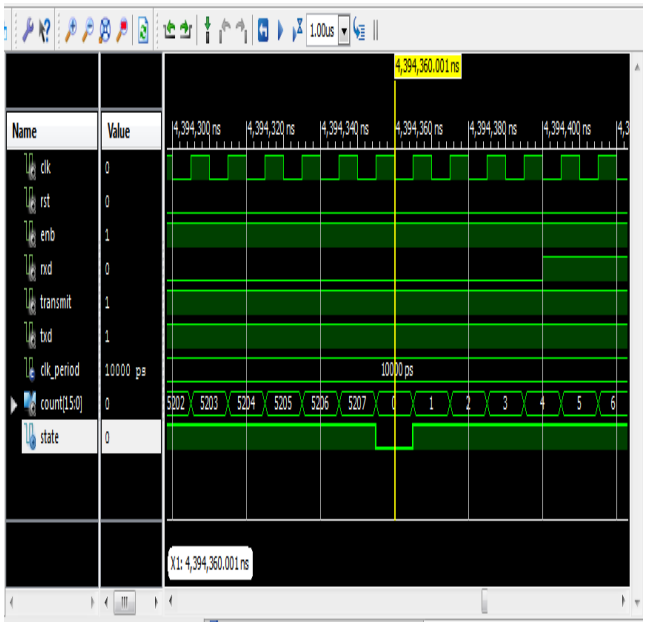

Fig 5 State for transmission at 5207 seconds

Count is the number of clock pulses to generate the baud rate for the 50 mhz transmitter

Conclusion

9600 baud rate uart has been designed in fpga with 50 mhzclock.uart is with successful transmission and reception is implemented. Art with 9 pin design is architecture is described in brief

REFERENCES

[1] Mohd Yamani IdnaIdris, MashkuriYaacob, Zaidi Razak, “A VHDL Implementation of UART Design with BIST capability”

[2] Dr. T.V.S.P. Gupta, Y. Kumari, M.AsokKumar”UART realization with BIST architecture using VHDL” International Journal of

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International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com Vol. 3, Issue 1, January -February 2013, pp.636-640

[3] M.S. Harvey,Generic UART Manual,SiliconValley,December 1999.

[4] P. J. Anderson , "The designer's guide to VHDL" , Morgan Kaufman , 2nd edition, 2002.

[5] Neil H.E. Weste, Kim Haase, David Harris , A. Banerjee , "CMOS VLSI Design: A circuits and Systems Perspective", Pearson Education.

[6] K. Zarrineh, and S. J. Upadhyaya, "On programmable memory built-in self test architectures", Design, Automation and Test in Europe Conference and Exhibition 1999. Proceedings , 1999, pp. 708 -713