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Performance Analysis of Dynamic Voltage Restorer for Mitigation of Voltage Sags and Swells under Non-Linear Load Conditions

Bommu Malyadri
M.Tech (Power Systems and Automation),
Department of Electrical Engineering,
Sir C.R.R. College of Engineering, Eluru, AP, India.

R.Madhusudan
Assistant Professor,
Department of Electrical Engineering,
Sir C.R.R. College of Engineering, Eluru, AP, India.

Abstract:

Power quality problems such as transients, sags, swells, and other distortions to the sinusoidal wave form of the supply voltage affect the performance of loads. There are different methods to compensation of voltage sag and swell, one of the most popular methods of sag and swell compensation is Dynamic Voltage Restorer (DVR), The Dynamic Voltage Restorer (DVR) is series-connected power electronics based device. In this paper the effectiveness of dynamic voltage restorer for voltage balancing is presented. This paper presents compensation of sags and swells voltage during single line to ground (SLG) and three-phase faults. Simulation results carried out by Matlab/Simulink verify the performance of the proposed method.

I. INTRODUCTION:

Electrical energy is the most efficient and popular form of energy and the modern society is heavily dependent on the electric supply. The life cannot be imagined without the supply of electricity. At the same time the quality and continuity of the electric power supplied is also very important for the efficient functioning of the end user equipment. Most of the commercial and industrial loads demand high quality uninterrupted power. Thus maintaining the qualitative power is of utmost important. The quality of the power is affected if there is any deviation in the voltage and frequency values at which the power is being supplied. This affects the performance and life time of the end user equipment. Whereas, the continuity of the power supplied is affected by the faults which occur in the power system.

So to maintain the continuity of the power being supplied, the faults should be cleared at a faster rate and for this the power system switchgear should be designed to operate without any time lag. The power quality is affected many problems which occur in transmission system and distribution system. Some of them are like- harmonics, transients, sudden switching operations, voltage fluctuations, frequency variations etc. These problems are also responsible in deteriorating the consumer appliances. In order to enhance the behavior of the power system, these all problems should be eliminated. With the recent advancements in power electronic devices, there are many possibilities to reduce these problems in the power system. One of them is the use of Flexible AC Transmission System (FACTS) devices. The connection of these devices in the power system helps in improving the power quality and reliability. In this project the mitigation of voltage sag using FACTS devices is studied and analyzed.

II. DYNAMIC VOLTAGE RESTORER:

Basic DVR Operating Principles:

The DVR functions by injecting three single phase AC voltages in series with the three phase incoming network voltages during sag, compensating for the difference between faulty and nominal voltages. All three phases of the injected voltages are of controllable amplitude and phase. Three pulse-width modulated (PWM) voltage source inverters (VSI) fed from a DC link supply the active and reactive power. During undisturbed power supply condition, the DVR operates in a low loss standby mode.

The necessary amount of energy that must be delivered by the energy source depends on load MVA requirement, control strategy applied, deepest sag to be protected. Under normal conditions, the short circuit impedance of the injection transformer determines the voltage drop across the DVR. This impedance must be low and has an impact on the fault current through the VSI on secondary side caused by a short circuit at load side.

- Maximum MVA-load and power factor,
- Maximum 1 phase and 3 phase voltage sags to be compensated,
- Maximum duration of 3 phase voltage sag,
- Maximum allowed voltage drop across DVR under steady-state conditions,
- Short circuit impedance of the injection transformers,
- Short circuit impedance and connection of step down transformers at the input and output sides of the DVR as well as the short circuit power.

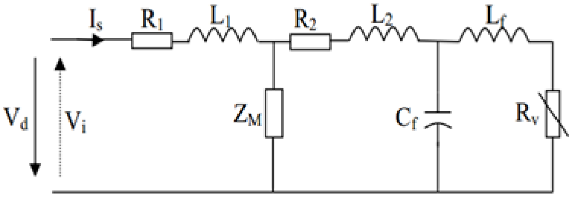

Figure 1: Equivalent Circuit of DVR with Inverter-Side Filter

In above Figure, R1 and L1 represent the primary-side resistance and leakage inductance of the transformer. R2 and L2 represent the secondary-side resistance and leakage inductance of the transformer referred to the primary-side. Lf and Cf constitute the filter elements and are also referred to the primary-side. Rv is a resistor to account for the total conduction voltage drop caused by the switches and diodes. ZM represents the magnetizing impedance of the transformer.

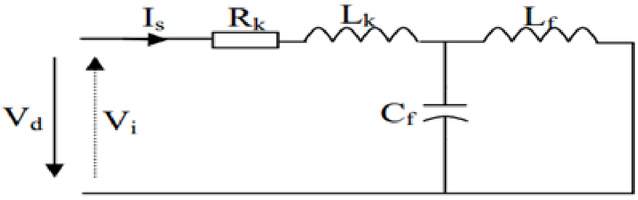

Figure 2: Simplified Equivalent Circuit of DVR with Inverter-Side Filter

Let Rk+jwLk represents the short-circuit impedance of the injection transformer where Rk=R1+R2, Lk=L1+L2.

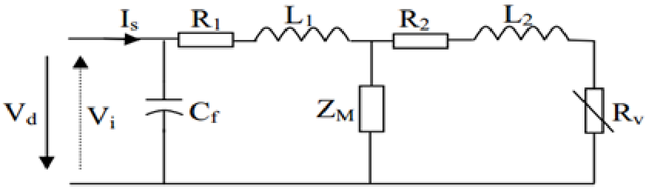

Figure 3: Equivalent Circuit of DVR with Line-Side Filter

Filter capacitance, Cf, is connected in shunt with the other structure of the DVR system; inclusion of it will not cause much voltage change of the power system. For simplicity, the effect of the capacitor can be neglected. Filtering Schemes In the design of DVR, special attentions must be paid to the filtering scheme as it is related with the system dynamic response. Two filtering schemes were seen from the recent literature, which are the inverter-side filter and line-side filter. In the scheme of inverter-side filter, a series inductor Lf and a shunt capacitor Cf are inserted between the transformer and switching devices. From the view point of harmonic elimination, the inverter-side filter scheme may be a preferable one.

Yet, as the insertion of the inductor may introduce an additional voltage-drop component across the series transformer, it is also found that the magnitude and phase difference between the fundamental components of voltage has appeared on both sides of the filter, implying that an inadvertent choice of the filter design would significantly downgrade the DVR control performance. As for the DVR design of line-side filter, it can be implemented by placing the filtering scheme on the line-side of the series transformer. In such a line-side filter scheme, the leakage flux of series transformer is served as the filtering inductance, and the capacitor is placed across the transformer winding.

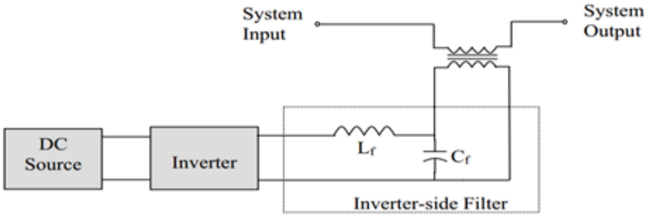

Figure4: Inverter-Side Filter

Line-Side Filter:

A typical DVR system can be analyzed using its equivalent circuit shown in below Figure. All the variables in Figure have been referred to the line side of injection transformer. In this figure Ri and Li denote the resistance and the leakage inductance of the injection transformer. In the analysis, it will be assumed that Ri and Li are known. Cf is the filter capacitor. Vse represents the equivalent source of the power system interfaced to the output of the filter with Ze = Re+jwLe being the equivalent impedance (at the frequency w) external to the DVR. Vsi represents the voltage on the inverter side of the filter. The functions of the other DVR components are not included in the analysis. Note that the capacitor Cf together with the equivalent impedance of the series injection transformer forms an LC filter which can be used to attenuate the harmonic contents appearing in the injection voltage

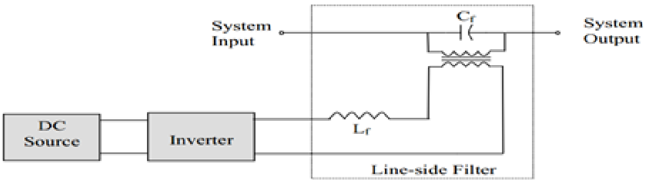

Figure 5: Line-Side Filter

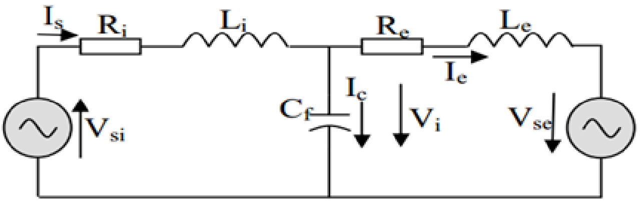

Figure 6: Line-Side Filter Equivalent Circuit

The basic principle behind the selection of the capacitor is to provide a shunt path for the harmonic current and let the series transformer carry almost all the harmonic voltages. To achieve this goal, the capacitor should be chosen to satisfy.

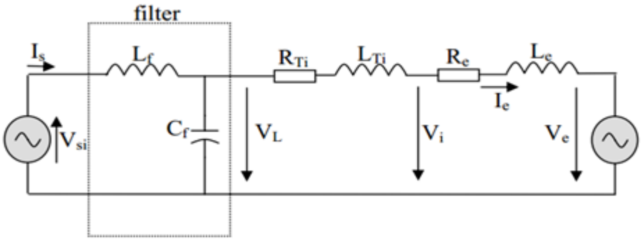

Figure 7: Inverter-Side Filter Equivalent Circuit

Proposed DVR:

The schematic of a DVR-connected system is shown in Fig 8(a). The voltage *V*inj is inserted such that the load voltage *V*load is constant in magnitude and is undistorted, although the supply voltage *V*sis not constant in magnitude or is distorted. Fig 8(b) shows the phasor diagram of different voltage injection schemes of the DVR. VL(pre−sag) is a voltage across the critical load prior to the voltage sag condition. During the voltage sag, the voltage is reduced to Vs with a phase lag angle of θ. Now, the DVR injects a voltage such that the load voltage magnitude is maintained at the pre-sag condition. According to the phase angle of the load voltage, the injection of voltage scan be realized in four ways. Vinj1 represents the voltage injected in-phase with the supply voltage. With the injection of Vinj2, the load voltage magnitude remains same but it leads Vs by a small angle.

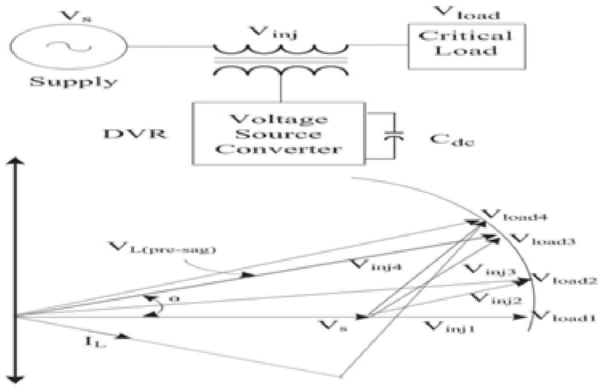

Fig. 8: (a) Basic circuit of DVR. (b) Phasor diagram of the DVR voltage injection schemes.

Fig. 9 shows a schematic of a three-phase DVR connected to restore the voltage of a three-phase critical load. A three-phase supply is connected to a critical and sensitive load through a three-phase series injection transformer. The equivalent voltage of the supply of phase Av Ma is connected to the point of common coupling (PCC) vSa through short-circuit impedance Zsa. The voltage injected by the DVR in phase AvCa is such that the load voltage vLa is of rated magnitude and undistorted. A three-phase DVR is connected to the line to inject a voltage in series using three single-phase transformers Tr. Lr and Crrepresent the filter components used to filter the ripples in the injected voltage. A three-leg VSC with insulated-gate bipolar transistors (IGBTs) is used as a DVR, and a BESS is connected to its dc bus.

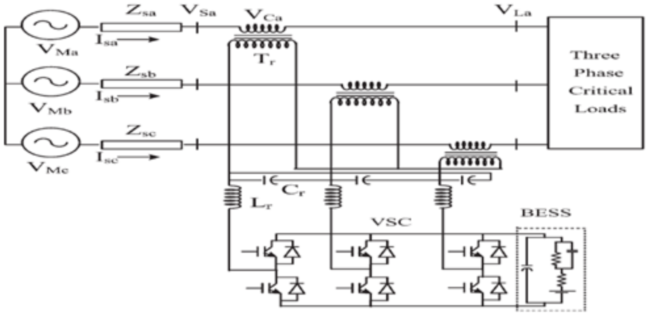

Fig. 9: Schematic of the DVR-connected system.

The magnitude of dc link current often changes in step (and sometimes its direction also changes) as the inverter switches are turned on and off. The step change in instantaneous dc link current occurs even if the ac load at the inverter output is drawing steady power. However, average magnitude of the dc link current remains positive if net power-flow is from dc bus to ac load. The net power-flow direction reverses if the ac load connected to the inverter is regenerating. Under regeneration, the mean magnitude of dc link current is negative.

BESS Component of Model:

In designing the BESS component of the model, I was determining the parameters that would most actively be manipulated to analyze the possible configurations of the energy storage at the PV site.

In setting up the parameters, I looked at what values were available to project managers to change during the design phase of the system, (such as the charge and discharge speed, which are related to battery chemistry), as well as the parameters that would be adjusted from month-to-month, week-to-week or day-to-day by the facility operator or utility coordinator. These parameters included the application that was being utilized by the system, and according to which application was being used the parameters would include items such as the steady-state charge level, the output leveling target, or a parameter such as the point of transition from off-peak to on-peak power for time-shifting purposes.

III. CONTROL of DVR:

The compensation for voltage sags using a DVR can be performed by injecting or absorbing the reactive power or the real power. When the injected voltage is in quadrature with the current at the fundamental frequency, the compensation is made by injecting reactive power and the DVR is with a self-supported dc bus. However, if the injected voltage is in phase with the current, DVR injects real power, and hence, a battery is required at the dc bus of the VSC.

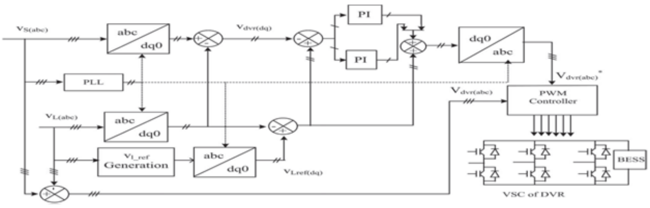

Fig. 10: Control block of the DVR that uses the SRF method of control.

The error between the reference and actual DVR voltages in the rotating reference frame is regulated using two proportional–integral (PI) controllers. The compensating strategy for compensation of voltage quality problems considers that the load terminal voltage should be of rated magnitude and undistorted.

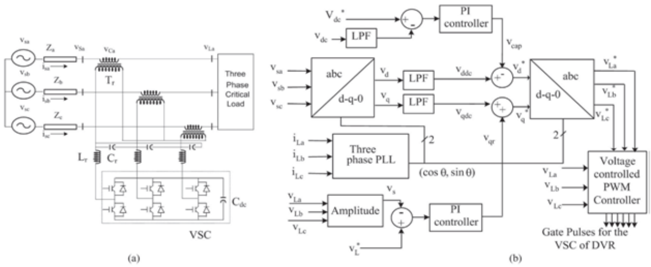

Fig 11: (a) Schematic of the self-supported DVR. (b) Control block of the DVR that uses the SRF method of control.

IV. SIMULATION RESULTS:

The DVR-connected system consisting of a three-phase supply, three-phase critical loads, and the series injection transformers shown in Fig. 11 is modeled in MATLAB/Simulink environment along with a sim power system toolbox and is shown in Fig. 12. An equivalent load considered is a 10-kVA0.8-pf lag linear load. The control algorithm for the DVR shown in Fig. 10 is also modeled in MATLAB. The reference DVR voltages are derived from sensed PCC voltages (vsa, vsb, vsc) and load voltages(vLa, vLb, vLc). A PWM controller is used over the referenceand sensed DVR voltages to generate the gating signals for the IGBTs of the VSC of the DVR. The capacitor-supported DVR shown in Fig. 4 is also modeled and simulated in MATLAB, and the performances of the systems are compared in three conditions of the DVR.

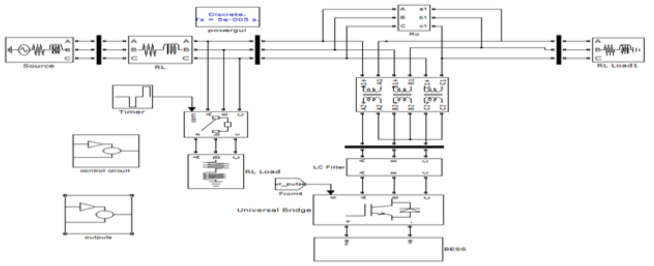

Fig 12: MATLAB-based model of the BESS-supported DVR-connected system

The performance of the DVR is demonstrated for different supply voltage disturbances such as voltage sag and swell. Fig. 13show the transient performance of the system under voltage sag and voltage swell conditions.

At 0.2 s, a sag in supply voltage is created for five cycles, and at 0.4 s, a swell in the supply voltages is created for five cycles. It is observed that the load voltage is regulated to constant amplitude under both sag and swell conditions. PCC voltages vS, load voltages vL, DVR voltages vC, amplitude of load voltage VL and PCC voltage Vs, source currents iS, reference load voltages vLref ,and dc bus voltage vdc are also depicted in Fig. 6.

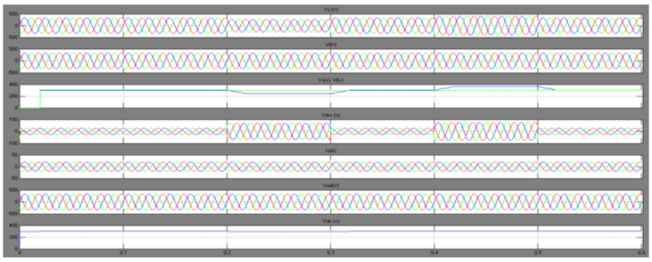

Fig 13: Dynamic performance of DVR with in-phase injection during voltage sag and swell applied to critical load.

The load and PCC voltages of phase A are shown in Fig. 14, which shows the in-phase injection of voltage by the DVR. The compensation of harmonics in the supply voltages is demonstrated in Fig. 15.

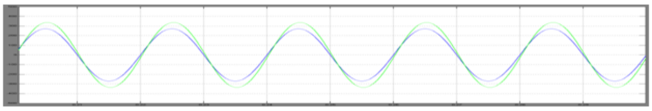

Fig 14: Voltages at the PCC and load terminals

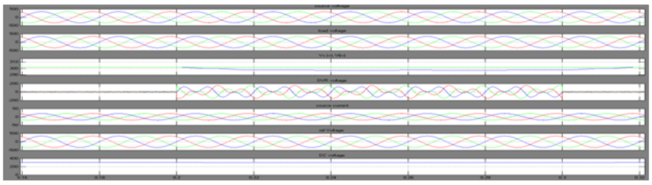

Fig 15: Dynamic performance of DVR during harmonics in supply voltage applied to critical load

At 0.2 s, the supply voltage is distorted and continued for five cycles. The load voltage is maintained sinusoidal by injecting proper compensation voltage by the DVR. The total harmonics distortions (THDs) of the voltage at the PCC, supply current, and load voltage are shown in Figs. 16–11, respectively.

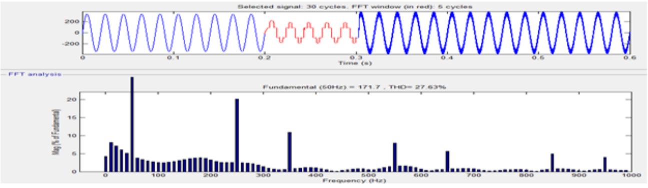

Fig 16: PCC voltage and harmonic spectrum during the disturbance

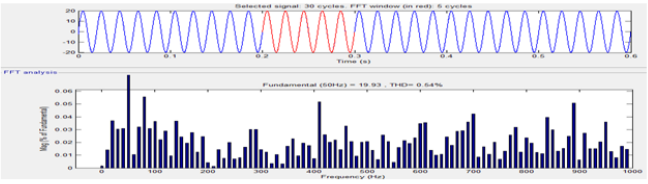

Fig 17: Supply current and harmonic spectrum during the disturbance

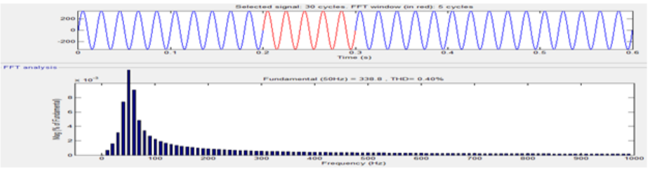

Fig 18: Load voltage and harmonic spectrum during the disturbance

It is observed that the load voltage THD is reduced to a level of0.66% from the PCC voltage of 6.34%.The magnitudes of the voltage injected by the DVR for mitigating the same kinds of sag in the supply with different angles of injection are observed. The injected voltage, series current, and kilovolt ampere ratings of the DVR for the four injection schemes are given in Table I. In Scheme-1 in Table I, the in-phase injected voltage is Vinj1 in the phas or diagram in Fig. 8. In Scheme-2, a DVR voltage is injection at a small angle of 30◦, and in Scheme-3, the DVR voltage is injected at an angle of 45◦.

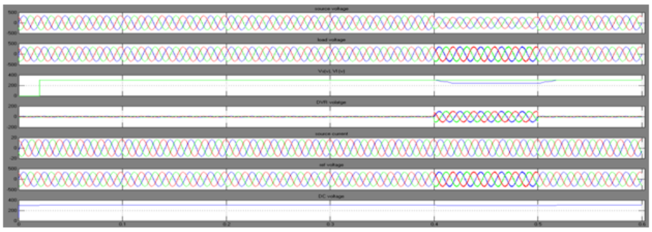

Fig 19: Dynamic performance of the capacitor-supported DVR during voltage sag

The injection of voltage in quadrature with the line current is in Scheme-4. The required rating of compensation of the same using Scheme-1 is much less than that of Scheme-4.

DVR with Non-Linear Load and Three-Phase fault

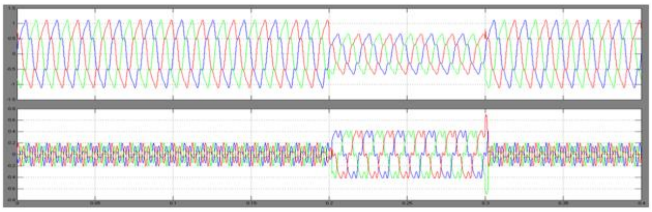

Fig 20: input voltage and DVR voltage during three-phase fault

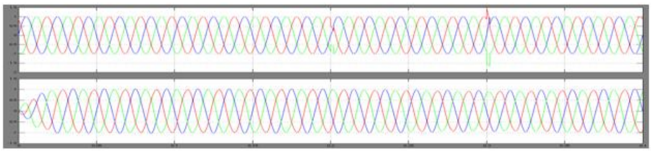

Fig 21: Load voltage and load current during three-phase fault under non-linear load condition

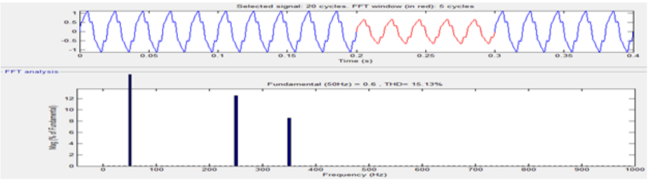

Fig 22: FFT analysis of source voltage under non-linear load conditions

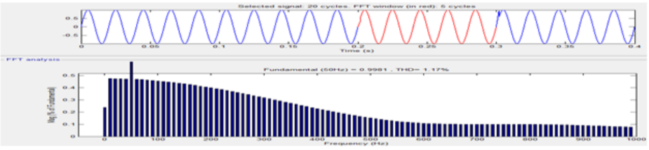

Fig 23: FFT analysis of load voltage during fault condition

V. CONCLUSION:

The operation of a DVR has been demonstrated with a new control technique using various voltage injection schemes. The effectiveness of a DVR system mainly depends upon the rating of DC storage rating and the percentage voltage sag. Therefore, DVR is considered to be an efficient solution due to its relatively low cost and small size, also it has a fast dynamic response. The DVR handles both balanced and unbalanced situations without any difficulties and injects the appropriate voltage component to keep the load voltage balanced and constant at the nominal value. The main advantages of DVR are low cost, simpler implementation; require less computational efforts and its control is simple as compared to other methods.

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