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FFT Implementation of Multi-Precision Based Dynamic Voltage Scaling Multiplier with Operands Scheduler

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ABSTRACT

In this paper, we present a multi-precision (MP) reconfigurable multiplier that incorporates variable precision, parallel processing (PP), razor-based dynamic voltage scaling (DVS), and dedicated multi-precision (MP) operands scheduling to provide optimum performance for a variety of operating conditions. All of the building blocks of the proposed reconfigurable multiplier can either work as independent smaller-precision multipliers or work in parallel to perform higher-precision multiplications. Given the user's requirements, a dynamic voltage/ frequency scaling management unit configures the multiplier to operate at the proper precision and frequency. Adapting to the run-time workload of the targeted application, razor flip-flops together with a dithering voltage unit then configure the multiplier to achieve the lowest power consumption. The single-switch dithering voltage unit and razor flip-flops help to reduce the voltage safety margins and overhead typically associated to dynamic voltage scaling (DVS) to the lowest level. The large silicon area and power overhead typically associated to reconfigurability features are removed. Finally, the proposed novel multi-precision (MP) multiplier can further benefit from an operands scheduler that rearranges the input data, hence to determine the optimum voltage and frequency operating conditions for minimum power consumption.

Experimental results show that the proposed multi-precision (MP) design features a reduction in circuit area and power consumption compared with conventional fixed-width multiplier. When combining this multi-precision (MP) design with error-tolerant razor-based dynamic voltage scaling (DVS), parallel processing (PP), and the proposed novel operands scheduler, total power reduction is achieved. This paper successfully demonstrates that multi-precision (MP) architecture can allow more aggressive frequency/supply voltage scaling for improved power efficiency.

INTRODUCTION

Multipliers perform one of the most frequently encountered arithmetic operations in digital signal processors (DSPs). Most of today's full-custom digital signal processors (DSPs) and application-specific integrated circuits (ASICs) are designed for a fixed maximum word-length optimization. Therefore, an 8-bit multiplication computed on a 32-bit Booth multiplier would result in unnecessary switching activity and power loss.

The proposed multiplier not only combines multi-precision (MP) and dynamic voltage scaling (DVS) but also parallel processing (PP). Our multiplier comprises 8 × 8 bit reconfigurable multipliers. These building blocks can either work as nine independent multipliers or work in parallel to perform one, two or three 16 × 16 bit multiplications or a single-32 × 32 bit operation.

EXISTING SYSTEM

This spurious switching activity can be mitigated by balancing internal paths through a combination of architectural and transistor-level optimization techniques. In addition to equalizing internal path delays, dynamic power reduction can also be achieved

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by monitoring the effective dynamic range of the input operands so as to disable unused sections of the multiplier and/or truncate the output product at the cost of reduced precision. This is possible because, in most sensor applications, the actual inputs do not always occupy the entire magnitude of its word-length. For example, in artificial neural network applications, the weight precision used during the learning phase is approximately twice that of the retrieval phase. Besides, operations in lower precisions are the most frequently required. In contrast, most of today's full-custom digital signal processors (DSPs) and application-specific integrated circuits (ASICs) are designed for a fixed maximum word-length so as to accommodate the worst case scenario. Therefore, an 8-bit multiplication computed on a 32-bit Booth multiplier would result in unnecessary switching activity and power loss.

PROPOSED SYSTEM

In this paper, we propose a low power reconfigurable multiplier architecture that combines multi-precision (MP) with an error-tolerant dynamic voltage scaling (DVS) approach based on razor flip-flops. The main contributions of this paper can be summarized follows.
1) A novel multi-precision (MP) multiplier architecture featuring, respectively, reduction in silicon area and power consumption compared with its conventional 32 × 32 bit fixed-width multiplier counterpart. All reported multipliers trade silicon area/power consumption for multi-precision (MP). In this paper, silicon area is optimized by applying an operation reduction technique that replaces a multiplier by adders/subtractors.

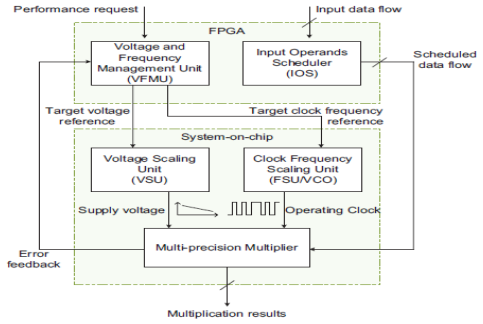

Fig: -1. Proposed multiplier system architecture

The proposed multi-precision (MP) multiplier system (Fig. 1) comprises five different modules that are as follows:
1) The multi-precision (MP) multiplier; 2) The input operands scheduler (IOS) whose function is to reorder the input data stream into a buffer, hence to reduce the required power supply voltage transitions; 3) The frequency scaling unit implemented using a voltage controlled oscillator (VCO). Its function is to generate the required operating frequency of the multiplier; 4)The voltage scaling unit (VSU) implemented using a voltage dithering technique to limit silicon area overhead. Its function is to dynamically generate the supply voltage so as to minimize power consumption;5)The dynamic voltage/frequency management unit (VFMU) that receives the user requirements (e.g., throughput). The voltage/frequency management unit (VFMU) sends control signals to the voltage scaling unit (VSU) and frequency scaling unit (FSU) to generate the required power supply voltage and clock frequency for the multi-precision (MP) multiplier. The multi-precision (MP) multiplier is responsible for all computations. It is equipped with razor flip-flops that can report timing.

MODULES EXPLANATIONS

STRUCTURE OF INPUT INTERFACE UNIT

Bellow Fig. shows the structure of the input interface unit, which is a sub module of the multi-precision (MP) multiplier. The role of this input interface unit (Fig.2) is to distribute the input data between the nine independent processing elements (PEs) (Fig.5) of the 32 × 32 bit multi-precision (MP) multiplier, considering the selected operation mode. The input interface unit uses an extra most significant bit (MSB) sign bit to enable both signed and unsigned multiplications. A 3-bit control bus indicates whether the inputs are 1/4/9 pair(s) of 8-bit operands, or 1/2/3 pair(s) of 16-bit operands, or 1 pair of 32-bit operands, respectively. Depending on the selected operating mode, the input data stream is distributed Multiplier Figure between the processing elements (PEs) to perform the computation.

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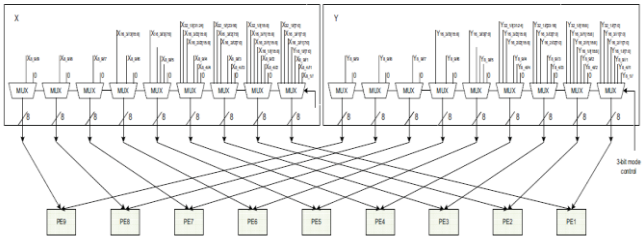

Fig:- 2. Structure of input interface unit

THREE PE's COMBINED TO FORM 16 X 16 BIT MULTIPLIER

In Fig shows how three 8 × 8 bit processing elements (PEs) are used to realize a 16 × 16 bit multiplier. The 32 × 32 bit Multiplier is constructed using a similar approach but requires 3 × 3 processing elements (PEs).

A 3-bit control word defines which processing elements (PEs) work concurrently and which processing elements (PEs) are disabled. Whenever the full precision (32 × 32 bit) is not exercised, the supply voltage and the clock frequency may be scaled down according to the actual workload. To evaluate the overhead associated to reconfigurability and multi-precision (MP), we define *X* and *Y* as the 2*n*-bits wide multiplicand and multiplier, respectively. *XH*, *YH* are their respective *n* most significant bits whereas *XL*, *YL* are their respective *n* least significant bits. X_LY_L ,X_HY_L , X_LY_H, X_HY_H is the crosswise products.

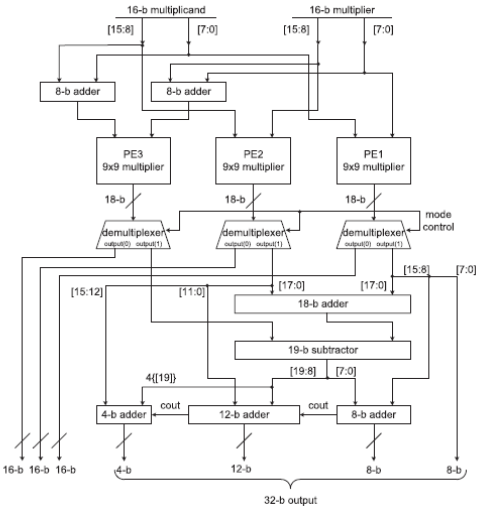

Fig:- 3. Three processing elements (PE's) combined to form 16 x16 multiplier

RAZOR FLIP-FLOP

The razor flip-flop operates as a standard positive edge triggered flip-flops coupled with a shadow latch, which samples at the negative edge. Therefore, the input data is given in the duration of the positive clock phase to settle down to its correct state before being sampled by the shadow latch. The minimum allowable supply voltage needs to be set, hence the shadow latch always clocks the correct data even for the worst case conditions. This requirement is usually satisfied given that the shadow latch is clocked later than the main flip-flop. A comparator flags a timing error when it detects a discrepancy between the speculative data sampled at the main flip-flop and the correct data sampled at the shadow latch. The correct data would subsequently overwrite the incorrect signal. The key idea behind razor flip-flops is that if an error is detected at a given pipeline stage *X*, then computations are only re-executed through the following pipeline stage *X* + 1. This is possible because the correct sampled value would be held by the shadow latch. This approach ensures forward progress of data through the entire pipeline at the cost of a single-clock cycle.

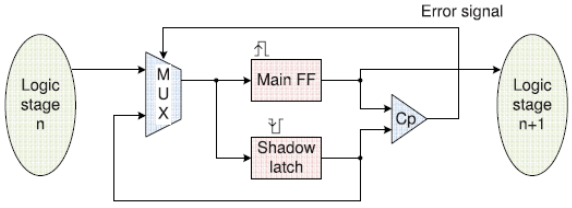

Fig:- 4. Conceptual view of razor flip-flop

THE PROPOSED MULTIPLIER

The proposed multiplier (Fig. 5) not only combines multi-precision (MP) and dynamic voltage scaling (DVS) but also parallel processing (PP). Our multiplier comprises 8 × 8 bit reconfigurable multipliers. These building blocks can either work as nine independent multipliers or work in parallel to perform one, two or three 16 × 16 bit multiplications or a single-32 × 32 bit operation. Parallel processing (PP) can be used to increase the throughput or reduce the supply voltage level for low power operation.

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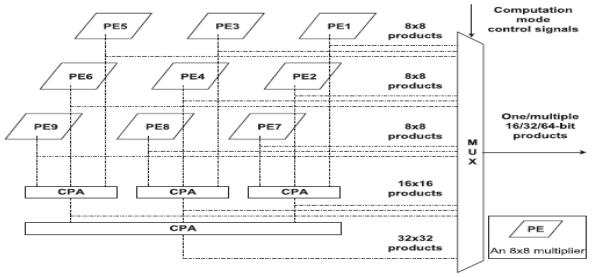

Fig:- 5. Possible configuration modes of proposed multi-precision (MP) multiplier

FFT ARCHITECTURE

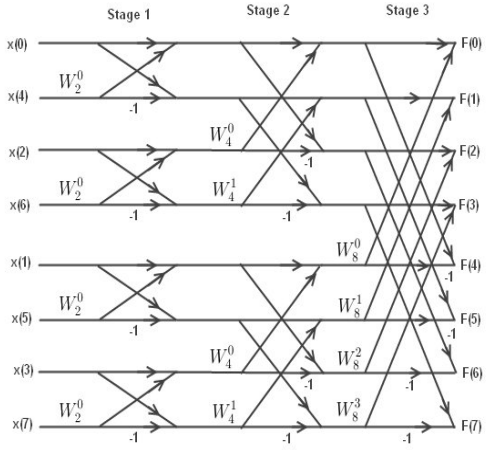

Fig:-6. FFT Architecture

SIMULATION RESULTS

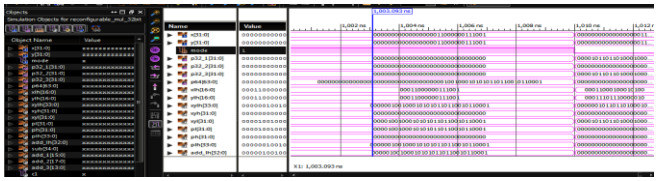

Fig:-7. Simulation result for test_reconfigurable_multiplier_32bit

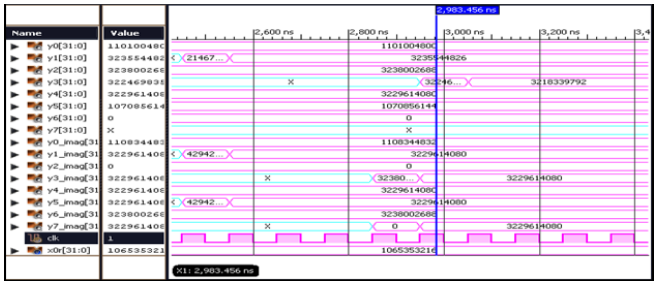

Fig:-8. Simulation result for test_reconfigurable_multiplier_FFT

PERFORMANCE COMPARISON

Design	XORs	LUTs	IOBs	Delay(ns)	Memory(kb)
Reconfigurable_mul_32bit	898	1744	225	36.116	233808
Reconfigurable_mul_64bit	6658	5903	449	110.760	205632
Reconfigurable_mul_FFT	104516	100523	1032	210.588	561024

CONCLUSION & FUTURE SCOPE

A novel multi-precision (MP) multiplier architecture featuring, reduction in power consumption compared with its 32 × 32 bit conventional fixed-width multiplier counterpart. When integrating this multi-precision (MP) multiplier architecture with an error tolerant razor-based dynamic voltage scaling (DVS) approach and the proposed novel operands scheduler .In FFT Implementation and digital signal processing (DSP) Applications the multi-precision (MP) reconfigurable multiplier is major concern in calculations. The future implementation of this paper is by using some other applications we can reduce the area and delay. The 64x64 multi-precision (MP) reconfigurable multiplier provided a solution towards achieving full computational flexibility and low power consumption for various general purpose low-power applications. If look up table (LUT) uses in the proposed multiplier architecture, It provides a solution to achieve the reduced delay low power consumption and full computational flexibility. If Carry Select Adder (CSA) uses in the proposed multiplier architecture, it provides a solution to reduces the time delay and this multiplier used in FIR filters.

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