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A 17 Voltage Levels Using a Three Level Flying Capacitor Inverter

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Abstract

Multilevel power converter has wide range of applications because increasing the number of voltage levels , the output voltage is nearer to sinusoidal wave with reduced harmonic content, and greatly improving the performance of the drive. In this paper 17 voltage levels generated by using a multi level inverter of a three-level flying capacitor inverter and cascaded H-bridge modules with floating capacitors has been proposed. The stability of the capacitor balancing algorithm has been verified both during transients and steady-state operation. By using the pole voltage combination all the capacitors voltages can be balanced. Another advantage of this topology is its ability to generate all the voltages from a single dc-link power supply which enables back to back operation of converter. The presented inverter able to operate at all the power factor ranges. The performance of the system can be observed in simulation results. Even though H-bridge is failed inverter can operate at full load for reduced levels. The simulation results are shown in MATLAB/SIMULINK

I. INTRODUCTION

Multi level inverters are currently now a day's mostly using in several applications, because the number of voltage levels will increase, the output voltage is nearer to sinusoidal wave with reduced harmonic content, improving the performance of the drive greatly as given in [4] and [5]. Various aspects of the proposed inverter like capacitor voltage leveling are given in the present paper. The work given in [9] generates multiple voltage levels by change the load current through capacitors. One in every of the pioneering works within the field of multilevel inverters is that the neutral point clamped inverter [6].

On the other hand, the use of multiple isolated dc sources using H-bridges for plasma stabilization generating multiple voltage levels was given in [7]. The work given in [8] analyzes the problems with the theme of cascading multiple rectifiers and proposes a solution for balancing the capacitors Here, the voltage through the capacitors is maintained at desired price by changing the direction of load current through the capacitor by choosing the redundant states for an equivalent pole voltage. The work given in [10] combines the concepts of work given in [9] and [7].

Here, the floating capacitors H-bridges are used to generate multiple output voltages. The to generate multiple output voltages. The voltages of the capacitors are maintained at their intended values by switching through redundant states for the same voltage level. The works given address aspects of using cascaded H-bridges and propose numerous efficient control algorithms. modular structure converters that are highly regarded in HVDC applications are another genre of multilevel converters which may be used for motor drive applications as given. The conception of cascading flying capacitor inverter with neutral point clamped inverter is given. The conception of increasing the number of levels using flying capacitor inverter with cross connected capacitors has been given. a noteworthy configuration to get seventeen voltage levels mistreatment multiple capacitors is given. but the capacitor voltages can't be balanced instantly. They'll be balanced only at the basic frequency.

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II. PROPOSED TOPOLOGY CONFIGURATION

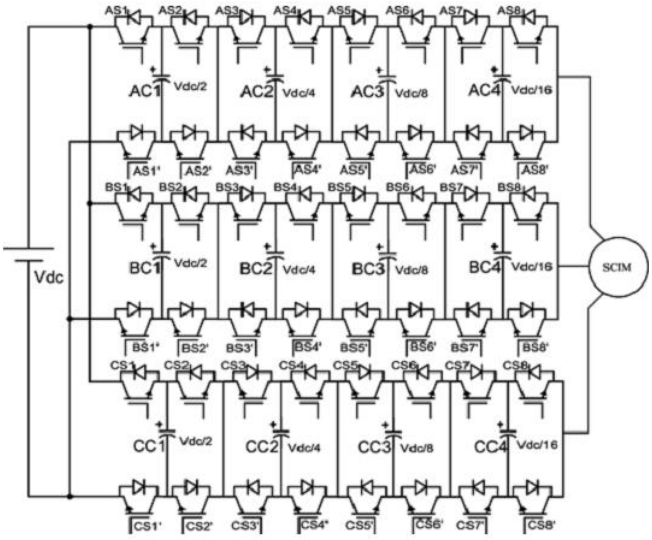

Fig. 1. Three-phase power schematic of the proposed seventeen-level inverter configuration formed by cascading three-level flying capacitor inverter with three H-bridges using a single dc link.

The voltages of capacitors AC1, BC1, and CC1 are maintained at Vdc/2. Capacitors AC2, BC2, and CC2 are maintained at voltage level of Vdc/4. Similarly capacitors AC3, BC3, and CC3 are maintained at voltage level of Vdc/8 and capacitors AC4, BC4, and CC4 are maintained at voltage level of Vdc/16. The three-phase power schematic is shown in Fig.1.It consits of hybrid multilevel topology employing a three-level flying capacitor inverter and cascading it with three floating capacitor H-Bridges. Each cascaded H-bridge can either add or subtract its voltage to the voltage generated by its previous stage.

In addition to that, the CHBs can also be bypassed. The resulting inverter pole voltage is the arithmetic sum of voltages of each stage. The schematic diagram for one phase of the proposed converter is shown in Fig. 2. The switch pairs (AS1, AS1'), (AS2, AS2'), (AS3, AS3'), (AS4, AS4'), (AS5, AS5'), (AS6, AS6'), (AS7, AS7'), and (AS8, AS8') are switched in complementary fashion with appropriate dead time. Each switch pair has two distinct logic states,

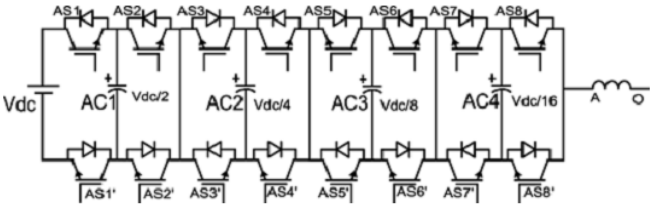

Fig. 2. One phase of the proposed 17-level inverter configuration formed by cascading three-level flying capacitor inverter with three H-bridges using a single dc link.

Namely top device is ON (denoted by 1) or the bottom device is ON (denoted by 0). Therefore, there are 256 (28) distinct switching combinations possible. Each voltage level can be generated using one or more switching states (pole voltage redundancies). By switching through the redundant switching combinations (for the same pole voltage), the current through capacitors can be reversed and their voltages can be controlled to their prescribed values.

This method of balancing the capacitor voltages at all load currents and power factors instantaneously has been observed for 17 pole voltage levels. They are 0, Vdc/16, Vdc/8, 3 Vdc/16, Vdc/4, 5 Vdc/16, 3 Vdc/8, 7 Vdc/16, Vdc/2, 9 Vdc/16, 5 Vdc/8, 11 Vdc/16, 3 Vdc/4, 13 Vdc/16, 7 Vdc/8, 15 Vdc/16, and Vdc. However, by switching through all the possible pole voltage switching combinations, 31 distinct pole voltage levels can be generated using the proposed topology. In the additional 14 levels, the voltages of capacitors can be balanced only in a fundamental cycle. There are 82 switching combinations (see Table I) that can be used to generate the above mentioned 17 pole voltage levels where instantaneous capacitor voltage balancing is possible.

The effect of 82 switching combinations on every capacitor's charge state (charge or discharge) for positive direction of current (i.e., when the pole is sourcing current as marked in Fig. 3) is shown in Table I. For negative direction of current, the effect of the switching state on the capacitor is reversed. For example, when the controller demands a pole voltage

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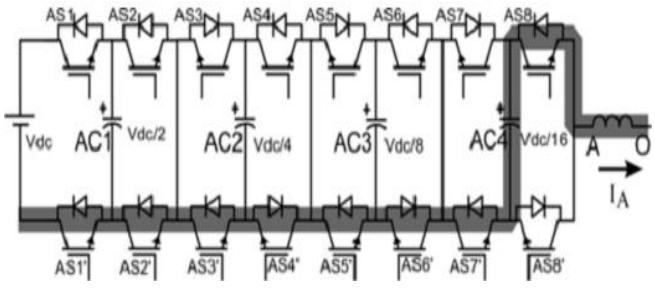
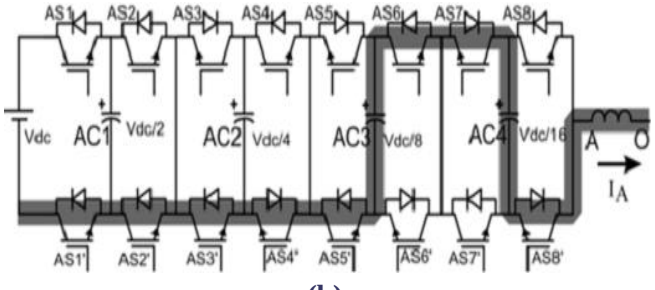
of Vdc/16, there are five different redundant switching combinations to generate it.

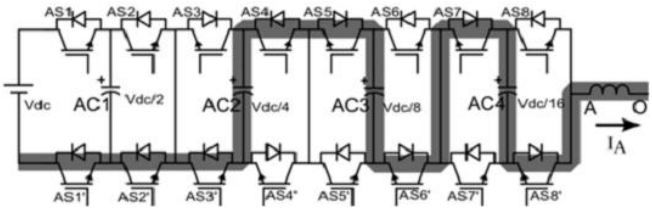
Each switching combination has a different effect on the state of charge of the capacitors. When the switching state (0, 0, 0, 0, 0, 0, 0, 1) (see Table I) is applied, the capacitor C4 discharges when the pole is sourcing current as [see Fig. 3(a)]. To balance the capacitor C4 and to bring its voltage back to the prescribed value (Vdc/16), one of the other four switching combinations is applied Fig. 3(b)–(e). It can be observed that when switching state (0, 0, 0, 0, 0, 1, 1, 0) is applied, the direction of current in the capacitor C4 is reversed [see Fig. 3(b)] and the capacitor C4 charges. However in this process, the capacitor C3 is discharged. If the capacitor C3 needs charging, switching state redundancy of (0, 0, 0, 1, 1, 0, 1, 0) is applied [see Fig. 3(c)] which discharges C2. As shown in Fig. 3(d) to charge C2 one of the switching redundancies and (e) is applied based on the state of charge of capacitor C1. If switching state (0, 1, 1, 0, 1, 0, 1, 0) is applied, the capacitor C1 is discharged and this state charges all the other capacitors as shown in Fig. 3(d). Finally, when switching state of (1, 0, 1, 0, 1, 0, 1, 0) is applied, all the four capacitors are charged for positive direction of current as shown in Fig. 3(e).



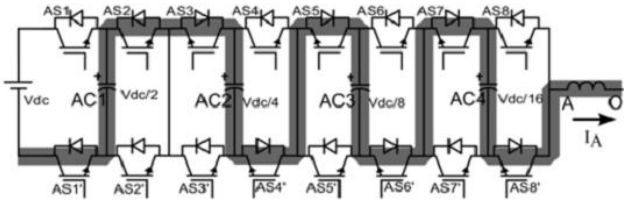
(a)



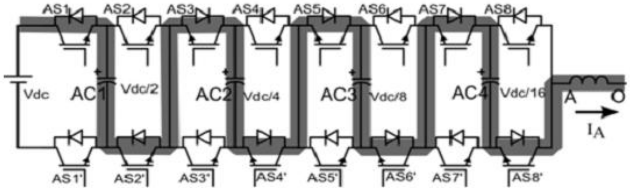
(b)



(c)



(d)



(e)

Fig. 3. Switching Redundancies for pole voltage of Vdc/16. (a) Current path for switching state (0, 0, 0, 0, 0, 0, 0, 1). (b) Current path for switching state (0, 0, 0, 0, 0, 1, 1, 0). (c) Current path for switching state (0, 0, 0, 1, 1, 0, 1, 0). (d) Current path for switching state (0, 1, 1, 0, 1, 0, 1, 0). (e) Current path for switching state (1, 0, 1, 0, 1, 0, 1, 0).

If all the capacitors need discharging, the capacitor C4 is discharged first and the remaining capacitors can be discharged during subsequent switching cycles when C4 needs to be charged.

By switching through the redundant pole voltage combinations, all the capacitors' voltages can be maintained at their prescribed values it can be observed that the while generating pole voltage of Vdc/16 for positive direction of current.

For negative direction of current, the effect of the capacitor voltages is the opposite. The entire process of capacitor voltage balancing for pole voltage of Vdc/16 that has been explained is illustrated in Fig. 4.

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Here, the capacitor voltage variation with application of various redundant states for pole voltage of Vdc/16 has been shown for positive direction of current. For other pole voltages namely, Vdc/8, 3 Vdc/16, Vdc/4, 5 Vdc/16, 3 Vdc/8, 7 Vdc/16, Vdc/2, 9 Vdc/16, 5 Vdc/8, 11 Vdc/16, 3 Vdc/4, 13 Vdc/16, 7 Vdc/8, 15 Vdc/16, and Vdc, to balance all the capacitor voltages a similar strategy can be used. The switching frequency of any CHB module is at most the PWM switching frequency of the converter.

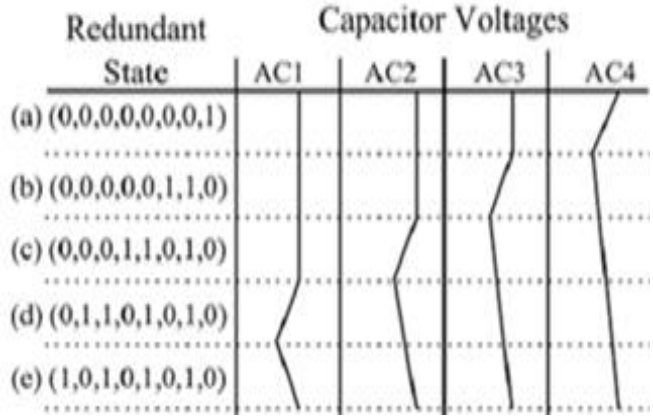

Fig. 4. Capacitor voltage variation with application of redundant states for pole voltage of Vdc/16 for positive current.

III. SPACE VECTOR CONTROL REGION

Each pole of the three-phase inverter can generate one of the 17 discrete pole voltage levels namely 0, Vdc/16, Vdc/8, the capacitor is charging, discharging Symbols of + , −, indicates, and no effect respectively for positive direction of current.3 Vdc/16, Vdc/4, 5 Vdc/16, 3 Vdc/8, 7 Vdc/16, Vdc/2, 9 Vdc/16, 5 Vdc/8, 11 Vdc/16, 3 Vdc/4, 13 Vdc/16, 7 Vdc/8, 15 Vdc/16, and Vdc. For the proposed three-phase inverter, there is a total of 4913 (173) pole voltage combinations. Each pole voltage combination generates a voltage space vector VSV as given in the following equation:

$$V_{SV} = V_{AN} + V_{BN} < 120° + V_{CN} < 240° \qquad (1)$$

Where VAN , VBN and VC N are the three-phase voltages.

The diagram of the space vector polygon formed by these 817 locations is shown in Fig. 5. There 16 concentric hexagons that form the space vector control region of the proposed seventeen level inverter. The space vectors on the outer hexagon do not have any phase voltage redundancies.

TABLE I POLE VOLTAGE REDUNDANCIES AND CAPACITOR STATES FOR VARIOUS SWITCHING COMBINATIONS WHEN POLE SOURCES CURRENT

S. No.	Pole Voltage	Switch State (S1, S2, S3, S4, S5, S6, S7, S8)	C1ª	C2ª	C3ª	C4ª	S.No	Pole Voltage	Switch State (S1, S2, S3, S4, S5, S6, S7, S8)	C1ª	C2ª	C3ª	C4ª
1	0	(0, 0, 0, 0, 0, 0, 0, 0)	0	0	0	0	42	Vdc/2	(1, 0, 0, 0, 0, 0, 0, 0)	+	0	0	0
2	Vdc/16	(0, 0, 0, 0, 0, 0, 0, 1)	0	0	0	−	43	9 Vdc/16	(0, 1, 0, 0, 0, 0, 0, 1)	−	0	0	−
3		(0, 0, 0, 0, 0, 1, 1, 0)	0	0	−	+	44		(0, 1, 0, 0, 0, 1, 1, 0)	−	0	−	+
4		(0, 0, 0, 1, 1, 0, 1, 0)	0	−	+	+	45		(0, 1, 0, 1, 1, 0, 1, 0)	−	−	+	+
5		(0, 1, 1, 0, 1, 0, 1, 0)	−	+	+	+	46		(1, 0, 0, 0, 0, 0, 0, 1)	+	0	0	−
6		(1, 0, 1, 0, 1, 0, 1, 0)	+	+	+	+	47		(1, 0, 0, 0, 0, 1, 1, 0)	+	0	−	+
7	Vdc/8	(0, 0, 0, 0, 0, 1, 0, 0)	0	0	−	0	48		(1, 0, 0, 1, 1, 0, 1, 0)	+	−	+	+
8		(0, 0, 0, 1, 1, 0, 0, 0)	0	−	+	0	49		(1, 1, 1, 0, 1, 0, 1, 0)	0	+	+	+
9		(0, 1, 1, 0, 1, 0, 0, 0)	−	+	+	0	50	5 Vdc/8	(0, 1, 0, 0, 0, 1, 0, 0)	−	0	−	0
10		(1, 0, 1, 0, 1, 0, 0, 0)	+	+	+	0	51		(0, 1, 0, 1, 1, 0, 0, 0)	−	−	+	0
11	3 Vdc/16	(0, 0, 0, 0, 0, 1, 0, 1)	0	0	−	−	52		(1, 0, 0, 0, 0, 1, 0, 0)	+	0	−	0
12		(0, 0, 0, 1, 0, 0, 1, 0)	0	−	0	+	53		(1, 0, 0, 1, 1, 0, 0, 0)	+	−	+	0
13		(0, 0, 0, 1, 1, 0, 0, 1)	0	−	+	−	54		(1, 1, 1, 0, 1, 0, 0, 0)	0	+	+	0
14		(0, 1, 1, 0, 0, 0, 1, 0)	−	+	0	+	55	11 Vdc/16	(0, 1, 0, 0, 0, 1, 0, 1)	−	0	−	−
15		(0, 1, 1, 0, 1, 0, 0, 1)	−	+	+	−	56		(0, 1, 0, 1, 0, 0, 1, 0)	−	−	0	+
16		(1, 0, 1, 0, 0, 0, 1, 0)	+	+	0	+	57		(0, 1, 0, 1, 1, 0, 0, 1)	−	−	+	−
17		(1, 0, 1, 0, 1, 0, 0, 1)	+	+	+	−	58		(1, 0, 0, 0, 0, 1, 0, 1)	+	0	−	−
18	Vdc/4	(0, 0, 0, 1, 0, 0, 0, 0)	0	−	0	0	59		(1, 0, 0, 1, 0, 0, 1, 0)	+	−	0	+
19		(0, 1, 1, 0, 0, 0, 0, 0)	−	+	0	0	60		(1, 0, 0, 1, 1, 0, 0, 1)	+	−	+	−
20		(1, 0, 1, 0, 0, 0, 0, 0)	+	+	0	0	61		(1, 1, 1, 0, 0, 0, 1, 0)	0	+	0	+
21	5 Vdc/16	(0, 0, 0, 1, 0, 0, 0, 1)	0	−	0	−	62		(1, 1, 1, 0, 1, 0, 0, 1)	0	+	+	−
22		(0, 0, 0, 1, 0, 1, 1, 0)	0	−	−	+	63	3 Vdc/4	(0, 1, 0, 1, 0, 0, 0, 0)	−	−	0	0
23		(0, 1, 0, 0, 1, 0, 1, 0)	−	0	+	+	64		(1, 0, 0, 1, 0, 0, 0, 0)	+	−	0	0
24		(0, 1, 1, 0, 0, 0, 0, 1)	−	+	0	−	65		(1, 1, 1, 0, 0, 0, 0, 0)	0	+	0	0
25		(0, 1, 1, 0, 0, 1, 1, 0)	−	+	−	+	66	13 Vdc/16	(0, 1, 0, 1, 0, 0, 0, 1)	−	−	0	−
26		(1, 0, 0, 1, 0, 1, 1, 0)	+	0	+	+	67		(0, 1, 0, 1, 0, 1, 1, 0)	−	−	−	+
27		(1, 0, 1, 0, 0, 0, 0, 1)	+	+	0	−	68		(1, 0, 0, 1, 0, 0, 0, 1)	+	−	0	−
28		(1, 0, 1, 0, 0, 1, 1, 0)	+	+	−	+	69		(1, 0, 0, 1, 0, 1, 1, 0)	+	−	−	+
29	3 Vdc/8	(0, 0, 0, 1, 0, 1, 0, 0)	0	−	−	0	70		(1, 1, 0, 0, 1, 0, 1, 0)	0	0	+	+
30		(0, 1, 0, 0, 1, 0, 0, 0)	−	0	+	0	71		(1, 1, 1, 0, 0, 0, 0, 1)	0	+	0	−
31		(0, 1, 1, 0, 0, 1, 0, 0)	−	+	−	0	72		(1, 1, 1, 0, 0, 1, 1, 0)	0	+	−	+
32		(1, 0, 0, 0, 1, 0, 0, 0)	+	0	+	0	73	7 Vdc/8	(0, 1, 0, 1, 0, 1, 0, 0)	−	−	−	0
33		(1, 0, 1, 0, 0, 1, 0, 0)	+	+	−	0	74		(1, 0, 0, 1, 0, 1, 0, 0)	+	−	−	0
34	7 Vdc/16	(0, 0, 0, 1, 0, 1, 0, 1)	0	−	−	−	75		(1, 1, 0, 0, 1, 0, 0, 0)	0	0	+	0
35		(0, 1, 0, 0, 0, 1, 1, 0)	−	0	0	+	76		(1, 1, 1, 0, 0, 1, 0, 0)	0	+	−	0
36		(0, 1, 0, 0, 1, 0, 0, 1)	−	0	+	−	77	15 Vdc/16	(0, 1, 0, 1, 0, 1, 0, 1)	−	−	−	−
37		(0, 1, 1, 0, 1, 0, 1, 1)	−	+	−	−	78		(1, 0, 0, 1, 0, 1, 0, 1)	+	−	−	−
38		(1, 0, 0, 0, 0, 1, 1, 0)	+	0	0	+	79		(1, 1, 0, 0, 0, 1, 1, 0)	0	0	0	+
39		(1, 0, 0, 0, 1, 0, 0, 1)	+	0	+	−	80		(1, 1, 0, 0, 1, 0, 0, 1)	0	0	+	−
40		(1, 0, 1, 0, 0, 1, 0, 1)	+	+	−	−	81		(1, 1, 1, 0, 0, 1, 0, 1)	0	+	−	−
41	Vdc/2	(0, 1, 0, 0, 0, 0, 0, 0)	−	0	0	0	82	Vdc	(1, 1, 0, 0, 0, 0, 0, 0)	0	0	0	0

Symbols of +, −, and 0 indicates the capacitor is charging, discharging, and no effect respectively for positive direction of current.

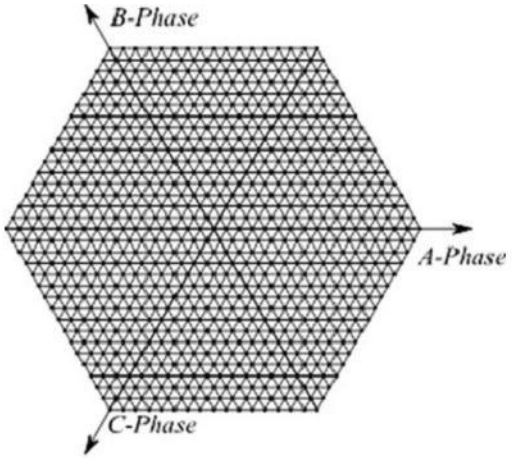

Fig. 5. Space vector polygon formed with the proposed five-level inverter the level data.

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For the smaller inner hexagons, the number of pole voltage combinations for generating the space vector locations increases. There are 16 redundant pole voltage combinations each with a different common mode voltage for each space vector location on the inner most hexagon.. The block diagram of the controller to generate the switching signals for the inverter is presented in Fig.6.

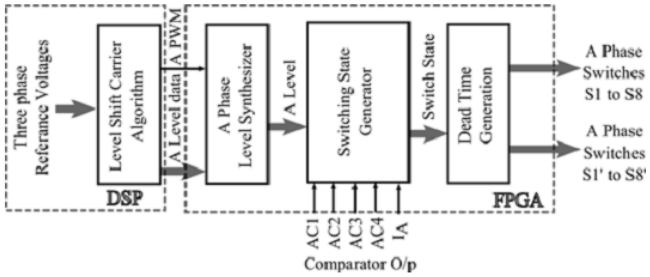


Fig. 6. Block diagram of controller for one phase of the proposed converter

These voltage levels are sent to level shifted carrier based space vector PWM generation algorithm implemented in DSP as described in [24], the output of which is (fed to FPGA) a set of level data and the PWM signal for each phase. This data is fed to a level synthesizer based on the PWM signal which generates the instantaneous level and The instantaneous level data is fed to a switching state generator which generates an appropriate switching state based on the demanded level, the state of capacitor voltages and current. In the demanded level, the state of capacitor voltages and current. by implementing the logic described in Table I as a look up table in FPGA this is achieved.

Realization of the proposed 17-level inverter needs total of 12 switches rated at Vdc/2 (4 × 3 phases), 12 switches rated at Vdc/4 (4 × 3 phases), 12 switches rated at Vdc/8 (4 × 3 phases), and 12 switches rated at Vdc/16 (4 × 3 phases) with a total of 48 switches. Also, the proposed inverter configuration has a flying capacitor stage and three cascaded floating capacitor H-bridge stages. Hence, one capacitor rated at Vdc/2 and three capacitors each rated at Vdc/4, Vdc/8, and Vdc/16 with a total of 12 capacitors are required for each phase of the proposed converter .

VI SIMULATION RESULTS

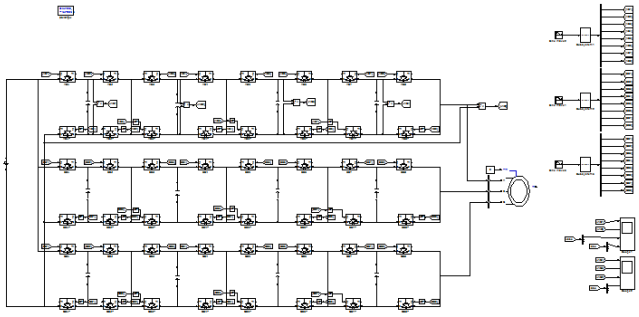
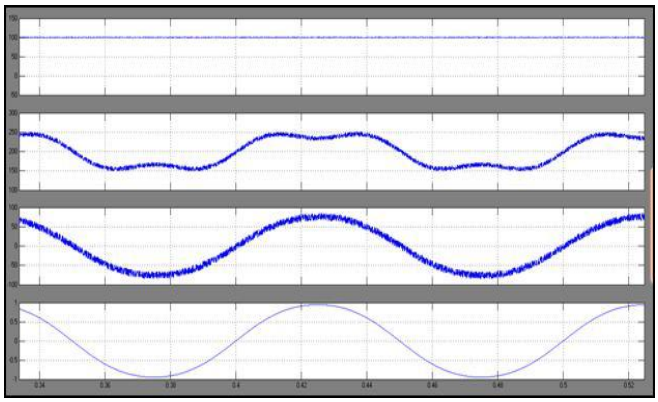
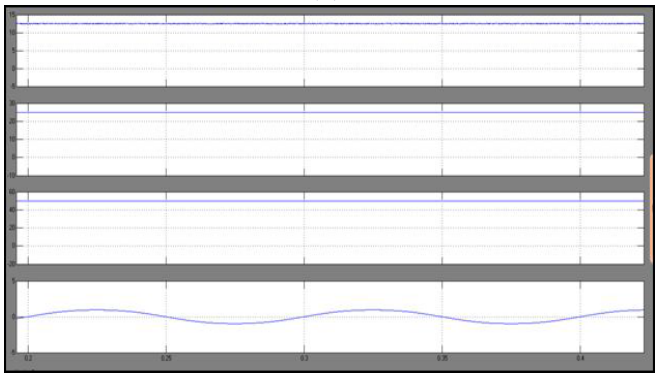


Fig. 7. Simulation diagram of the proposed system



(a)



(b)

Fig. 8. Pole, Phase, capacitor voltages along with current for 10-Hz operation of converter. VAC1 (50V/div),VAO: Pole voltage (100 V/div), VAN: Phase Voltage (100 V/div), VAC4: (100 V/div),VAC3: (10 V/div),VAC2: (25 V/div), IA:2 A/div, Timescale: (20 mS/div).

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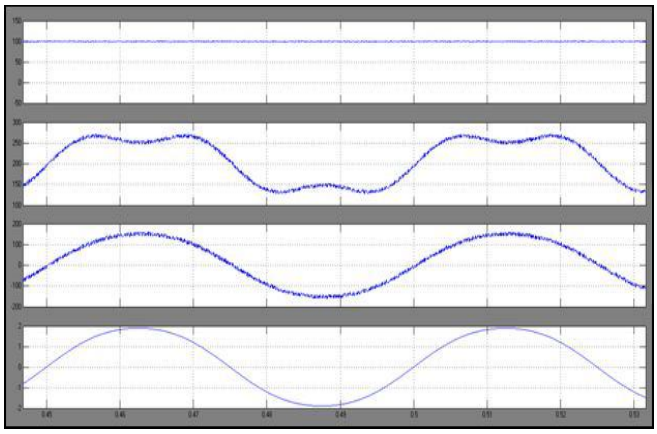
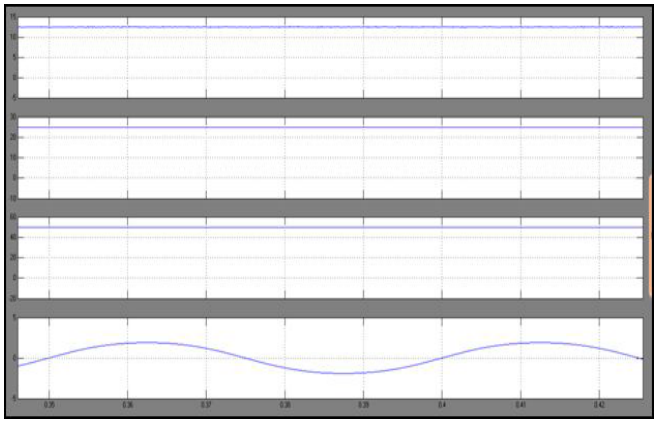
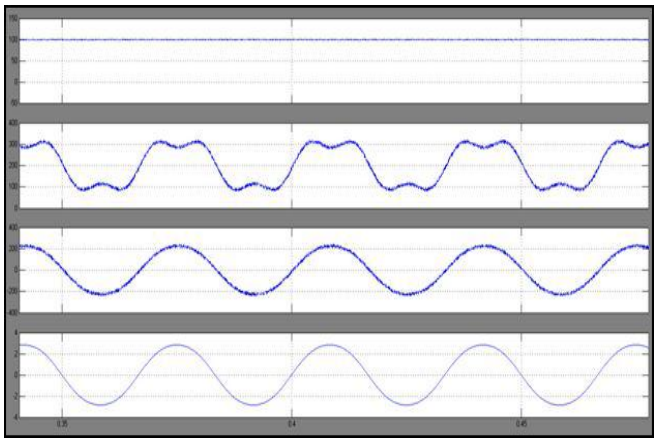


(a)

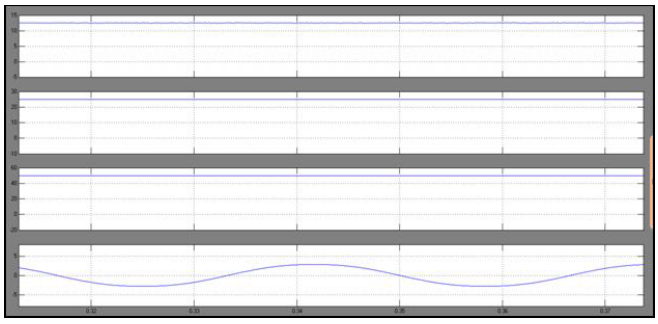


(b)

Fig. 9. Pole, Phase, capacitor voltages along with current for 20-Hz operation of the converter. VAC1: (50 V/div),VAO: Pole voltage(100 V/div), VAN: Phase Voltage (100 V/div), VAC4: (20 V/div),VAC3: (10 V/div),VAC2: (25 V/div), IA:2 A/div, Timescale: 10 mS/div.

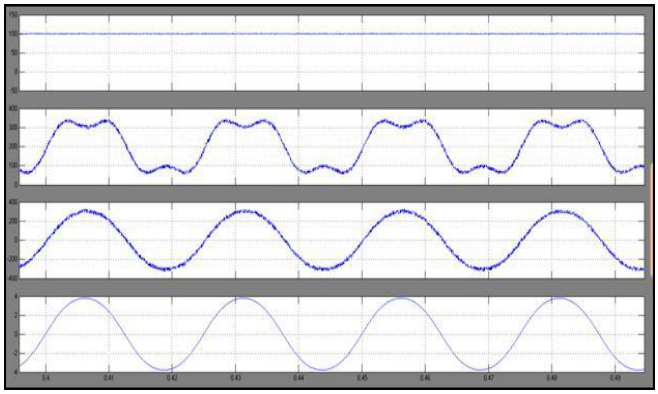


(a)

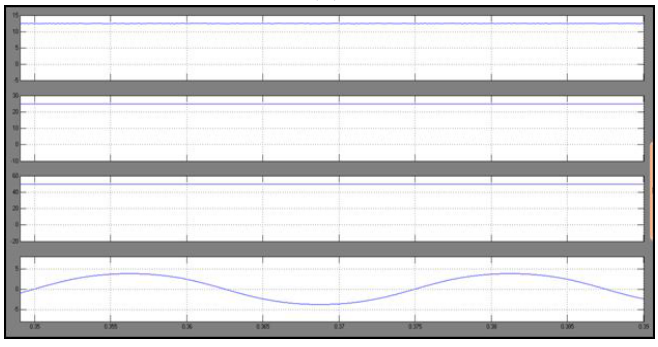


(b)

Fig. 10. Pole, Phase, capacitor voltages along with current for 30-Hz operation of the converter. VAC1:(50 V/div),VAO: Pole voltage(100 V/div),VAN: Phase Voltage (100 V/div), VAC4: (20 V/div),VAC3: (10 V/div),VAC2: (25 V/div), IA:2 A/div, Timescale: 10 mS/div.



(a)



(b)

Fig. 11. Pole, Phase, capacitor voltages along with current for 40-Hz operation of the converter. VAC1:(50 V/div),VAO: Pole voltage(100 V/div),VAN: Phase Voltage (100 V/div), VAC4: (10 V/div),VAC3: (10 V/div),VAC2: (100 V/div), IA:2 A/div, Timescale: 5 mS/div.

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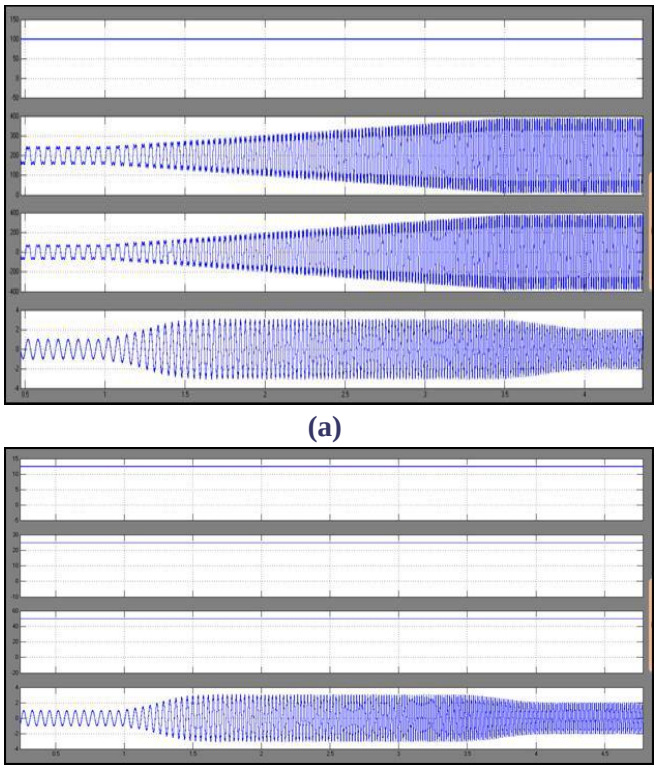

(a)

(b)

Fig. 12. Pole, Phase, capacitor voltages along with current during sudden acceleration. VAC1:Cap AC1 voltage(100 V/div), VAO: Pole Voltage(100 V/div), VAN: Phase Voltage(100 V/div),VAC4:Cap AC4 voltage(10 V/div), VAC3:CapAC3 voltage (20 V/div), VAC2:Cap AC2 voltage (20 V/div),IA: Phase current (2 A/div) Timescale: 500 mS/div.

IV. CONCLUSION

In the proposed configuration if any of the devices in any of the H-bridges fail, the faulty H-bridge are often bypassed and the electrical converter can be operated at reduced number of levels at full power. In this paper a cascading a 3- level flying capacitor and three floating capacitor H-bridges has been formed for generating a 17 level configuration and the proposed 17-level inverter has improved reliability. The advantage of the proposed configuration is modularity and symmetry in structure with the same control scheme which enables the inverter to be extended to more number of phases like five-phase and six phase configurations. At any power factor all the voltage levels can be balanced in the proposed system at full loads. The performance can be observed in the simulation. The stability of the capacitor balancing algorithm has been tested by using simulation suddenly accelerating the motor at no load and observing the capacitor voltages at various load currents.

REFERENCES

[1] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Trans. Ind. Appl.,vol. 49, no. 4, pp. 724–738, Aug. 2002.

[2] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," IEEE Ind. Electron.Mag., vol. 2, no. 2, pp. 28–39, Jun. 2008.

[3] S. Kouro, M. Malinowski, K. Gopakumar, J.Pou, L. G. Franquelo, B.Wu, J. Rodriguez, M. A. Perez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2553– 2580, Aug. 2010.

[4] A. M. Massoud, S. Ahmed, P. N. Enjeti, and B. W. Williams, "Evaluation of a multilevel cascaded-type dynamic voltage restorer employing discontinuous space vector modulation," IEEE Trans. Ind. Electron., vol. 57, no. 7, pp. 2398– 2410, Jul. 2010.

[5] S. Rivera, S. Kouro, B. Wu, S. Alepuz, M. Malinowski, P. Cortes, and J. R. Rodriguez, "Multilevel direct power control—a generalized approach for grid-tied multilevel converter applications," IEEE Trans. Power Electron., vol. 29,no. 10, pp. 5592–5604, Oct. 2014.

[6] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped PWM inverter," IEEE Trans. Ind. Appl., vol. IA-17, no. 5, pp. 518–523, Sep. 1981.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

[7] M. Marchesoni, M. Mazzucchelli, and S. Tenconi, "A non-conventional power converter for plasma stabilization," in Proc. IEEE 19th Annu. Power Electron. Spec. Conf. Rec., Apr. 11–14, 1988, vol. 1, pp. 122–129.

[8] L. Sun, W. Zhenxing, M. Weiming, F. Xiao, X. Cai, and L. Zhou, "Analysis of the DC-Link capacitor current of power cells in cascaded Hbridge inverters for high-voltage drives," IEEE Trans. Power Electron., to be published.

[9] T. A. Meynard and H. Foch, "Multi-level conversion: High voltage choppers and voltagesource inverters," in Proc. IEEE 23rd Annu. Power Electron. Spec. Conf., Jun. 29–Jul. 3, 1992, vol. 1, pp. 397–403.

[10] Z. Du, L. M. Tolbert, J. N. Chiasson, B. Ozpineci, H. Li, and A. Q. Huang, "Hybrid cascaded H-bridges multilevel motor drive control for electric vehicles," in Proc. IEEE 37th Power Electron. Spec. Conf., Jun. 18–22, 2006, pp. 1–6.