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Efficient Protection of Parallel Filters Using Error Correction Codes

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Abstract:
Many applications relay on the different filters for the processing the signal at the different levels their entire operation is depends on the performance of the filter. After increase of the advance VLSI system design the area is important aspect.we cannot tolerate the huge area considerations hence causes the huge occurrence of the faults and failures which cannot be detected at designing and also in testing but that introduces at the real time operation conditions. We are turning on to the fault determination and diagnosis system, but in previous man We are turning on to the fault determination and diagnosis system, but in previous man systems like triple modular redundancy but they results in increases in area and power. We are providing the novel method for the fault detection and correction mechanism for the similar response filters by this method provides the less consideration and performance improve also can be attained above can be designed using the VERILOG HDL, simulated in model-sim and synthesized with XILINX

I.INTRODUCTION:

Different applications that are requires a proper response analyzers and appropriate response calculations. In order to full-fill the requirements, most application relay on the suitable filters in the system. Hence the filters are the important element in the different applications, based on the application the filter design standards also will be varies some applications may consider the speed; some of them are concentrated on the area and also the power.

Based on these features the design also departs with each other but this may causes the huge increase in the architecture complexity there by causes the faults and failure occurrence. This may be not be considered by the accurate systems. In order to satisfy such systems we rely on the sophisticated faults and failure detection and alternative functional achievement. For such we uses the triple modular redundancy and the penta modular redundancy techniques were used, but the major problem that is with the use of this methods are the same circuit repeats trice and more that causes the increase in the area and power. Hence we proposes the new method of FIR filters with which we can reduces area and power of the basic filter architecture and also the error correction circuit . This paper organizes as follows. In Section I deal with the introduction, followed by the session II that deals with filter algorithm, Session III covers ECC method, session IV deals with Results and analysis of our architecture with the proposed technique And Section VI concludes the paper.

II. FILTER ALGORITHM:

Finite impulse response (FIR) digital Filter is one of the basic elements in many digital signal processing (DSP) and communication systems. It got great degree uses in many portable applications with determined area and power cheap. There are basic two FIR structures, direct form and transposed form, shown in Fig. 1 for a linear-phase even-order FIR Filter. In the direct form in Fig. 1(a), the multiple constant multiplication (MCM)/ accumulation (MCMA) module performs the concurrent multiplications of

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individual delayed signals and respective Filter coefficients, followed by accumulation of all the products.

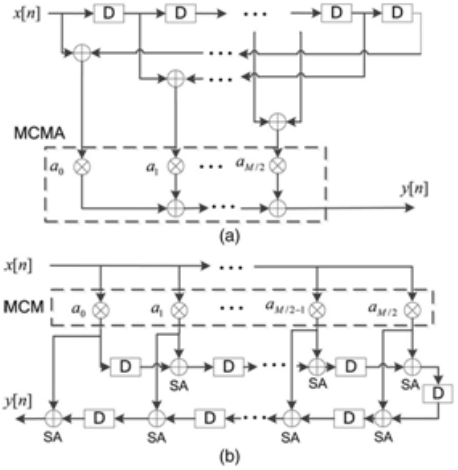

Fig.1. Structures of linear-phase even-order FIR Filters: (a) Direct form and(b) transposed form.

Base-forming of hard ware over head conditions the Fir structures are classified in two basic two types based on the utility of costly multipliers, they are multiplier-less based and memory based. Basic constant multiplications carry out by the structure adders (SAs) and delay elements. In this the Filter coefficients are fixed hence called as the multiple constant multiplications.

For better design strategies of the multiplier-less based Filter resent proposals introduces MCM with shift-and add operations and share the common sub-operations using common sub-expression elimination (CSE) and canonical signed digit (CSD) recoding to minimize the added cost of MCM [8]. For design of the reserve multiplier-less Filters, we take such considerations and stepwise design stages are listed below. By this the suitable design can be designed by the advanced and the less utilization of the adder elements in the proposed design.

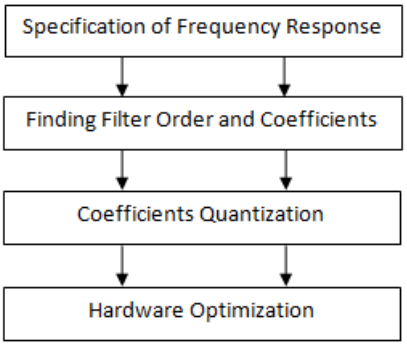

Fig.2. stages in digital FIR Filter design and implementation.

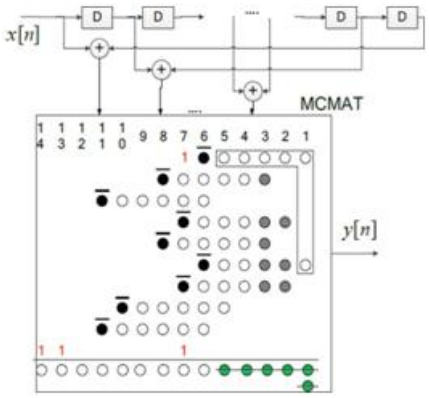

Fig.3. Overall FIR Filter architecture using multiple constant multipliers/accumulators

III.ECC METHOD:

In our proposed method the ECC calculations can be carried out by the hamming method the new advanced hamming method can be used for the detection and correction. This method wills by applied for the filter which has the same filters with different inputs. The proposed method describes that it requires the non overlapped combination of the proposed ECC. Here we adopt the OLS matrix for the calculation of the proposed ECC. The main feature that gives the advantage that gives by the OLS based hamming scheme that provides only any particular input considered for the calculation of the ECC parity bit. For our proposed method it requires the three parity bits p1, p2, p3 for the 4 different filter outputs [1]

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P1=d1 xor d2 xor d3
P2=d1 xor d2 xor d4
P3=d1 xor d3 xor d4

By this we can easily identify the erroneous data of the particular filter i.e if the three parity bits are high that means the data d1 is erroneous, if p1, p2 are high then the d2 is error data, for d3 p1 and p3 and for d4 p2 and p3. For the above each the data covered in limited parity bits only hence we can easily find the data for the correction. Proposed OLS matrixes consider for the parity bit determination.

$$G = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix}$$

$$H = \begin{bmatrix} 1 & 1 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & 1 \end{bmatrix}.$$

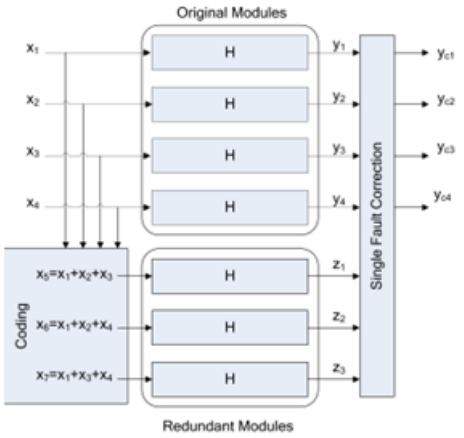

Fig.4.Proposed scheme for four Filters

IV.RESULTS AND DISCUSSION:

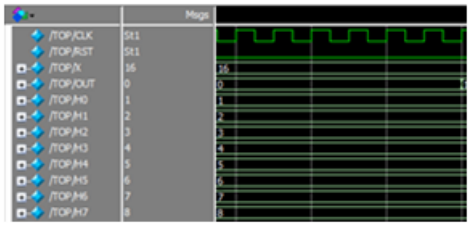

Fig.5. general simulation result for the Proposed method

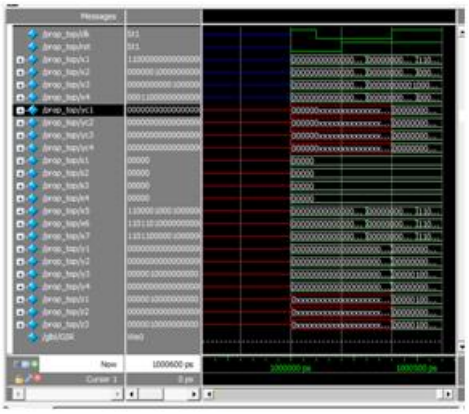

Fig6. Simulation results for the proposed method.

Form the above simulation we can observe that the same filters are taking with different inputs for the redundant modules the inputs are given as the summation of the respective inputs and normal inputs for the original modules. From the above we notice that the original module d2 has to be corrected.

V. CONCLUSION:

The proposed method is designed using the OLS matrix based hamming method for the detection of the erroneous Filter in the same type Filters with different inputs. That can be corrected using the ECC generated using the redundant modules. By this method we can detect any erroneous data by the original and as well as the redundant modules also.

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