

Design of Shift Register Using Pulse Triggered Flip Flop

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Abstract:

This paper presents a design of low power shift register using pulse triggered flip-flop. In conventional explicit type P-Flip-flop long discharging problem occurs. This problem can be solved in proposed pulse-triggered flop-flop and achieves better speed and power performance. Here by using this proposed flip flop we can design a shift register. In existing system it contains shift registers using pulsed latches but in proposed system we can replace this pulsed latches with proposed flip-flop. By using these pulse triggered proposed flip-flop we can reduce the power as well as delay of the circuit. All these simulation results are based on CMOS 180nm technology in H-SPICE tool.

Keywords:

Flip-flop, pulsed latch, pulse triggered, Shift Register, low power, Delay.

I.INTRODUCTION:

The Shift register are the basic block in a very large scale integration circuits. We can use shift registers in many applications like communication receivers, digital filters and image processing ICs. As the word length of the shifter register increases, the delay and power consumption of the shift register important design considerations. Flip-flops (FFs) are the basic storage elements used extensively in all kinds of digital designs. Pulse-triggered FF (P-FF), because of its single-latch structure, is more popular than the conventional transmission gate (TG) and master-slave based FFs in high-speed applications. Besides the speed advantage, its circuit simplicity lowers the power consumption of the clock tree system. A P-FF consists of a pulse generator for strobe signals and a latch for data storage.

If the triggering pulses are sufficiently narrow, the latch acts like an edge-triggered FF. Since only one latch, as opposed to two in the conventional master-slave configuration, is needed, a P-FF is simpler in circuit complexity. This leads to a higher toggle rate for high-speed operations. P-FFs also allow time borrowing across clock cycle boundaries and characteristic a zero or even negative setup time. Here we present a low power pulse triggered flip-flop based on a signal feed through scheme. The design manages to shorten the longer delay by feeding the input signal directly to an internal node of the latch design to speed up the data transition. This mechanism is implemented by introducing a simple pass transistor for extra signal driving. When combined with the pulse generation circuitry, it forms a new P-FF design with enhanced speed and power-delay-product (PDP) performances.

II.EXISTING SYSTEM

In shift registers pulsed latch cannot be used due to timing problem occur in this design, as shown in Fig.1

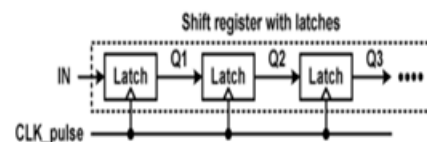


Fig.1: Shift Register with Latches and a Pulsed Clock

One solution to overcome this timing problem is adding delay circuits in between the latches, as shown in Fig. 2.

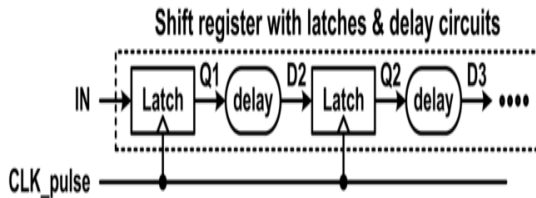


Fig.2: shift register with latches, delay circuits and pulsed clock signal

As a result, all latches have constant input signals during the clock pulse and no timing problem occurs between the latches. By adding delay circuits in between we will get more power and delay. Another solution is to use multiple non-overlap delayed pulsed clock signals, as shown in Fig. 3(a). The delayed pulsed clock signals are generated when a pulsed clock signal goes through delay circuits. Each latch uses a pulsed clock signal which is delayed from the pulsed clock signal used in its next latch. Therefore, each latch updates the data after its next latch updates the data. As a result, each latch has a constant input during its clock pulse and no timing problem occurs between latches. However, this solution also requires many delay circuits.

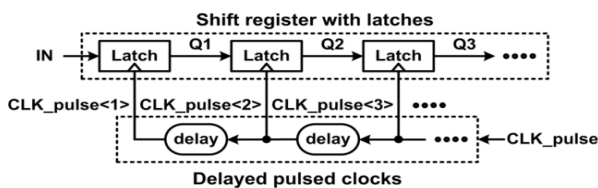


Fig.3: shift register with latches and delayed pulsed clock signal

The proposed shift register is divided into sub shifter registers to reduce the number of delayed pulsed clock signals. Fig. 4 shows an example the proposed shift register.

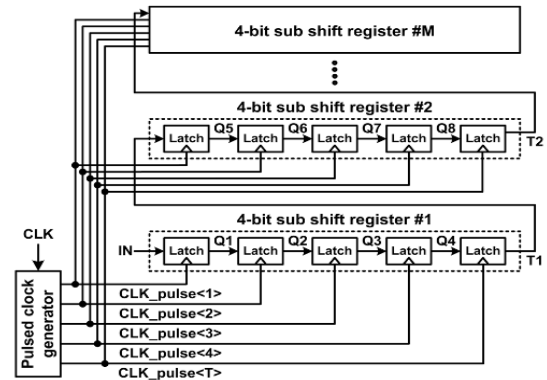


Fig.4: Shift Register Using Latches

III. PROPOSED PULSE TRIGGERED FLIP-FLOP:

Here we are designing the two types of pulse triggered designs

1. Conventional Pulse Triggered Flip-Flop
2. Pulse Triggered Flip-Flop

1. Conventional Pulse Triggered Flip-Flop:

Conventional P-FF Designs can be classified in to two types

- 1) Implicit type
- 2) Explicit type

In implicit design, latch and the pulse generator are in built present, In explicit pulse triggered design, latch and the pulse generator are separate. The implicit and explicit designs take the more power when we are working with without generating the pulse signals.

A) Ep-Dco(Explicit Pulsed Data Close To output):

The design is designed by based on explicit P-FF Design. The design has the NAND logic gate based pulse generator and True Single Phase Clock (TSPC) latch design. In this NAND gate based Pulse generator Flip-Flop Design, I3 and I4 inverters provides latch data, to hold the internal node X we are using the I1, I2 inverters. The design pulse width is determined by the delay of 3 inverters.

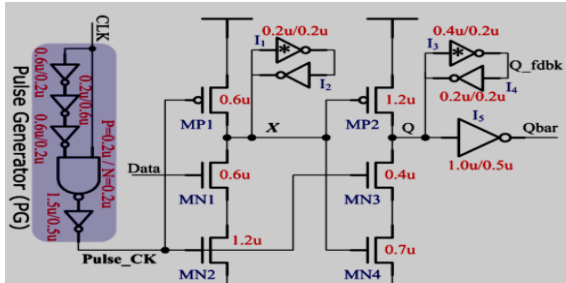


Fig.5: Ep-Dco

In Data Close to Output based on Explicit P-FF design have some drawbacks those are when the rising edge on pulse generator the internal node X will be discharged. Pulse generator provides the pulses high and low, when the pulse will be high automatically the 'X' will be discharged. To solve the problem, we are proposing the conditional precharge, conditional capture, conditional enhancement and conditional discharge.

b) Conditional discharge flipflop (CDFF):

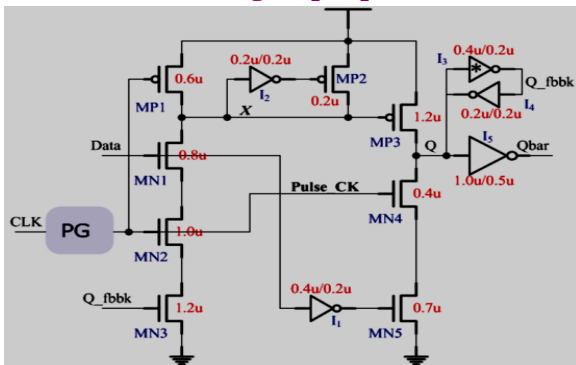


Fig.6: CDFF

An extra transistor is connected to previous design that is MN3 it controls the output Qfdbk so here no discharge will be occurred when pulse generator provides the positive peak.

c) Static conditional discharge flip-flop(SCDFF):

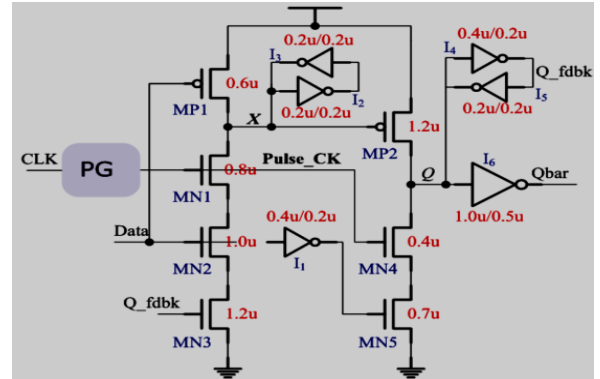


Fig.7: static-CDFF

Static CDFF design provides accurate results. The static CDFF design provides the longer data to Q delay. Both Designs are providing the longer delay in M1, M2, M3 Transistors The CDFF and Static CDFF pulse triggered Flip-Flops are providing the longer delay in M1, M2, M3 Transistors so to reduce that problem we are implementing the new design i.e. Modified Hybrid Latch Flip-Flop and it's have the static latch.

d) Modified Hybrid Latch FlipFlop(MHLFF):

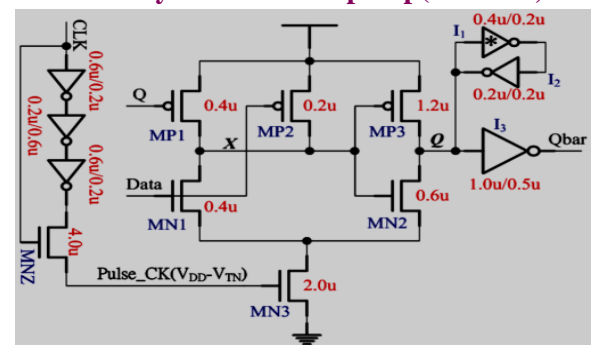


Fig.8: MHLFF

In this design the internal node 'X' will be removed. In this MHLFF design the weak signal m1 transistor controlled by the output Q when the internal node X will be zero. The design circuit complexity is high when compare with the other techniques. The figure 4 shows the MHLFF design.

2. Pulse Triggered Flip-Flop:

The DCO, CDDF, Static CDDF and MHLFF have their own drawbacks because of this reason we are proposing the Pulse Triggered Flip-Flop. The static CDDF and Proposed pulse triggered Flip-Flop both are having the static latch. However, we have the 3 major differences in proposed pulse triggered flip-flop design in a unique TSPC latch structure. First, in the first stage of TSPC latch pull up PMOS transistor MP1 gate will be connected to the ground. When the signal rising edge on that time no discharge path will be occurred in the Pulse Triggered Design. This design also reduces the capacitance node of 'X'. Second one, the simple pass transistor is controlled by the pulse clock signal which is included so that the given input data can be divided in to the latch directly. The pull up transistor MP2 that is second stage of inverter is directly connected the input Source node to Q. The level of node can be speedily pulled up to the transmission time delay. Third one, the second stage of inverter network completely removed in the pulse triggered Flip-Flop Design. Here we are connecting a new pass transistor that provides a new discharging path in the design.

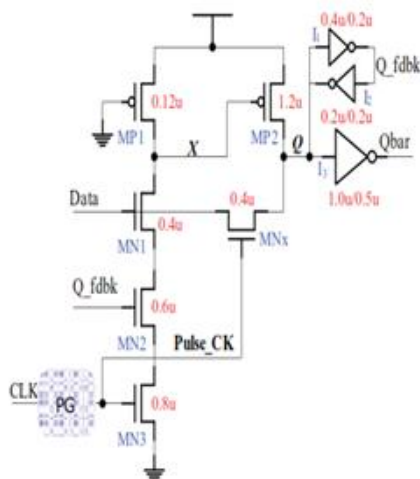


Fig.9:Proposed P-FF

By using this proposed flip-flop(P-FF) we will implement shift register because compare to all flip-flops P-FF is more advantageous in terms of power and delay.

Shift Register Design Using P-FF:

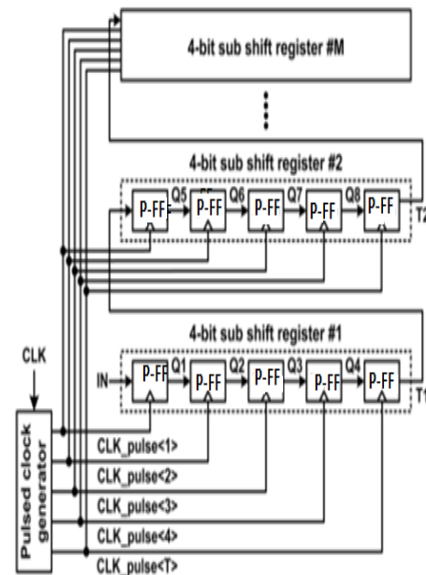


Fig.10: Proposed Shift Register Using P-FF

By using these P-FF in shift register instead latch is more efficient in terms of power and delay compared to shift register design using latch.

IV.SIMULATION RESULTS:

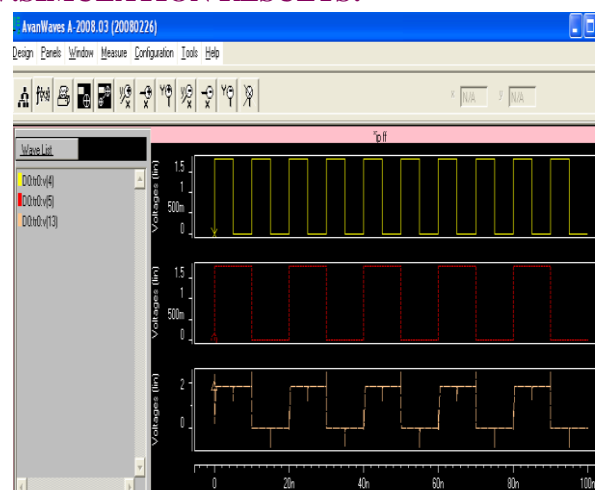


Fig.11: Simulation Results of Ep-Dco

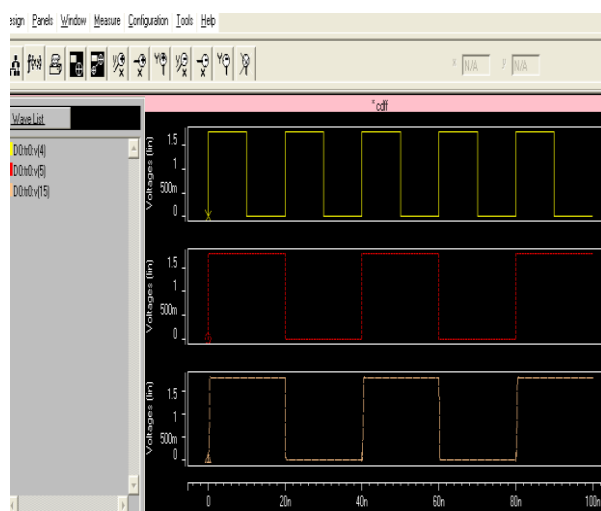


Fig.12: Simulation Results of CDFD

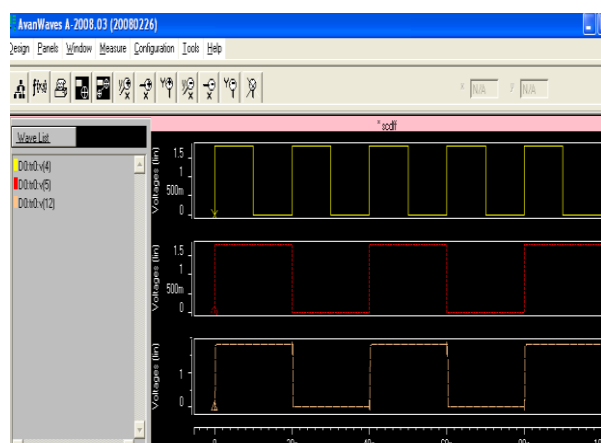


Fig.13: Simulation Results of Static-CDFD

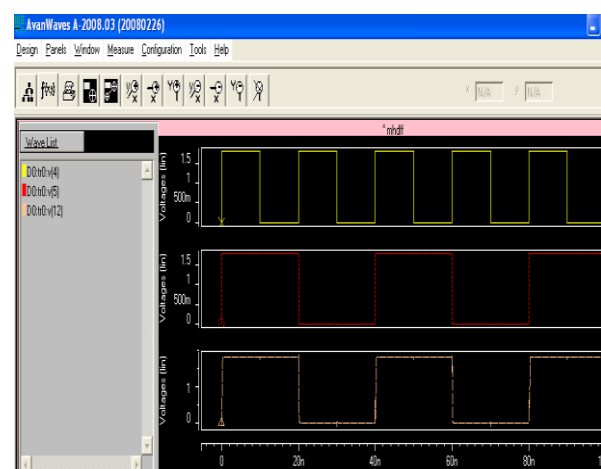


Fig.14:Simulation Results of MHLFF

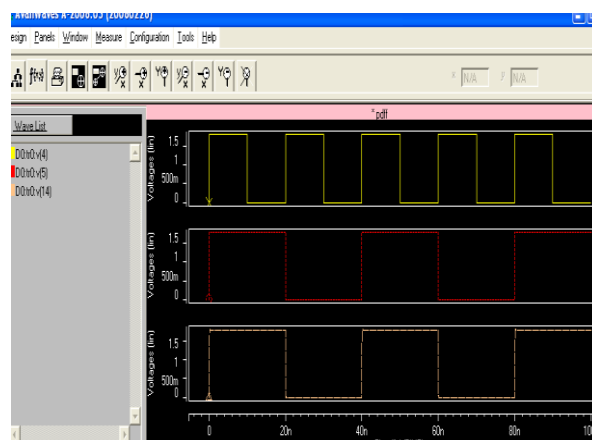


Fig.15: Simulation Results of P-FF

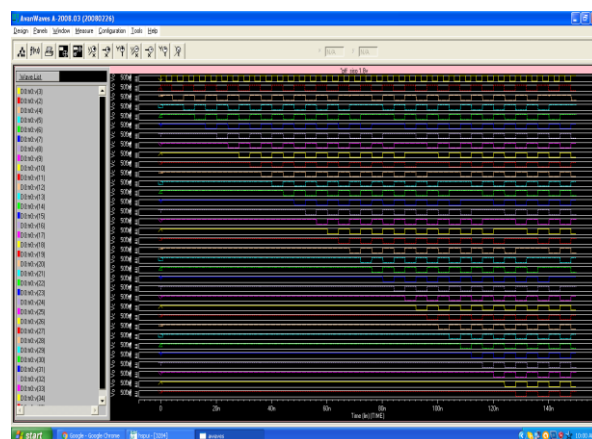


Fig.16: Simulation Results of Proposed Shift Register

Table. I. Power and delay Comparison

Design	Power (μ watts)	Delay
Shift register using latches	6860	17.21n
Ep-Dco	28.4	11.45p
CDFD	31.8	315.74p
Static-CDFD	28.6	179.16p
MHLFF	11.2	191.78p
Proposed P-FF	10.9	2.52p
Shift register using P-FF	180	139.6p

V.CONCLUSION:

Here we are designing the low power shift register using pulse triggered flip-flop based on signal feed through scheme in 90nm Technology. The proposed Pulse triggered Flip-Flop design is working with the low power and it provides the high speed results compared to the shift registers designed with latches.

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