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4x4 MIMO Alamouti Decoder Implementation Using VERTEX2

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Abstract:

The main aim of this paper is to design and implement a wireless communication system based on the IEEE 802.11n standards techniques. The results of this paper was simulated in Matlab to obtain numerical result such as bit error rate plots for different MIMO techniques and verify the functionality of each block in the design and rebuilt the whole system in Verilog for simulation and implemented on a FPGA.802.11n is the standard for wireless communication. It combines the advantage of the previous standards 802.11a/b and g. 802.11n operates in 2.4GHz like 802.11g/b, and uses OFDM (Orthogonal Frequency Division Multiplexing) for modulation of MIMO (Multiple-Input Multiple Output) technology which allows multiple signals to be sent and received at the same time. Theoretically, the 802.11n wireless system can archive a maximum data rate of 540 megabits per seconds (M bps) which is ten times faster than 802.11g 54Mbps data rate.

802.11n also has the backward compatibility to the previous standard. Implementing MIMO techniques we can use different modulation techniques like BPSK/QPSK/QAM defending on data width and bit error rate for multiple transmitter and receivers. To simulate the MIMO model of a simple 802.11n wireless communication system using the matlab communication tool box to measure bit error rate with data width plot to verify the theoretical result. To verify the functionality of each block in simulation process by using Verilog. To implement total system on FPGA sparatan6 to compare power consumption of 2x2 and 4x4 MIMO. Practically the total power will be reduced up to 50% of 4x4 MIMO. J.Ravindra

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Key words: IEEE 802.11n, MIMO technique, Modulation techniques, FPGA sparatan6

INTRODUCTION

Wireless communication has become very popular now-a-days. The increasing use of cell phone changed the way people live. We can contact each other just about anywhere and anytime. The technology and product such as Google allows people to access and find information like stock information and the whole encyclopedia instantly or instant messenger can help a person to join conferences or meetings which are happen half way around the world. The rapid development of wireless LAN also makes everything possible. People do not need to be in the same spot to solve their problem. Wireless communication makes this world spin faster.

Wireless technology still has some disadvantage like low data rate and limit in range. However, the technology has been significantly improved in the past few years. In 1997, IEEE introduced the 802.11 family standards which are the most popular standards in the market today. The newest member of the family is the802.11n standard. In this project, our objective is to build a wireless system based on the 802.11n draft using FPGA technology and Xilinx Vertex II Pro core.

Existing Work

The prototyping of multiple input-multiple output (MIMO) systems has become increasingly important to validate theoretical results, anticipating higher-data rate and improved link quality antenna systems are applied to wireless communications. For that purpose, Field Programmable Gate Arrays (FPGAs) with their



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high level of parallelism high densities and embedded multipliers are a suitable prototyping platform. The optimum detector for spatially multiplexed un-coded MIMO systems is the maximum likelihood detector (MLD) but it suffers from an extremely high complexity for large number of antennas and higher order constellations.

The maximum likelihood detector (MLD) has been implemented in practice for small constellation sizes. For medium constellation sizes, ML performance has been achieved through the use of the sphere decoder (SD) with a variable throughput. However, the problem of large constellation sizes has not been addressed from an implementation point of view. This project presents a real time FPGA implementation of a recently proposed fixed throughput sphere decoder (FSD) that can be applied to large constellation sizes achieving quasi-ML performance.

Proposed Work

Realization of multi input and multi output (MIMO) systems is highly essential for WiMAX networks. Space-time block coding is a technique used in wireless communications to transmit multiple copies of a data stream across a number of antennas and to exploit the various received versions of the data to improve the reliability of data-transfer. In wireless Communications the transmitted signal must traverse a potentially difficult environment with scattering, reflection, refraction and so on and may then be further corrupted by thermal noise. In the receiver STBC redundancy results in a higher chance of being able to use one or more of the received copies to correctly decode the received signal. The space-time coding combines all the copies of the received signal in an optimal way to extract as much information from each of them as possible. In this project a computationally efficient algorithm for space time block decoding will be implemented for FPGA based applications. The VHDL will be used for realization of the decoding algorithm and other communication blocks.

The algorithm will be realized for Binary Phase Shift Keying modulation (BPSK) scheme. The STBC encoder will also be realized in MATLAB/OCTAVE which generates the required appropriate codes for decoder. The work involves FPGA implementation of STBC decoder and demodulator. Various sub blocks such as SIN/COS generators, multipliers, adders, encoding look up tables, complex arithmetic units etc will be implemented. These blocks will be realized in style to ensure scalability and generic reconfigurability of the STBC decoder design

Overview of Alamouti Scheme

The Alamouti scheme is the only orthogonal spacetime block code using complex signals for two transmit antennas which provides full diversity of 2 and full rate of 1. For more 2010 Fifth IEEE International Symposium on Electronic Design, Test & Applications than two transmit antennas, the goal is to design transmission codes that achieve full diversity at the highest possible rate with low decoding complexity. In our 2 x 2 MIMO implementation, we use two distinct training codes over 2 time multiplexed preamble slots at the transmitter. When one transmitter is sending training data in one time slot, the other is off. These 26-bit preambles are GSM training sequence codes (TSC) 0 and 1 [11].

The two transmitters then transmit 128 space-time encoded data symbols simultaneously before the cycle repeats. At the transmitter, the SASRATS transmitters are programmed to run a 2 transmit Alamouti encoding scheme, where two symbols, s0 and s1, are transmitted simultaneously from two transmitters at time instant t. At time instant t + T, the symbols $-s1^*$ and $s2^*$ are transmitted simultaneously from the transmitters where * represents the complex conjugate. The transmission matrix is represented by the transmitted symbols travel through 2 independent channels h0 and h1 to a receiver where noises n0 and n1 are added to the received signals. h0 and h1 are complex multiplicative distortions assumed constant across two consecutive symbols. Implementation of a MIMO 2 transmitter and



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2 receiver Alamouti system, requires the estimation of 4 channel, 2 at each receiver as shown in Figure 2.1. In this situation, the output of combiner yields 2 outputs.

Where and are channel estimates from the second receiver. In the case of a 2 x 2 Alamouti implementation using PSK signals, the ML decoder remains unchanged except for the combiner. The combined output is actually the sum of from receiver 0 and from receiver 1. Likewise, is actually the sum of from receiver 0 and from receiver 1. Thus a 2 x M Alamouti implementation can be easily implemented by summing together the appropriate combiner outputs from receivers before feeding one ML detector. In an extended version of Alamouti for 4 transmitters, full rate is achieved but the system is half rank (quasiorthogonal) with some loss in diversity as transmitted symbols cannot be fully decoupled. Tarokh's STBC scheme for 4 transmitters on the other hand, achieves complete orthogonality at half the full rate. Tarokh's scheme suffers no loss in diversity and receiver decoding is simpler as the transmitted symbols can be fully decoupled.

The decoding of the Alamouti encoded signals is a linear process and our SASRATS receiver system design implements the combiner and maximum likelihood detection on the Xilinx Vertex 2 Pro FPGA board using the Xilinx Integrated System Environment (ISE) Foundation design tool.

Alamouti introduced the new transmit diversity scheme: two brands transmit diversity with one receiver as shown below and At the same period, two signals are simultaneously transmitted from two antennas. The signal s0 is transmitted from antenna 0 and s1 from antenna 1.

In the next period, which is the negative of the conjugate of s1 is transmitted at antenna 0 and conjugate of s0 is transmitted from antenna 1.



Fig1: block diagram of Alamouti decoder

Comparison between IEEE 802.11 standards Table 1: Comparison between IEEE standards

Standard	Speed+	Range*	Range (Meter)	Frequency
802.11b	11 Mbps	150 Feet	45.72 M	2.4 GHz
802.11g	54 Mbps	50 Feet	15.24 M	2.4 GHz
802.11a*	54 Mbps	50 Feet	15.24 M	5 GHz
802.11n	300 Mbps 450 Mbps§	175 Feet	51.85 M	2.4/5 GHz

The above table shows the comparison between different IEEE 802.11 series of wireless network protocols with different parameters like speed, Range and frequency.

System Architecture

The overall architecture of Alamouti 4x4 decoding scheme for QPSK modulated received symbols as shown in Fig 2.The architecture consists of several blocks. The blocks are



Fig 2: overall system architecture



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i. Pre-combiner: The inputs into the pre-combiner block consists of 16 bits I and Q data and channel estimates $\hat{h}0$ and $\hat{h}1$ which remain static for the duration of 128 data symbols. On receipt of the Data-Valid (DV) pulse from the channel estimator, the precombiner circuitry latches to capture r0 and r1 over two symbol periods and calculates the complex conjugates of $\hat{h}0$, $\hat{h}1$ and r1 needed in the combiner. This is achieved by performing a two's compliment operation on the imaginary parts of $\hat{h}0$, $\hat{h}1$ and r1 using the Xilinx two's compliment IP module. Pre-combine that alerts the user to and provides assurance concerning some problems that can occur when multiples data data-sets are merged and appended. It describes variables that are common to multiple data sets as well as variables that are unique to one data set. Where value labels are attached to variables, it checks whether code sets are identical across data sets. Summary statistics for values of all variables can also be listed and left in memory along with the descriptions of each variable of each data set.

ii.combiner:

The combiner is as shown in Fig 4.7. The combiner block calculates the s0 and s1. The product terms *r0, $\hat{h}1$ *r1, $\hat{h}1$ *r0 and $\hat{h}0$ r1* are first calculated in 4 separate Xilinx Computer Multiplier v2.0 IP blocks. The product terms $\hat{h}0$ *r0 and $\hat{h}1$ r1* are then summed to compute s0. The signal s1 is then formed by taking difference between $\hat{h}1$ *r0 and $\hat{h}0$ r1* by two properly configured Xilinx adder/subtracter v7.0 IP core respectively. An RF combiner is used to combine RF from a number of different sources. This is achieved while maintaining the characteristic impedance of the system. Dependent upon the type of combiner it may introduce additional loss by using resistors, or it may be use transformers in which case it could in theory is loss less.

iii. ML Detector:

The outputs s0 and s1 are then fed into the maximum likelihood (ML) detector processing block. The ML block consists of 2 parallel and independent sets of

Euclidean distance calculator and minimum distance comparators as shown in Fig 3. Where the decision statistics s0 and s1 are processing independently



Fig 3: ML Detector

iv. Output formatter: The output formatter places the bit estimates of s^0 and s^1 in the correct time position resulting in continuous serial bit output which can stored and checked against the original bit stream sent at the transmitter for bit error rate measurement. The system outputs 4bits for ever pair of QPSK symbol received.

Experimental Results

I. 2x2 Alamouti Decoder Results:

The 2x2 Alamouti Decoder Behavior Model and Internal Block Diagram are shown in Fig 4 and Fig 5.



Fig 4:2x2 Alamouti Decoder Behavior Model



Fig 5:2x2 Alamouti Decoder Internal Block Diagram

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The $2x^2$ Alamouti Decoder power calculations by using vertex and spartan6 are as shown in Fig 6 and Fig 7.



Fig6: 2x2 Alamouti Decoder Power calculated Using Vertex



Fig7: 2x2 Alamouti Decoder Power calculated Using Spartan6

4x4 ALAMOUTI DECODER RESULTS:

The 4x4 Alamouti Decoder Behavior Model and Internal Block Diagram are shown in Fig 8 and Fig 9.



Fig 8:4x4 Alamouti Decoder Internal Block Diagram



Fig9:4x4 Alamouti Decoder Behavior Model

The 4x4 Alamouti Decoder power calculations by using spartan6 are as shown in Fig 10



Fig10:4X4 Alamouti Decoder Power calculated Using virtex4

8. CONCLUSION & FUTURE SCOPE

In this project Alamouti STBC transmission is shown to be in upper bound for transmitting data through communication channel with respect to combating fading and transmission loss. The STBC encoding allows us to get Space wise (by multi transmitting



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antennas) and Time wise (corresponding to different transmitting times) encoding of blocks of data to be transmitted, by which reliability of data transmission is provided, the fundamental need of communication system. In MIMO[6] with STBC when selecting the number of transmit/receive antennas, several practical considerations must be taken into account as under strict delay constraints, achieving high diversity gains (i.e. high reliability) becomes critical in order to minimize the need for re-transmissions.

Since transmit/receive diversity gains experience diminishing returns as their numbers increase, complexity considerations dictate the use of small antenna arrays (typically no more than 4 antennas at each end). By providing mechanisms in reducing the setup costs and power consumption by multiple antennas in MIMO system and by combating above technologies stated problems with latest in communication system, we can effectively provide the reliable communication with less increased complexity.

Future Scope:

FPGA is a feasible solution to implement wireless communication system, but it also has some disadvantage than the normal micro controller method such as resource limitation and accuracy in calculation. If increase multiple transmitters and multiple receiver with higher modulation techniques like 8QAM/16QAM or 64QAM will reduce bit error rate and power consumption until 60 to 70% of total system with proper vertex processors.

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