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# Design and Implementation of RNS Reverse Converter Using Parallel Prefix Adders

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***ABSTRACT***

***In this paper, the implementation of residue number system reverse converters based on hybrid parallel prefix adders is analyzed. The parallel prefix adder provides high speed and reduced delay arithmetic operations but it is not widely used since it suffers from high power consumption. Hence, a hybrid parallel prefix adder component is presented to perform fast modulo addition in Residue Number System reverse conversion. The proposed components are not only results in fast arithmetic operation and it also highly reduced the hardware complexity since it requires fewer amount of logic elements. In this work, the proposed components are implemented Xilinx and different moduli sets reverse converter designs and the performances are compared for different values of n.***

***KEYWORDS:*** ***Digital Arithmetic, Parallel-prefix adder, Residue number system (RNS), Reverse converter.***

## I. INTRODUCTION

The Residue Number System plays a significant role in the battery based and portable devices because of its low power features and its competitive delay. The Residue number system reverse converter is designed with parallel prefix addition by using new components methodology for higher speed operation. The RNS consists of two main components forward and the reverse converter that are integrated with the existing digital system[5]. The forward converter performs the operation of converting the binary number to the modulo number whereas the reverse converter performs the operation of reverse converting the modulo number to the binary number which is the hard and time consuming process compared with the forward converter[3]. The fundamental RNS concepts such as 1)RNS definition with properties and their applications,2)consideration of modulo set selection,3)design of forward converter,4)modulo arithmetic units,5)design of reverse converter are discussed[2].

The voltage over scaling (VOS) technique is applied to the residue number system to achieve high energy efficiency [7]. The VOS technique introduces soft errors which degrades the performance of the system. To overcome these soft errors a new technique is implemented called joint RNS-RPR which is the combination of RNS and the reduced precision redundancy. This method provides the advantage of satisfying the basic properties of RNS includes shorter critical path, reduced complexity and low power. New

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architectures are presented for the moduli set (2n-1,2n, 2n+1) for the conversion from the residue to the binary equivalents. Here the speed and the cost are major concern[9.10].

Distributed arithmetic principles are used to perform the inner product computation[8]. The input data which are in the residue domain which are encoded using the Thermometer code format and the outputs are encoded using the one hot code format. Compared to the conventional method which used Binary code format, the proposed system which achieves higher operating speed. The residue number system which provides carry free addition and fully arithmetic operation, for several applications such as digital signal processing and cryptography.

In this brief, we present a comprehensive method which uses the parallel prefix adder in selected position, thereby using the shift operation on one bit left to design a multiplier on the same design module to achieve a fast reverse converter design. The usage on parallel prefix structure in the design leads to higher speed in operation meanwhile it increases the area and power consumption. In order to compensate the tradeoff between the speed, area and power consumption, a novel specific hybrid parallel prefix based adder components are used to design the reverse converter.

## II. LITERATURE REVIEW

To design a converter that may be either forward or reverse contain specific procedures. The airthematic units are the prime concern in the residue based digital systems. To make efficient design of reverse converter we have to follow the procedures. The reverse converter design efficiency will depend on the two factors are selection algorithm, selection of moduli set. The proper selection these two factors will yields the efficient design of reverse converter since its design has complex and non modular architecture. Still the selection of hardwares resources used in the converters will affect the performance of the reverse converter. The modulo adders are the conventional resources that are using in reverse converters. The modulo ripple carry adder will have simple structure yet affects from longer propagation delay whenever number of bits are growing for the inputs. The modulo parallel prefix adder will compute carries initially based on set of prefix networks even though having high speed lagging in area due to long prefix networks which causes area. The converters that are designed based on this adders will also be inefficient as like as them. To avoid all these drawbacks we are designing anew converters that is also based on the prefix adders with slight changes to them which makes area efficient without affecting the speed performance. The proposed adders are efficient hence the new converters will also have sufficient trade off between the area and speed. The new adder architectures are presented in subsequent chapters. Parallel-prefix adders with its high-speed feature have been used in the RNS modular arithmetic channels. This performance gain is due to parallel carry computation structures, which is based on different algorithms. Each of these structures has distinct characteristics, such as Sklansky (SK), and Kogge–Stone (KS) as they have the maximum and minimum fan-out, respectively, both providing minimal logic depth. Minimum fan-out comes at the expense of more circuit area [18]. Therefore, hardware components selection should be undertaken carefully.

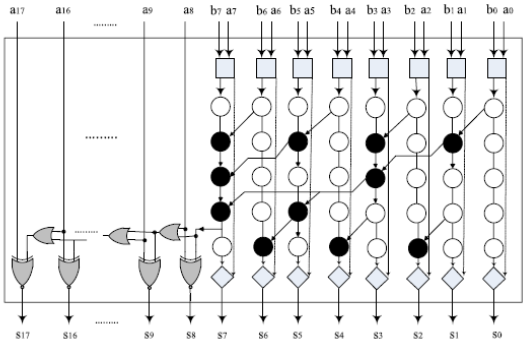


**Fig.1: PPX structure.**

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## III. PROPOSED NOVEL COMPONENTS

The First proposed reverse converter with large dynamic range is Ripple carry adder based reverse converter. It suffers from the delay whenever there is increase in the number of residues that should perform addition which affects the speed of the design[1]. To improve its speed high speed parallel prefix adders will be employed, they consist more prefix networks to compute the carry which makes less efficient area. The number of prefix networks will increase logarithmically when the number of bits that are to be added are growing. We already discussed that reverse converter algorithm will composed of certain number of addition. Each and every adder has to be carefully designed. The addition that was coming at the final stage in the algorithm will plays vital m role on performance of converter. That parameters will impact on whole algorithm. The adder used at the final stage of conversion will have usually two inputs. One of input contain 4n+1 bits. The second will contain 2n+1 bits. To make the second operand as 4n+1 bits we will add constant 2n+1 bits to the second operand which accomplishes the addition. Such that we don't need any extra prefix network to the addition MSB 2n+1 bits in the two operands. At this step we are reducing the size of prefix networks to half such as 4n+1 adder will may contain only 2n+1 prefix networks. The remaining biot addition will be accomplished as per lemma shown below Lemma: According to this the between two of the operands that are applying to final stage adder will have 2n+1 constant bits and they are equal to 1. In the final stage of algorithm we actually perform subtraction between the operands that are applying to it. To perform this we actually need a subtarctor. We are using an adder that to perform subtraction to make it possible we have to convert one of the operand in 2's complement form.

## IV. NEW PARALLEL-PREFIX BASED COMPONENTS

The HMPE Structure consists of two parts: Regular prefix adder and the Modified Excess One unit. The first two operands are added using the parallel prefix adder and the result is conditionally incremented based on the control signal generated by the prefix structure to assure the single zero representation. The below figure shows HMPE Structure.

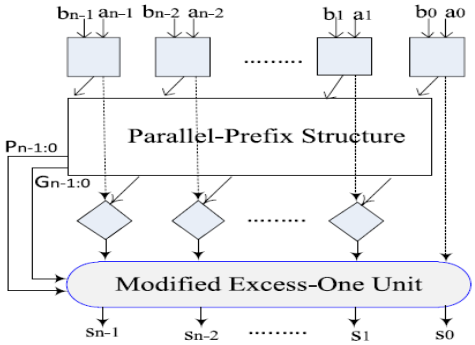


**Fig 2 HRPX Module**

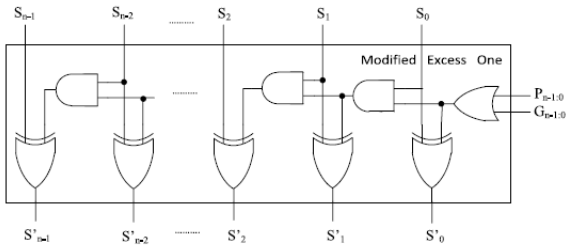


**Fig 3 Modified Excess one unit**

The Reverse converters which are designed with RCA already have discussed that having the effect when there is the growth in number of residues which complicates the speed. To improve the performance introduced parallel prefix adders which in turns increase the speed but when number of operands is increasing, there is a logarithmic growth in the number of prefix levels computation which in turn increases the area and power. The reverse converter normally several adders and in the one is prominent which required at the last stage in the converter used for binary representation. The adders which are usually have large number of bits, this adders parameters and performance will shows major effect on the whole converter performance. This should be

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carefully designed. We can keep one of the operand applying for this adder is as constant such that decrease the computation effect of this class of converter. We may deduce one lemma Lemma: this proposes that one of the operand that is applying for the CPA4in the converter is always constant and that equals to one's which are of 2n+1 bits

Fig.3 shows the Modified Excess One unit circuit diagram. The result generated by the prefix structure is conditionally incremented by this unit based on the control signal generated by the parallel prefix adder.

The reverse converter design is implemented for (4n+1) modulo addition (n=5) designing the adder and also the multiplier by using the same adder design without using any parallel prefix multiplier structure for designing multiplier.

In this design, the adder design is implemented by using the Kogge Stone adder parallel prefix structure. Here the first two operands are added by using the prefix adder preprocessing stage thereby generating the propagate and generate equation. The first stage processed signal get passed to the next stage called the prefix carry tree, this stage again computes the generate and propagate equation by using the previous output and all the logic cells employed in the Kogge Stone adder network. These processed signals are passed to the post processing block.

## V. RESULTS

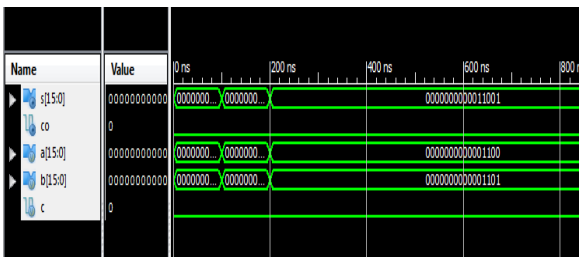


**Fig 4 Simulation Result**

| | DELAY | AREA | POWER |
|---|---|---|---|
| HMPE | 16.662 | 34.61 | 344 |
| KOGGESTONE | 15.682 | 64.111 | 345 |
| SPRING | 19.115 | 22.39 | 481 |
| SPARSEKOGGE | 15.502 | 32.57 | 482 |
| RCA | 21.690 | 18.32 | 352 |

**Fig 5 Table of Different Adders**

## VI. CONCLUSION

The reverse converter which actually used in conversion of numbers from residues to binary values. This is actually used in residue based airthematic devices where residue number system has vital role. Since the residue number system will increase the speed of processing due to carry free addition, borrow free subtraction and parallel pipelining. These are the advantages that make residue number system effective. The proposed converter will be designed to reduce the delay caused by RCA and large area caused by parallel prefix adder due to more number of stages. The HRPX and HMPE are the modules that are designed to achieve less are and speed trade off. The HRPX and HMPE initially designed and verified then remaining modules are designed all modules are Connected to -gether to perform reverse conversion. The designing is achieved through the Verilog HDL, then they are synthesized and simulated in Xilinx 13.2 i. The results are proving that it s having good tradeoff between area and speed.

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