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Design of Low Power, High Performance 2-4 and 4-16 Mixed-Logic Line Decoders

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Abstract:
This paper introduces a mixed-logic design method for line decoders, combining transmission gate logic, pass transistor dual-value logic and static CMOS. Two novel topologies are presented for the 2-4 decoder: a 14-transistor topology aiming on minimizing transistor count and power dissipation and a 15-transistor topology aiming on high power- delay performance. Both a normal and an inverting decoder are implemented in each case, yielding a total of four new designs. Furthermore, four new 4-16 decoders are designed, by using mixed-logic 2-4 predecoders combined with standard CMOS post-decoder. All proposed decoders have full swinging capability and reduced transistor count compared to their conventional CMOS counterparts. Finally, a variety of comparative spice simulations at the 32 nm shows that the proposed circuits present a significant improvement in power and delay, outperforming CMOS in almost allcases.

Index Terms:
line decoder, mixed-logic, power-delay optimization.

I. INTRODUCTION:

Static CMOS circuits are used for the vast majority of logic gates in integrated circuits [1]. They consist of complementary nMOS pull down and pMOSpullupnetworksandpresentgoodperformanceaswellasresistancetonoiseand device variation.

Therefore, CMOS logic is characterized by robustness against voltage scaling and transistor sizing and thus reliable operation at low voltages and small transistor sizes [2]. Input signals are connected to transistor gates only, offering reduced design complexity and facilitation of cell-based logic synthesis and design. Pass-transistor logic was mainly developed in the 1990s, when various design styles were introduced [3-6], aiming to provide a viable alternative to CMOS logic and improve speed, power and area. Its main design difference is that inputs are applied to both the gates and the source/drain diffusion terminals of transistors. Pass transistor circuits are implemented with either individual nMOS/pMOS pass transistors or parallel pairs of nMOS and pMOS called transmission gates.

This work develops a mixed-logic design methodology for line decoders, combining gates of different logic to the same circuit, in an effort to obtain improved performance compared to single-style design. Line decoders are fundamental circuits, widely used in the peripheral circuitry of memory arrays (e.g. SRAM), multiplexing structures, implementation of boolean logic functions and other applications. Despite their importance, a relatively small amount of literature is dedicated to their optimization, with some recent work including [7-9]. The rest of this paper is organized as follows: Section II provides a brief overview of the examined decoder circuits, including logic characterization and implementation with conventional CMOS circuitry.

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Section III introduces and describes the new mixed-logic designs. Section IV conducts a comparative study among the proposed and conventional decoders through proper simulation, with a detailed discussion on the derived results. Section V provides the summary and final conclusions of the work presented.

II. OVERVIEW OF LINE DECODERCIRCUITS:

In digital systems, discrete quantities of information are represented by binary codes. An n-bit binary code can represent up to 2^n distinct elements of coded data. A decoder is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines or fewer, if the n-bit coded information has unused combinations. The circuits examined in this work are called n-to-m line decoders, and their purpose is to generate the $m = 2^n$ minterms of n input variables.

A. 2-4 Line Decoder:

A 2-4 line decoder generates the 4 minterms D0-3 of 2 input variables A and B. Its logic operation is summarized in Table

I. Depending on the input combination, one of the 4 outputs is selected and set to 1 while the others are set to 0. An inverting 2-4 decoder generates the complementary minterms I0-3, thus the selected output is set to 0 and the rest are set to 1, as shown in TableII.

TABLEITRUTH TABLE OF2-4DECODER

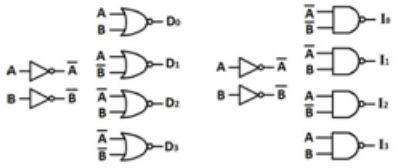
A	B	D_0	D_1	D_2	D_3
0	0	**1**	0	0	0
0	1	0	**1**	0	0
1	0	0	0	**1**	0
1	1	0	0	0	**1**

TABLEIITRUTH TABLE OF INV. 2-4DECODER:

A	B	I_0	I_1	I_2	I_3
0	0	**0**	1	1	1
0	1	1	**0**	1	1
1	0	1	1	**0**	1
1	1	1	1	1	**0**

In conventional CMOS design, NAND and NOR gates are preferred to AND and OR, since they can be implemented with 4 transistors, as opposed to 6, therefore implementing logic functions with higher efficiency.

A 2-4 decoder can be implemented with 20 transistors using 2 inverters and 4 NOR gates, as shown in Fig. 1(a). The corresponding inverting



(a) (b)

Fig. 1. 20-transistor 2-4 line decoders implemented with CMOS logic: (a) Non-inverting NOR-based decoder, (b) Inverting NAND-based decoder. Decoder can also be implemented with 20 transistors using 2 inverters and 4 NAND gates, as shown in Fig. 1(b).

B. 4-16 Line Decoder with 2-4Predecoders:

A 4-16 line decoder generates the 16 minterms D0-15 of 4 input variables A, B, C and D, and an inverting 4-16 line decoder generates the complementary minterms I0-15. A straightforward implementation of these circuits would require 16 4-input NOR and NAND gates. However, a more efficient design can be obtained using a predecoding technique, according to which blocks of n address bits can be predecoded into 1-of-2^n predecoded lines that serve as inputs to the final stage decoder [1]. With this technique, a 4-16 decoder can be implemented with 2 2-4 inverting decoders and 16 2-input NOR gates (Fig. 2(a)) and an inverting one can be

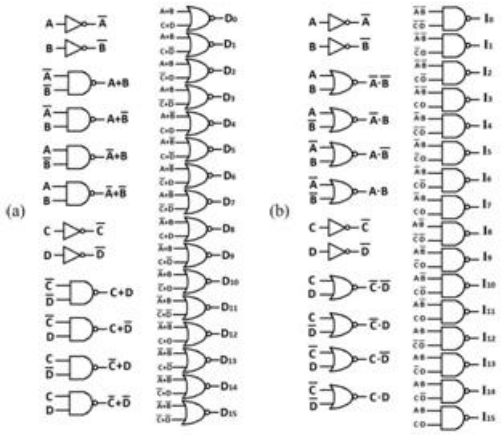


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Fig. 2. 104-transistor 4-16 line decoders implemented with CMOS logic and predecoding: (a) Non-inverting decoder implemented with two 2-4 inverting predecoders and a NOR-based post-decoder, (b) Inverting decoder implemented with two 2-4 non-inverting predecoders and a NAND-based post- decoder.

Implemented with 2 2-4 decoders and 16 2-input NAND gates (Fig. 2(b)). In CMOS logic, these designs require 8 inverters and 24 4-input gates, yielding a total of 104 transistors each.

III. NEW MIXED-LOGICDESIGNS:

In combinational logic, transmission gates have mostly been used in XOR-based circuits such as full adders and as the basic switch element in multiplexers. However, we consider their use in the implementation of AND/OR logic, as demonstrated in [5], which can be efficiently applied in line decoders. The 2-input TGL AND/OR gates are shown in Fig. 3(a) and 3(b), respectively. They are full-swinging, but not restoring for all input combinations. Regarding pass-transistor logic, there are two main circuit styles: those that use nMOS only pass-transistor circuits, like CPL [3] and those that use both nMOS and pMOS pass- transistors, like DPL [4] and DVL [6]. The style we consider in this work is DVL, which offers an improvement on DPL, preserving its full swing operation with reduced transistor count[10].The2-inputDVLAND/OR gates are shown in Fig. 3(c) and 3(d), respectively. Similar to the TGL gates, they are full-swinging but non-restoring. Assuming that complementary inputs are available, the TGL/DVL gates require only 3 transistors, as opposed to the 4 required in CMOS NAND/NOR gates. Decoders are high fan-

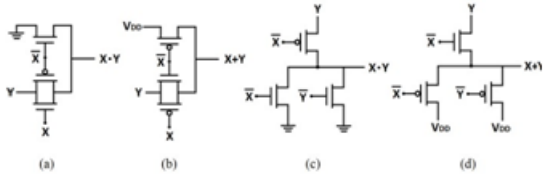

Fig. 3. The 3-transistor AND/OR gates considered in this work (a) TGL AND gate, (b) TGL OR gate, (c) DVL AND gate, (d) DVL OR gate.

Out circuits, where few inverters can be used by multiple gates, thus using the TGL/DVL gates can result to reduced transistor count. An important common characteristic of these gates is their asymmetric nature, ie the fact that they do not have balanced input loads. As shown in Fig. 3, we labeled the 2 gate inputs X and Y. In TGL gates, input X controls the gate terminals of all 3 transistors, while input Y propagates to the output node through the transmission gate. In DVL gates, input X controls 2 transistor gate terminals, while input Y controls 1 gate terminal and propagates through a pass transistor to the output. We will refer to X and Y inputs as the control signal and the propagate signal of the gate, respectively. This asymmetric feature gives a designer the flexibility to perform signal arrangement, ie choosing which input is used as control and which as propagate signal in each gate. Having a complementary input as propagate signal is not a good practice, since the inverter added to the propagation path increases delay significantly. Therefore, when implementing the inhibition (A'B) or implication (A'+B) function, it is more efficient to choose the inverted variable as control signal. When implementing the AND (AB) or OR (A+B) function, either choice is equally efficient. Finally, when implementing the NAND (A'+B') or NOR (A'B') function, either choice results to a complementary propagate signal,perforce.

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A. The 14-transistor 2-4 Low-Power Topology:

Designing a 2-4 line decoder with either TGL or DVL gates would require a total of 16 transistors (12 for AND/OR gates and 4 for inverters). However, by mixing both AND gate types into the same topology and using proper signal arrangement, it is possible to eliminate one of the two inverters, therefore reducing the total transistor count to 14. Let us assume that, out of the two inputs, namely A and B, we aim to eliminate the B inverter from the circuit. The D_0 minterm (A'B') is implemented with a DVL gate, where A is used as propagate signal. The D_1 minterm (AB') is implemented with a TGL gate, where B is used as propagate signal. The D2 minterm (A'B) is implemented with a DVL gate, where A is used as propagate signal. Finally, The D_3 minterm (AB) is implemented with a TGL gate, where B is used as propagate signal. These particular choices completely avert the use of the complementary B signal, therefore the Binverter can be eliminated from the circuit resulting in a 14- transistor topology (9 nMOS, 5 pMOS).

Following a similar procedure with OR gates, a 2-4 inverting line decoder can be implemented with 14 transistors (5 nMOS, 9 pMOS), as well: I_0, I_2 are implemented with TGL (using B as propagate signal) and I_1, I_3 are implemented with DVL (using A as propagate signal). The B inverter can once again beelided.The inverter elimination reduces transistor count, logical effort and overall switching activity of the circuits, thereby minimizing power dissipation. As far as the authors are concerned, 14 is the minimum number of transistors required to realize a full-swinging 2-4 line decoder with static (non-clocked) logic. The two new topologies are named '2-4LP' and '2-4LPI', where 'LP' stands for 'low power' and 'I' for 'inverting'. Their schematics are shown in Fig. 4(a) and Fig. 4(b),respectively.

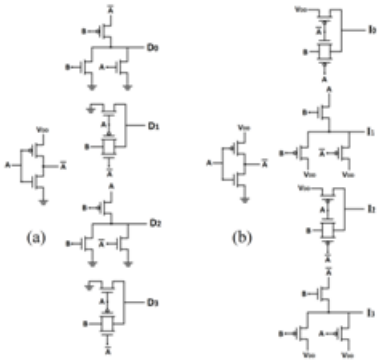

Fig. 4. New 14-transistor 2-4 line decoders: (a) 2-4LP (b) 2-4LPI.

B. The 15-transistor 2-4 High-Performance Topology:

The low-power topologies presented above have a drawback regarding worst case delay, which comes from the use of complementary A as the propagate signal in the case of D0 and I3. However, realizing D0 and I3 can be implemented more efficiently by using standard CMOS gates, since there is no need for complementary signals. Specifically, D0 can be implemented with a CMOS NOR gate and I3 with a CMOS NAND gate, adding one transistor to each topology. The new designs resulting from this modification mix 3 different types of logic into the same circuit and present a significant improvement in delay while only slightly increasing power dissipation.

They are named '2-4HP' (9 nMOS, 6 pMOS) and '2-4HPI' (6 nMOS, 9 pMOS), where 'HP' stands for 'high performance' and 'I' for 'inverting'. The reasoning behind the 'HP' designation is that these decoders present both low power and low delay characteristics, therefore achieving an overall good performance. The 2-4HP and 2-4HPI schematics are shown in Fig. 5(a) and Fig. 5(b), respectively, where the additional transistors are highlighted for easierdistinction.

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C. Integration in 4-16 Line Decoders:

At a small scale, circuits based on pass transistor logic can realize logic functions with fewer transistors and improved performance compared to static CMOS. However, cascading several non-restoring circuits causes a rapid degradation inperformance. A mixed-topology approach, ie alternating restoring and non-restoring levels of logic, can potentially

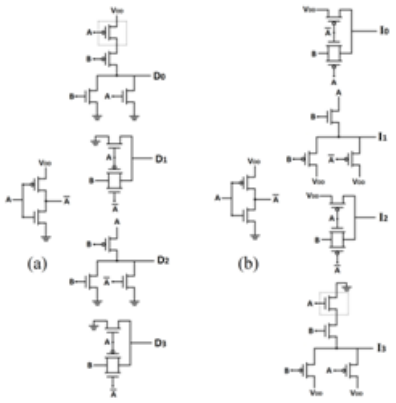

Fig. 5. New 15-transistor 2-4 line decoders: (a) 2-4HP (b) 2-4HPI. deliver optimum results, combining the positive characterists of both.

Adopting this design methodology, and with respect to the theory presented on section II, we implemented four 4-16 decoders by using the four new 2-4 as predecoders in conjunction with CMOS NOR/NAND gates to produce the decoded outputs. The new topologies derived from this combination are: 4-16LP (Fig. 6(a)), which combines two 2- 4LPI predecoders with a NOR-based post-decoder, 4-16HP (Fig. 6(b)), which combines two 2-4HPI predecoders with a NOR-based post-decoder, 4-16LPI (Fig. 6(c)), which combines two 2-4LP predecoders with a NAND-based post- decoder and, finally, 4-16HPI (Fig. 6(d)), which combines two 2-4HP predecoders with a NAND-based post-decoder.

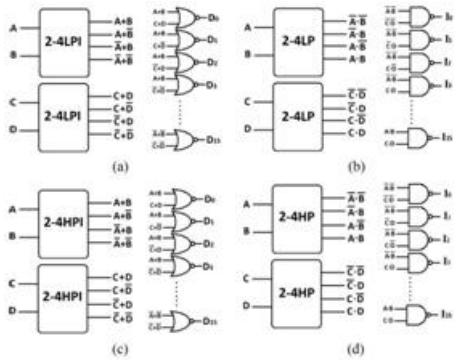

Fig. 6. New 4-16 line decoders: (a) 4-16LP, (b) 4-16LPI, (c) 4-16HP, (d) 4- 16HPI. The 'LP' topologies have a total of 92 transistors, while the 'HP' ones have 94, as opposed to the 104 transistors required by the pure CMOS implementation.

IV.SIMULATION RESULTS:

All the simulations are performed on Microwind and DSCH. The main focus of this work is to meet all challenges faces in designing of Decoder circuit using mixed logic.This work develops a mixed-logic design methodology for line decoders, combining gates of different logic to the same circuit, in an effort to obtain improved performance compared to single-style design. The simulation results are shown below figures.

Table:1 Comparisons results of mixed-logic line decoders

DESIGN	PARAMETERS	
	NO.OF TRANSISTORS	POWER
2to4 Decoder CMOS	6T	7.315uw
2to4 Decoder Mixed Logic	8T	6.647uw
4to16 Decoder CMOS	6T	7.315uw
4to16Decoder Mixed Logic	8T	6.647uw

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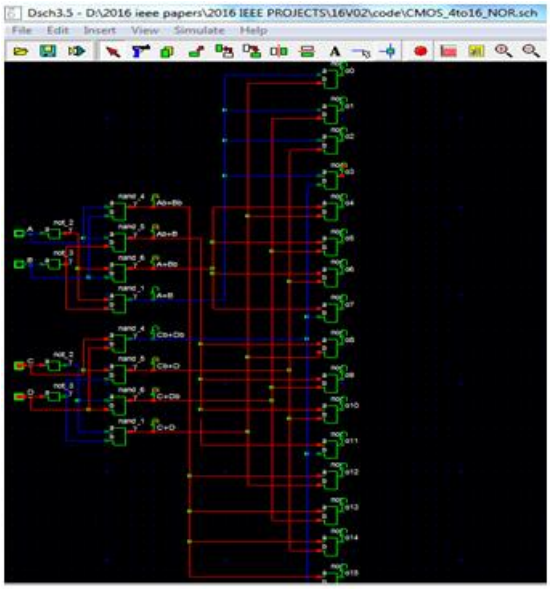

Fig 7: Schematic of 4to16 Decoder Using CMOS

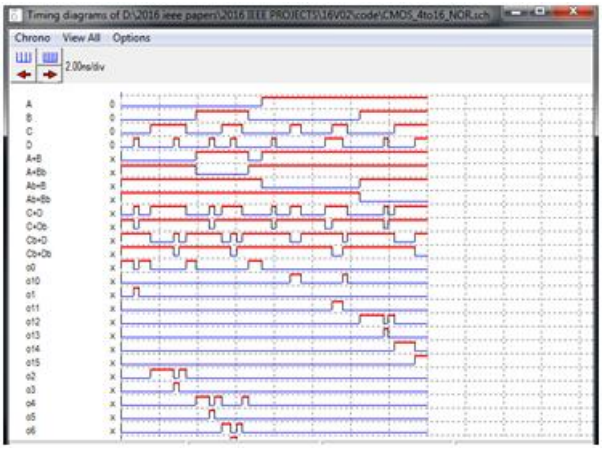

Fig 8: Timing Diagram of 4to16 Decoder Using CMOS

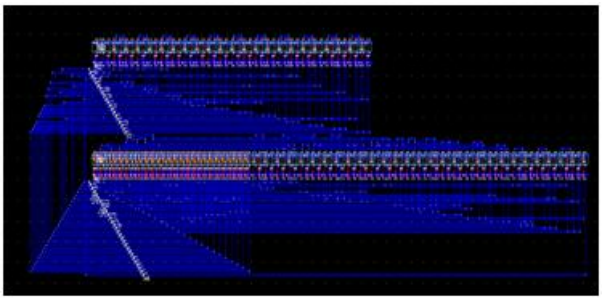

Fig 9: Layout of 4to16 Decoder Using CMOS

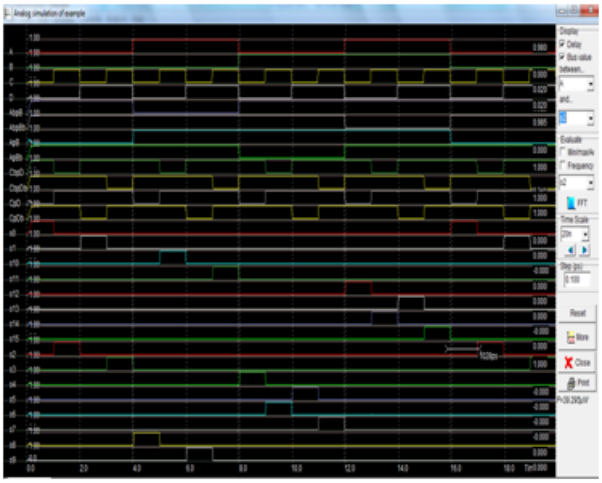

Fig 10: Simulation of Layout of 4to16 Decoder Using CMOS

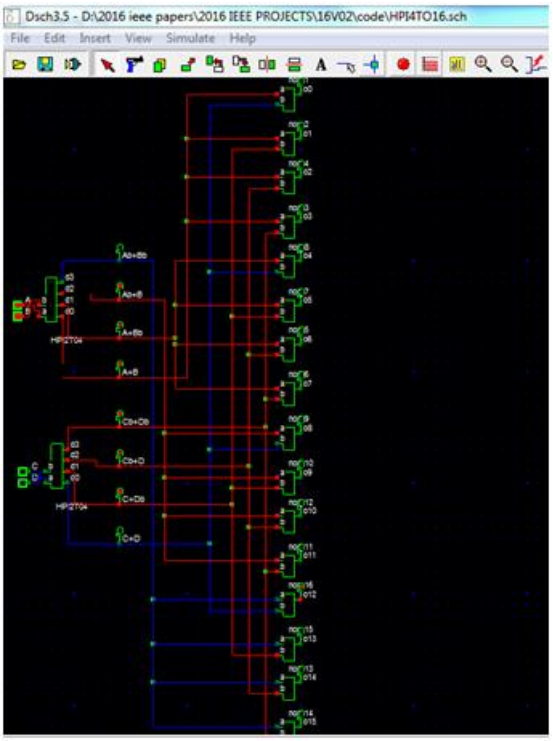

Fig 11: Schematic of 4to16 Decoder Using HPI

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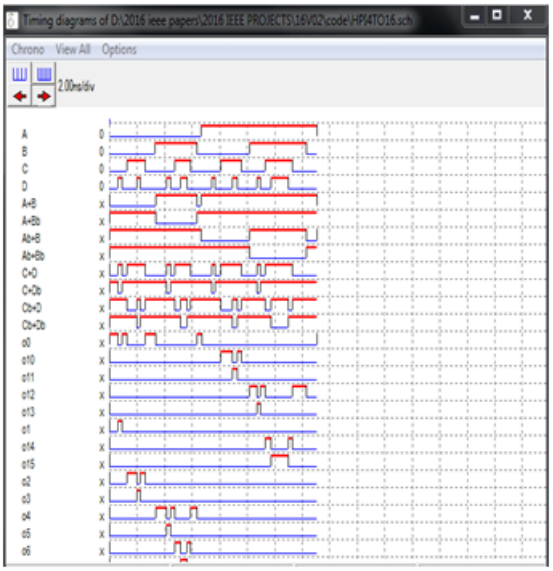

Fig 12: Timing Diagram of 4to16 Decoder Using HPI

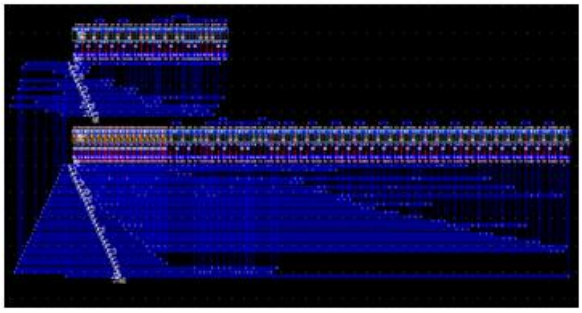

Fig 13: Layout of 4to16 Decoder Using HPI

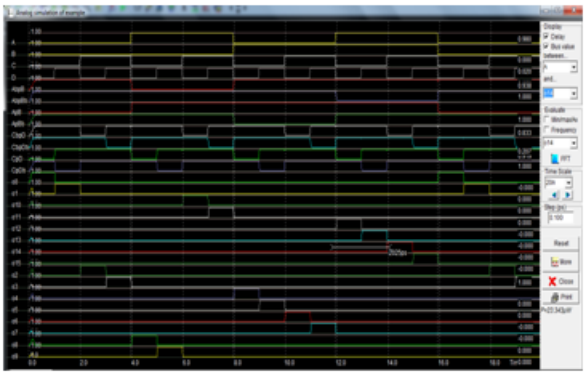

Fig 14: Simulation of Layout of 4to16 Decoder Using HPI

IV. CONCLUSIONS:

This paper introduced an efficient mixed-logic design for decoder circuits, combining TGL, DVL and static CMOS. By using this methodology, we developed four new 2-4 line decoder topologies, namely 2-4LP, 2-4LPI, 2-4HP and 2- 4HPI, which offer reduced transistor count (therefore potentially smaller layout area) and improved power-delay performance in relation to conventional CMOS decoders. Furthermore, four new 4-16 line decoder topologies were presented, namely 4-16LP, 4-16LPI, 4-16HP and 4-16HPI, realized by using the mixed-logic 2-4 decoders as predecoding circuits and combining them with post-decoders implemented in static CMOS logic. These designs combine the improved performance characteristics of pass transistor logic with the restoring capability of static CMOS. A variety of comparative spice simulations was performed at the 32 nm, verifying, in most cases, a definite advantage in favor of the proposed designs.

The 2-4LP and 4-16LPI topologies are mostly suitable for applications where area and power minimization is of primary concern. The 2-4LPI, 2-4HP and 2-4HPI, as well as the corresponding 4-16 topologies (4-16LP, 4-16HPI, 4-16HP), proved to be viable and all-around efficient designs, thus they can effectively be used as building blocks in the design of larger decoders, multiplexers and other combinational circuits of varying performance requirements. Moreover, the presented reduced transistor count and low power characteristics can benefit both bulk CMOS and SOI design as well. The obtained circuits are to be implemented on layout level, making them suitable for standard cell libraries and RTL design.

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