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A Quasi-Unipolar SPWM Full-Bridge Transformer less PV Grid-Connected Inverter with Constant Common-Mode Voltage

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Abstract:

The unipolar sinusoidal pulse width modulation (SPWM) full-bridge transformer less photovoltaic inverter with ac bypass brings low conduction loss and low leakage current. In order to better eliminate the leakage current induced by the common mode voltage, the clamping technology can be adopted to hold the common-mode voltage on a constant value in the freewheeling period. A full-bridge inverter topology with constant common-mode voltage (FB-CCV) has been derived and proposed in this paper, two unidirectional freewheeling branches are added into the ac side of the FB-CCV, and the split structure of the proposed freewheeling branches does not lead itself to the reverse-recovery issues for the freewheeling power switches and as such super junction MOSFETs can be utilized without any efficiency penalty. The passive clamping branches consist of a capacitor divider and two diodes, is added into the dc side of the FB-CCV, therefore, the weakness of active damping branch has been overcome, and the better clamping performance has been achieved in the freewheeling period. In the dead time between the main switches and the freewheeling switches, the anti parallel diodes of diagonal main switches of the FB-CCV form the freewheeling path to clamp the common-mode voltage at a constant value, and a quasi-unipolar SPWM strategy is presented.

Introduction:

In order to improve the common-mode performance of the unipolar SPWM full-bridge transformer less gridconnected inverter, a lot of in-depth research works, where the new freewheeling paths are constructed to C.Himabindu Assistant Professor, Dept of EEE, Chiranjeevi Reddy Institute of Engineering and Technology, Anantapur, AP, India.

separate the PV array from the grid in the freewheeling period, have been done in [22]–[31]. Several methods can be divided into the ac bypass [25]-[27] and the dc bypass [28]-[31]. The goal is to structure a simple, efficient, and reliable transformerless inverter topology for transformerless photovoltaic (PV) grid-connected application. Based on the common-mode equivalent model of the fullbridge inverter derived in [21], it is necessary that the potential of the freewheeling path is clamped to a half input voltage in the freewheeling period instead of only disconnecting the PV array from the grid. Depending on this rule, the switching frequency common-mode voltage can be completely avoided in the unipolar SPWM full-bridge inverter. The topologies in [27], [29], and [30], are complying with the aforementioned conclusion; however, their clamping ability is different. In [27] (the topology is shown in Fig. 1 (a), and is named as HB-ZVR), if the potential of the freewheeling path rises, it can be clamped, while if the potential falls, it cannot be clamped. In [29], Gonzalez et al. have brought a diode clamping branch into the input voltage side (shown in Fig. 1 (b), named as H6 in this paper), and the potential of the freewheeling path can be seamlessly clamped to a constant voltage in the freewheeling period. In [30], when the potential of the freewheeling path falls, it can be seamlessly clamped, however, when the potential rises, it is not clamped effectively during the dead time between the high frequency main switch and the clamping one. Apparently, the leakage current suppression performance in these three kinds of topologies is different due to the clamping ability. The H6 topology has the best performance about leakage current suppression in existing single-phase



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full-bridge transformerless topologies [30]. The losses of power devices in the topologies that are illustrated in [25], [29], and [30] have been calculated in different switching frequencies in [20]. It can be seen that the conduction losses (including freewheeling losses) have a large proportion in the total losses; therefore, reducing the conduction losses is beneficial to improve the efficiency of the inverter continually. Referring to Fig. 1 (c), the topology in [25] (named as Heric) has the minimum conduction losses and the total losses, and the reason is that the output current flows through only two power switches in the power processing period and the freewheeling period, respectively. The output current of other topologies flows or 2) improve the conversion efficiency based on the H6 topology with the best leakage current suppression. This project focuses on improving the leakage current suppression performance of the Heric topology by using passive clamping technology, according to rule 1). First, a fullbridge inverter topology with constant common-mode voltage (FB-CCV) is proposed in this paper. Compared with the Heric topology [25], the freewheeling path is reconstructed in the ac side, and a passive clamping branch is added into the dc side to clamp the potential of the freewheeling path in the freewheeling period. Under the effect of the proposed modulation strategy, the inductor current flows through the antiparallel diodes of diagonal main switches of the FB-CCV during the dead time between the main switches and the freewheeling switches, and this stage is consistent with the freewheeling mode of the bipolar SPWM full-bridge inverter, which guarantees that the common-mode voltage is a constant value in the dead time. Until the end of the dead time, the freewheeling path starts to provide the zero-vector freewheeling, and this stage is same with the freewheelingmode of the unipolar SPWM fullbridge inverter. By running the combined operation modes, the common-mode voltage is held on a constant value in whole switching period. For convenience, the novel modulation strategy is named as quasi-unipolar SPWM (qSPWM).

2. STRUCTURE AND OPERATION PRINCIPLE: A. Construction of the FB-CCV:

In order to guarantee that the common-mode voltage of the Heric is on a constant value in the freewheeling period, the procedure of deriving the freewheeling branches and passive clamping branches will be demonstrated in the following how a Heric topology, as shown in Fig. 1 (c), can be transformed to a FB-CCV topology, as shown in Fig. 3 (a). 1) Step 1: First, the bidirectional freewheeling branches are extracted from the Heric topology, as shown in Fig. 2 (a). Separate the bidirectional branches to form two unidirectional branches shown in Fig. 2 (b). 2) Step 2: Next, the positions of S5 and D5 are exchanged in the unidirectional branch B, as shown in Fig. 2 (c). 3) Step 3: Finally, find or build a clamping voltage source in the full-bridge inverter [for example, point 3 in Fig. 2 (d)], then introduce two clamping diodes D7 and D8 into the inverter to connect the center points of the two unidirectional branches to the clamping voltage source. The direction of the clamping diodes can be determined using the back-to-back rule of D5 and D6, as shown in Fig. 2 (d). Remark: It should be mentioned that the freewheeling branches and passive clamping branches can be rearranged as bridge leg structure, as shown in Fig. 2 (e). We can define that S5 and S6 make up the active freewheeling leg, D5 and D6 make up the passive freewheeling leg, and D7 and D8 make up the passive clamping leg. According the aforementioned steps, the capacitors Cdc1 and Cdc2, in series, are introduced into the dc side of the Heric to build the clamping voltage source, and the freewheeling branches and passive clamping branches shown in Fig. 2 (d) are introduced into the Heric also. Finally, the FB-CCV topology is constructed, as shown in Fig. 3 (a). The drive signals of qSPWM are shown in Fig. 3 (b), and the key operation waveforms of the FB-CCV with qSPWM are shown in Fig. 3 (c), respectively. In the positive half period of the grid-in current, the operation style of S1 and S4 is in unipolar SPWM modulation, S2 and S3 are always OFF, and the switches S5 and S6 are complementary with the switches S1 and S4 with a dead time to avoid the



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short-circuit paths from S1, S5, D5, S4, and S1, S5, D7, respectively; in the negative half period of the grid-in current, the operation style of S2 and S3 is in unipolar SPWM modulation, S1 and S4 are always OFF, and the switches S5 and S6 are complementary with the switches S2 and S3 with a dead time to avoid the short-circuit paths from S3, D6, S6, S2, and D8, S6, S2,

Respectivel



Fig. 1. Typical transformerless inverter topologies. (a) HB-ZVR topology.(b) H6 topology. (c) Heric topology.

In the qSPWM style, there are two freewheeling modes in the freewheeling period. One is dead-time mode, such as the time intervals [t2, t3] and [t4, t5] in Fig. 3 (c); another is zero-vector mode, the time interval [t3, t4], as shown in Fig. 3 (c) also. Especially, the potential of the zero-vector freewheeling path is defined as the potential of points 1 and 2 as shown in Fig. 3 (a), and the zero-vector freewheeling path can be freely clamped to the midpoint of the input voltage (it is the point 3) through

the diodes D7 and D8 in the zero-vector freewheeling stage.



Fig. 2. Derivation of the freewheeling branches and passive clamping branches. (a) Bidirectional freewheeling branches. (b) Two unidirectional branches. (c) Two unidirectional branches. (d) Proposed freewheeling branches with passive clamping branches. (e) Bridge leg structure. (fig. 2 desires final 2-column-width).

B. Operation Principle Analysis:

Before analysis, the following assumptions are given: 1) all active power devices are ideal switches with antiparallel diodes, and the power diodes are also ideal diodes without parasitic parameters; and 2) the capacitance Cdc1 and Cdc2 of the dc filter are large enough to be treated as constant voltage sources. Fig. 3 (c) shows the key operation waveforms of the FB-CCV at the grid frequency scale; a grid period can be divided into four states, I (ug > 0 and iref > 0), II (ug < 0 and iref > 0), III (ug < 0 and iref < 0), and IV (ug > 0 and iref < 0), respectively. Because of the similarity, only the switching modes in the positive half period of the grid-in current are described in detail. In state I, there are three kinds of stages.

Stage I-1 [t1, t2]: Refer to Figs. 3(c) and 4(a). At t1, the main switches S1 and S4 are turned ON and other switches are OFF, and the inductor current iL = IL (t1). In this stage, the power flows from the PV side to the grid through S1, S4, and the filter. The inductor current iL increases linearly until t2, this stage is named as power mode

$$i_{\rm L}(t) - I_{\rm L}(t_1) = \frac{U_{\rm pv} - u_{\rm g}}{L}(t - t_1)$$
(1)
$$u_{\rm 10} = U_{\rm rev}$$
(2)



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Stage I-2 [t2, t3]: Refer to Fig. 4 (b). At t2, S1, and S4 are turned OFF, and then all switches are off. This stage is called as dead-time freewheeling mode. The inductor current iL flows into a dc bus capacitor through the antiparallel diodes D2 and D3. The inductor current iL reduces linearly under the effects of the PV voltage and the grid voltage

$$i_{\rm L}(t) - I_{\rm L}(t_2) = \frac{-U_{\rm pv} - u_{\rm g}}{L}(t - t_2)$$
(3)
$$u_{12} = -U_{\rm pv}.$$
(4)

Stage I-3 [t3, t4]: Refer to Fig. 4 (c). At t3, the freewheeling switches S5 and S6 are turned ON with the same commutation order, and the other switches are OFF. This stage is called as zero-vector freewheeling mode. The inductor current iL flows through the diode D6 and the switch S6. The inductor current iL reduces linearly under the effect of the grid voltage

$$i_{\rm L}(t) - I_{\rm L}(t_3) = \frac{-u_{\rm g}}{L}(t - t_3)$$
 (5)
 $u_{12} = 0.$ (6)

At t4 , S5 , and S6 are turned OFF, and then all switches are OFF, the inverter works at the dead-time freewheeling mode again (likes stage I-2). In state II, the grid voltage goes into negative half period, and the grid-in current still stays at positive direction. Stage II-1 [t11, t12]: At t11, the freewheeling switches S5 and S6 are turned ON, and other switches are OFF. The direction of the grid voltage is reversed, and the inductor current iL flows through the diode D6 and the switch S6, is linearly increased under the effect of the grid voltage (Fig. 4 (c) can be referred as the equivalent circuit, but the bottom of the symbol of the grid is positive direction). This stage is called as the energy storage mode

$$i_{\rm L}(t) - I_{\rm L}(t_{11}) = \frac{|U_{\rm g}|}{L}(t - t_{11})$$
(7)
$$u_{12} = 0.$$
(8)



Fig. 3. Proposed transformerless PV grid-connected inverter. (a) FB-CCV topology. (b) Gate drive signal of the qSPWM with unity power factor. (c) Key operation waveforms of the FB-CCV with





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Fig. 4. Equivalent circuits in the positive half period of the grid-in current. (a) Stage 1 [t1 , t2]. (b) Stage 2 [t2 , t3]. (c) Stage 3 [t3 , t4].

Stage II-2 [t12, t13]: At t12, S5, and S6 are turned OFF, and then all switches are OFF. The inductor current iL flows into the dc bus capacitor through the antiparallel diodes D2 and D3, from the grid. The inductor current iL reduces linearly under the effect of the difference of the PV voltage and grid voltage



Fig. 5. Equivalent circuits in the clamped mode. (a) The potential of the zero vector freewheeling path falls. (b) The potential of the zero-vector freewheeling path rises.

$$u_{12} = -U_{\rm pv}.$$
 (10)

SStage II-3 [t13, t14]:S At t13, the main switches S1 and S4 are turned ON and other switches are OFF. In this stage, the energy is stored in filter inductors through S1, and S4. The inductor current iL is increased linearly until t14

$$i_{\rm L}(t) - I_{\rm L}(t_{13}) = \frac{U_{\rm pv} + |U_{\rm g}|}{L}(t - t_{13})$$
(11)
$$u_{12} = U_{\rm pv}.$$
(12)

From the aforementioned analysis, we can see that the auxiliary switches S5 and S6 run at high-frequency switching pattern. This makes it possible to have a reactive power flow that can be used to support the grid with additional services any time during the functioning of the inverter.

C. Operation Principle of the Clamping Branch:

The equivalent circuits of the clamping mode are shown in Fig. 5. In the positive half period of the gridin current, the path of the grid current (i.e., the differential-mode current iDM) is D6, S6, filter, grid lines, and back to D6, in sequence. If the potential of the freewheeling path falls, the commonmode current flows through D8, and the blue arrow represents the direction of the common-mode current iCM, as shown I Fig. 5 (a); when the potential of the freewheeling path rises, the common-mode current flows through D7, and the blue arrow represents the direction of the common-mode current iCM, as shown in Fig. 5 (b). Obviously, in both cases, the potential of the freewheeling path can be freely clamped to 0.5^* UPV. In the negative half period of the grid-in current, the clamping process is similar with the positive half period.



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3.Simulation Modelling Of Quasi-Unipolar Spwm Full Bridge Transformerless Topology:



Fig: Proposed transformerless PV grid-connected inverter. (a) FB-CCV topology



Fig: Proposed converter outputs a)Voltage b) filtered voltage c)current

4.Simulation Modelling Of Quasi-Unipolar Spwm Full Bridge Transformerless With Constant Common Mode Voltage Topology:



Fig: Simulation circuits in the clamped mode.



Fig: Quasi-unipolar spwm full bridge transformerless with constant common mode voltage topology outputs a)Voltage b) filtered voltage c)current

4. CONCLUSION AND FUTURE SCOPE:

A QSPWM full-bridge inverter topology with two unidirectional freewheeling braches and a passive clamping branch has been proposed in this paper. The proposed inverter has the following characteristics:

1)The QSPWM differential-mode voltage is a combination of unipolar and bipolar SPWM, and is more close to the unipolar SPWM.

2)There are two operation modes in the freewheeling period: the dead-time freewheeling mode and zerovector freewheeling mode, which guarantee that the high-frequency common-mode voltage is on a constant value in whole switching period.

3)The freewheeling paths have two kinds of combinations: MOSFET + diode, or full MOSFETs; meanwhile, the full MOSFETs type freewheeling path can reduce the conduction loss further. The proposed inverter is an optimized topology with high conversion efficiency and low leakage current.

These merits are verified and compared by a universal simulation models. It can be concluded that the proposed topology is extremely suitable for transformerless single-phase grid-connected inverter with lower switching frequency.

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