ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Design and Original of a Reversible Gates and Its Applications

Kasimbee Shaik
M.Tech (DSCE)

ABSTRACT:
The process of developing of the use in operations of computers. The originates great success in the last a period of ten years. But the ongoing miniaturization of integrated circuits will reach its limits in the near future. Make a smaller in size transistor and power dissipation is the major constraints in the development of smaller and consisting of many different and connected parts in circuits. Reversible logic provides an alternative that may overcome many of these problems in the future. For low-power design, reversible logic gates are very much in demand for the future computing technologies as they are known to produce zero power dissipation under ideal conditions. This paper proposes design of reversible logic gate and some of its applications. The quantum cost of a reversible logic circuit can be minimized by reducing the number of reversible logic gates. It can be helps to determine outputs from the inputs.

Keywords: Reversible Logic Circuits, Multiplexer.

I. INTRODUCTION:

Reversible logic has received great attention in the recent years due to their ability to reduce the power dissipation which is the main requirement in low power VLSI design. Quantum computers are constructed using reversible logic circuits. It has wide applications in low power CMOS and Optical information processing, DNA computing, quantum computation and nanotechnology [1]. In 1960 RLandauer demonstrated that high technology circuits and systems constructed using irreversible hardware result in energy dissipation due to information loss. According to Landauer's principle, the loss of one bit of information dissipates KTln2 joules of energy where K is the Boltzmann's constant and T is the absolute temperature at which the operation is performed.

The heat generated due to the loss of one bit of information is very small at room temperature but when the number of bits is more as in the case of high speed computational works the heat dissipated by them will be so large that it affects the performance and results in the reduction of lifetime of the components. Showed that one can avoid of energy dissipation constructing circuits using reversible logic gates. Reversibility in computing implies that no information about the computational states can ever be lost, so we can recover any earlier stage by computing backwards or un-computing the results. This is termed as logical reversibility. The benefits of logical reversibility can be gained only after employing physical reversibility [2]. Physical reversibility is a process that dissipates no energy to heat. Absolutely perfect physical reversibility is practically unachievable. Computing systems give off heat when voltage levels change from positive to negative: bits from zero to one.

Most of the energy needed to make that change is given off in the form of heat. Rather than changing voltages to new levels, reversible circuit elements will gradually move charge from one node to the next. This way, one can only expect to lose a minute amount of energy on each transition. Reversible computing strongly affects digital logic designs. Reversible logic elements are needed to recover the state of inputs from the outputs. It will impact instruction sets and high-level programming languages as well. Eventually, these will also have to be reversible to provide optimal efficiency. High-performance chips releasing large amounts of heat impose practical limitation on how far can we improve the performance of the system.

Cite this article as: Kasimbee Shaik, "Design and Original of a Reversible Gates and Its Applications", International Journal & Magazine of Engineering, Technology, Management and Research, Volume 4 Issue 12, 2017, Page 225-228.

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Reversible circuits that conserve information, by uncomputing bits instead of throwing them away, will soon offer the only physically possible way to keep improving performance. Reversible computing will also lead to improvement in energy efficiency. Energy efficiency will fundamentally affect the speed of circuits such as nanocircuits and therefore the speed of most computing applications. To increase the portability of devices again reversible computing is required. It will let circuit element sizes to reduce to atomic size limits and hence devices will become more portable[3]. Although the hardware design costs incurred in near future may be high but the power cost and performance being more dominant than logic hardware cost in today's computing era, the need of reversible computing cannot be ignored.

II. LITERATURE SURVEY:

Reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and performance and it include the area like. Optical information processing. Quantum computation. High energy efficiency, speed or performance. The number of Reversible gates (N): The number of reversible gates used in circuit. This refers to the number of inputs that are to be maintained constant at either 0 or 1 in order to synthesize the given logical functions.

III. EXPERIMENTAL DESIGN

BASIC REVERSIBLE LOGIC GATES

FEYNMAN GATE:

Feynman gate is a 2*2 one of the reversible gate as shown in figure 1. The is inputs are (A, B) and the output are (P, Q). The outputs are defined by P=A, Q=A xorB.[5]

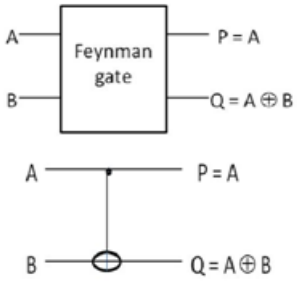

Fig.1: Feynman Gate

A	B	P	Q
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Truth table of Feynman gates

Examples of Feynman gate of truth table: if inputs are A that value 0 and B value is 1 then Q=A XOR B then outputs are Q=1 and P=0.

DOUBLE FEYNMAN GATE (F2G):

Fig. shows a 3*3 Double Feynman gate [7]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The outputs are defined by P = A, Q=A⊕B, R=A⊕C [4].

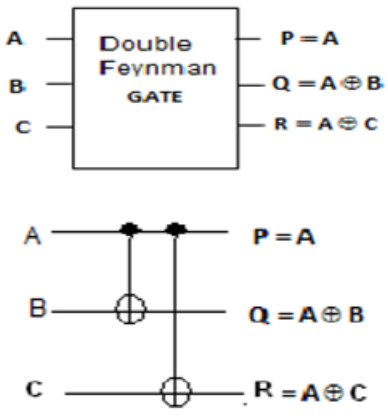

Fig.2: Double Feynman gate

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A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	0	0

Truth table of Double Feynman gates

Examples of Double Feynman gate of truth table: if Inputs are A that value 0 and B value is 1 and C value is 1 then Q=A XOR B then outputs are Q=1 and P=0, R=1.

FREDKIN GATE:

Fig shows a 3*3 Fredkin gate. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P=A, Q=A′B XOR AC and R=A′C XOR AB[5].

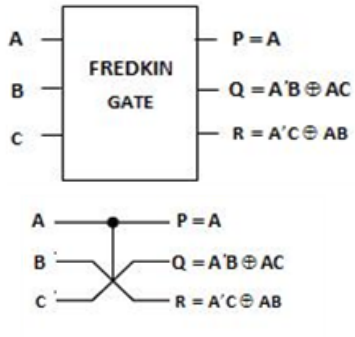

Fig.3: Fredkin gate

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Truth table of fredkin gate

HALF ADDER

The half adder and its truth table is shown in fig and table. The Halfadder using proposing in adder.

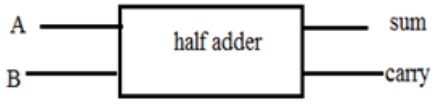

Fig.4: Block Diagram of Half Adder

Inputs are A and B outputs are sum and carry of the half adder.

Truth Table			
Input		Output	
A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

HALF SUBTRACTOR

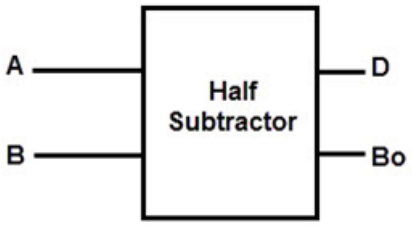

Fig.5: Diagram of Half Subtractor

A	B	D	B_0
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Truth table of Half Subtractor

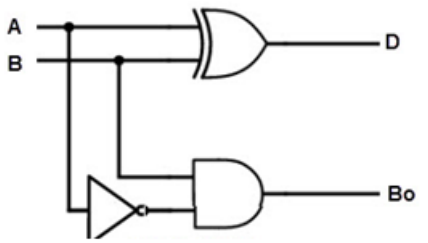

Fig.6: Logic circuit of Half Subtractor

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IV.SIMULATION RESULTS

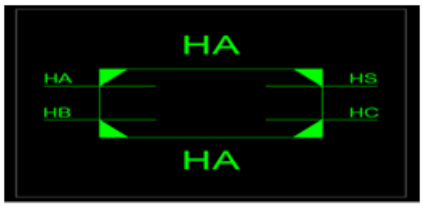

Fig.7: Schematic Diagram

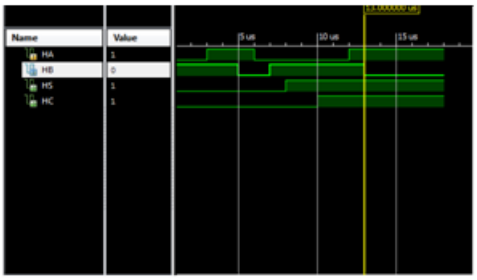

Fig.8: Output of the Half Adder

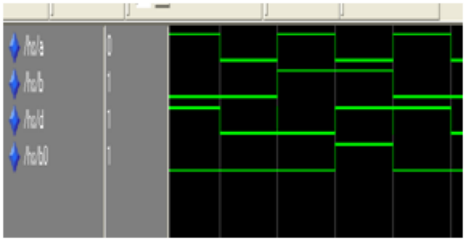

Fig.9: Output of the Half Subtractor

V. CONCLUSION:

We have presented an approach to the realize the multipurpose binary reversible gates. Such gates can be used in regular circuits realizing Boolean functions. In the same way it is possible to construct multiple-valued reversible gates having similar properties.

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