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Fault Coverage Circuit architecture using efficient Hardware for Testing Applications

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Abstract:
A new fault coverage test pattern generator using a linear feedback shift register (LFSR) called FC-LFSR can perform fault analysis and reduce the power of a circuit during test by generating three intermediate patterns between the random patterns by reducing the hardware utilization. The goal of having intermediate patterns is to reduce the transitional activities of Primary Inputs (PI) which eventually reduces the switching activities inside the Circuit under Test (CUT) and hence power consumption is also reduced without any penalty in the hardware resources. The experimental results for c17 benchmark, with and without fault confirm the fault coverage of the circuit being tested.

Keywords:
LFSR, Optimization, Low Power, Test Pattern Generation, BIST.

I. INTRODUCTION:
The main challenging areas in VLSI are performance, cost, power dissipation is due to switching i.e. the power consumed testing, due to short circuit current flow and charging of load area, reliability and power. The demand for portable computing devices and communications system are increasing rapidly. The applications require low power dissipation VLSI circuits. The power dissipation during test mode is 200% more than in normal mode. Hence the important aspect to optimize power during testing [1]. Power dissipation is a challenging problem for today‟s System-on-Chips (SoCs) design and test.

The power dissipation in CMOS technology is either static or dynamic. Static power dissipation is primarily due to the leakage currents and contribution to the total power dissipation is very small. The dominant factor in the power dissipation is the dynamic power which is consumed when the circuit nodes switch from 0 to 1. During switching, the power is consumed due to the short circuit current flow and the charging of load capacitances is given by equation:

$$P = 0.5VDD\ E\ (sw)\ CLFCLK \quad (1)$$

Where VDD is supply voltage, E(sw) is the average number of output transitions per 1/ FCLK, FCLK is the clock frequency and CL is the physical capacitance at the output of the gate. Dynamic power dissipation contributed to total power dissipation. From the equation dynamic power depends on three parameters: supply voltage, clock frequency and switching activity. To reduce the dynamic power dissipation by using first two parameters only at the expense of circuit performance. But power reduction using the switching activity doesn't degrade the performance of the circuit. Power dissipation during testing is one of most important issue. External testing using ATE has a serious disadvantage, since the ATE (control unit and memory) is extremely expensive and cost is expected to grow in the future as the number of chip pins increases [2].

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As the complexity of modern chips increases, external testing with ATE becomes extremely expensive. Instead, Built-In Self-Test (BIST) is becoming more common in the testing of digital VLSI circuits since overcomes the problems of external testing using ATE. BIST test patterns are not generated externally as in case of ATE. BIST perform self-testing and reducing dependence on an external ATE. BIST is a Design-for-Testability (DFT) technique makes the electrical testing of a chip easier, faster, more efficient and less costly. The important to choose the proper LFSR architecture for achieving appropriate fault coverage and consume less power. Every architecture consumes different power for same polynomial. In computing, a linear-feedback shift register (LFSR) is a shift register whose input bit is a linear function of its previous state [3]. The most commonly used linear function of single bits is exclusive-or (XOR). Thus, an LFSR is most often a shift register whose input bit is driven by the XOR of some bits of the overall shift register value. The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the stream of values produced by the register is completely determined by its current (or previous) state. Likewise, because the register has a finite number of possible states, it must eventually enter a repeating cycle [4]. However, an LFSR with a well-chosen feedback function can produce a sequence of bits which appears random and which has a very long cycle.

Applications of LFSR:

- Pattern generator,
- Low power testing,
- Data compression, and
- Pseudo Random Bit Sequences (PRBS).

II. LOW POWER TESTING SCHEMES:

Power dissipation has become a major design objective in many application areas, such as wireless communications and high performance computing, thus leading to the production of numerous low-power designs [5].

At the same time, power dissipation is also becoming a critical parameter during manufacturing test, as the design can consume much more power during test than during functional mode of operation. Because test throughput and manufacturing yield are often affected by test power, dedicated test methodologies have emerged over the past decade. These techniques can be broadly classified into those that apply during scan testing and those that apply during built-in self-test (BIST). A few of them are also applicable to test compression circuits or memory designs. Various authors reported on techniques to cope with power problems during testing. Existing low-power testing scheme is divided into the following two categories.

(A) Low - Power Testing Techniques for External Testing

(B) Low - Power Testing Techniques for Internal Testing

A. Low-Power Testing Techniques for External Testing

The category contains various techniques adopted to reduce the power consumption during external testing by ATE and depends on the number of transitions in test data set. A heuristic method to generate test sequences which create worst-case power droop by accumulating the high- and low-frequency effects using a dynamically constrained version of the classical D-algorithm for test generation. In high-speed circuits that process digital audio and video signals, the inputs to most of those modules change relatively slowly over time [6]. The low-power designers often take advantage of this fact when they determine the thermal and electrical limits of the circuit and system packaging requirements. In contrast, there is no definite correlation between successive test patterns generated by an ATPG tool during scan testing or produced by a pseudorandom pattern generator (PRPG) during logic BIST. As power dissipation in CMOS circuits is proportional to switching activity, this excessive switching activity during test can cause catastrophic problems, such as instant circuit damage,

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test-induced yield loss due to noise phenomena, reduced reliability, product cost increase, or reduced autonomy for battery-operated devices. The test compaction algorithm further reduces the number of test patterns as well as the average capture power. The idea is to identify an input control pattern such that, by applying that pattern to the primary inputs of the circuit during the scan operation, the switching activity in the combinational part can be minimized or even eliminated. The basic idea of input control technique with existing vector- or latch-ordering techniques that reduces the power consumption has been covered technique of gating partial set of scan cells. Minimizing power consumption during functional operation and during manufacturing tests has become one of the dominant requirements for the semiconductor designs in the past decade. From commercial design-for-test (DFT) tools' point of view, this paper describes how DFT tools can help to achieve comprehensive testing of low power designs and reduce test power consumption during test application.

B. Low-Power Testing Techniques for Internal Testing

Various authors reported on techniques to cope with power problems during BIST. Several techniques have been reported to address the low power BIST. The technique proposed in consists of a distributed BIST control scheme that simplifies BIST architecture for complex ICs, especially during higher levels of test activity. The approach can schedule the execution of every BIST element to keep the power dissipation under specified limits. The technique reduces average power and avoids temperature-related problems but increase in test time. A BIST strategy called dual-speed LFSR is proposed in [7] to reduce the circuit's overall switching activities. The technique uses two different speed LFSRs to control those inputs that have elevated transition densities. The low power test pattern generator presented in is based on cellular automata, reduces the test power in combinational circuits while attaining high fault coverage. Test time and area overhead remain unaffected.

Another low-power test pattern generator based on a modified LFSR is proposed in [8]. The scheme reduces the power in CUT in general and clock tree in particular. Gizopoulos et al. consider the problem of low-power BIST for data path architecture built around multiplier-accumulator pairs. The method proposes two alternative architectures depend on low energy or low power dissipation. The authors based on both modified binary counters, operating as Gray counters, generate only one transition at a time. A low-power random pattern generation technique to reduce signal activities in the scan chain. In this technique, an LFSR generates equally probable random patterns. The technique generates random but highly correlated neighboring bits in the scan chain, reducing the number of transitions and, thus, the average power. Girard et al. address the problem of energy minimization during test application for BIST enabled circuits. Test vector inhibiting techniques to filter out some non-detecting subsequences of a pseudorandom test set generated by an LFSR. The architectures apply the minimum number of test vectors required to attain the desired fault coverage and therefore reduce power. A test pattern generator for scan-based BIST was proposed, that reduce the number of transitions that occur at scan inputs during scan shift operation. A pseudorandom BIST scheme to reduce the switching activity in the scan chains. The activity and correlation in CUT is controlled by limiting the scan shifts to a portion of the scan chain structure using scan chain disable control.

III. PATTERN GENERATOR:

The BIST contains two major components: test pattern generator and response checker. Both of these components use Linear Feedback Shift Register (LFSR). The paper described the three different pattern generation techniques by using LFSR can be designed to reduce the power consumption during test in the following ways. A digital pattern generator is a piece of electronic test equipment or software used to generate digital electronics stimuli. Digital electronics stimuli are a specific kind of electrical waveform

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varying between two conventional voltages that correspond to two logic states ('low state' and 'high state', '0' and '1'). The main purpose of a digital pattern generator is to stimulate the inputs of a digital electronic device. For that reason, the voltage levels generated by a digital pattern generator are often compatible with digital electronics I/O standards – TTL, LVTTL, LVCMOS and LVDS, for instance. A digital pattern generator is a source of synchronous digital stimulus; the generated signal is interesting for testing digital electronics at logic level - this is why they are also called 'logic source'. A pulse generator is of purpose to generate electrical pulse of different shapes; they are mostly used for tests at an electrical or analog level. Another common name for such equipment is 'digital logic source' or 'logic source'. Stand-alone units are self-contained devices that include everything from the user interface to define the patterns that should be generated to the electronic that actually generates the output signal.

Some test equipment manufacturers propose pattern generators as add-on modules for logic analyzers (see for example the PG3A module for Tektronix' TLA7000 series of logic analyzers). In this case, the pattern generator is the 'generation counterpart' to the analysis functionality offered by logic analyzers. As integrated circuit feature size continues to shrink and wireless and portable devices grow, power consumption not only becomes one of the key issues to be considered during functional operation, but also has to be addressed during manufacturing tests. High power consumption during the functional operation implies
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- Higher design and manufacturing costs due to the extra effort to calibrate power grids in order to meet the power supply requirement.
- Higher system costs due to packaging and cooling requirements.
- Shorter device life cycle and lower device reliability.
- Shorter battery life for portable devices.

A. Generating Test Vectors by using Modified Clock Scheme

A new low power BIST test pattern generator that provides test vectors which can reduce the switching activity during test operation. The proposed low power/energy BIST technique is based on a modified clock scheme for the TPG and the clock tree feeding the TPG. Numerous advantages can be found in applying such a technique. The fault coverage and the test time are roughly the same as those achieved using a standard BIST scheme. The area overhead is nearly negligible and there is no penalty on the circuit delay. The proposed BIST scheme does not require any circuit design modification beyond the parallel BIST technique is easily implemented and has low impact on the design time. It has been implemented based on an LFSR-based TPG, but can also be designed using a cellular automata. Reductions of the energy, average power and peak power consumption during test operation are up to 94%, 55% and 48% respectively for ISCAS and MCNC benchmark circuits. Girard et al.

proposed the low-power test pattern generator (TPG) based on modified clock scheme. The low-power BIST technique relies on a gated clock scheme for the pseudorandom test pattern generator and the clock tree feeding the TPG. The two clocks are synchronous with a master clock CLK and have the same but shifted in time period. The clock CLK is the clock of the circuit in the normal mode and has a period equal to T. As one can observe, a test vector is applied to the CUT at each clock cycle of the test session, only one half of the circuit inputs can be activated during the time. Consequently, the average powers as well as the peak power consumed in the CUT are minimized. The drawback of the technique is to reduce the randomness property of the LFSR also requires two non-overlapping clocks with half frequency and increases the area overhead. Digital pattern generators are primarily characterized by a number of digital channels, a maximum rate and the supported voltage standards.

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- The number of digital channels defines the maximum width of any pattern generated - typically, 8-bits, 16-bits, 32 bits pattern generator. A 16-bits pattern generator is able to generate arbitrary digital samples on from 1 to 16 bits.
- The maximum rate defines the minimum time interval between 2 successive patterns. For instance, a 50 MHz (50 MSample/s) digital pattern generator is able to output a new pattern every 20 nanoseconds.
- The supported voltage standards ultimately define the set of electronic devices a digital pattern generator can be used with. Concretely, the voltages and the transition characteristics of the signal at the output of the digital pattern generator will be compliant to these voltage standards. Examples of supported voltage standards: TTL, LVTTL, LVCMOS, LVDS.

Most digital pattern generator add features such as the ability to generate a repetitive sequence or a digital clock signal at a specified frequency, the ability to use an external clock input and triggering options, to start pattern generation upon the reception of an event from an external input.

B. Generating Test Vectors by using LPATPG:

Low Power consumption has become increasingly important in hand-held communication systems and battery operated equipment, such as laptop computers, audio and video-based multimedia products, and cellular phones. For this new class of battery-powered devices, the energy consumption is a critical design concern since it determines the lifetime of the batteries. In addition, the capabilities presented by advanced submicron CMOS technology allowing to put millions on transistors on chip and clocking at hundreds of MHz have Compounded the problem of power/energy consumption. A strong push towards reducing power consumption is also coming from producers of high-end systems. The cost associated with packaging and cooling of such devices is huge and technological constraints are severe: The random nature of the test patterns is kept intact. The area overhead of the additional components to the LFSR is negligible compared to the large circuit sizes. The experimental results for ISCAS"85 and "89 benchmarks, confirm up to 77% and 49% reduction in average and peak power, respectively.

C. Generating Test Vectors by using LT-LFSR:

Mohammad Tehranipoor proposed a low-transition LFSR by combining techniques of random pattern generation called R-Injection (RI) and Bipartite LFSR for low-power BIST. The new LT-LFSR generates three intermediate patterns. The RI method inserts a new intermediate pattern between two consecutive test patterns by positioning a random-bit (R) in the corresponding bit of the intermediate pattern when there is a transition between corresponding bits of pattern pairs. The bipartite LFSR generates an intermediate pattern using one half of each of the two consecutive random patterns.

The goal is to design a new random pattern generator reduces the total number of transitions among the adjacent bits in each random pattern (horizontal dimension) and transitions between two consecutive random patterns (vertical dimension) as well. In other words, the new low transition random pattern generator increases the correlation between and within patterns. The main advantage of the technique can be used for both combinational and sequential circuits and the randomness quality of patterns does not deteriorate. The authors also use a k-input AND gate and T-latch to generate a high correlation between neighboring bits in the scan chain, reducing the number of transitions and the average power.

IV. BIST ARCHITECTURE:

BIST, is the technique of designing additional hardware and software features into integrated circuits to allow them to perform self-testing, i.e., testing of their own operation (functionally, parametrically, or both) using their own circuits, thereby reducing dependence on an external ATE.

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Recently, techniques to cope with the power and energy problems during BIST have appeared. A brief overview of these techniques is given in Section 2. In this paper, we address the low power testing problem in BIST. BIST is well known for its numerous advantages such as improved testability, at-clock-speed test of modules, reduced need for automatic test equipment, and support during system maintenance. Moreover, with the emergence of core-based SOC designs, BIST represents one of the most favorable testing method since it allows to preserve the intellectual property of the design. In most complex SOC designs characterized by very poor controllability and observability, BIST is even probably the only practical solution for efficient testing. The industrial needs initiated academic research. Hence, techniques to cope with the power and energy problems during BIST have appeared recently. These approaches targeting combinational circuits can be classified as follows:

1) Distributed BIST Control Schemes. The goal in these approaches is to determine the BIST blocks of a complex design to be activated in parallel at each stage of the test session in order to reduce the number of concurrently tested modules. The average power is reduced and consequently, the temperature related problems avoided by the increase of the test time duration. On the other hand, the total energy remains constant and the autonomy of the system is not increased.

2) Vector Filtering Architectures as each vector applied to the CUT consumes power but not every vector generated by the pseudo-random TPG contributes to the final fault coverage, the vector filtering architectures consist in preventing application of non-detecting vectors to the CUT. This approach is very effective in reducing power without reducing fault coverage, but does not preserve the CUT from excessive peak power consumption and can lead to high area overhead.

3) Low Power Test Pattern Generators. TPGs based either on LFSRs or Cellular Automata (CA) are carefully designed to reduce the activity at circuit inputs, thus reducing power consumption. These approaches effectively reduce power during test but sometimes at a cost of sub-optimal fault coverage and with no reduction of the peak power consumption.

4) Circuit Partitioning for Low Power BIST [22]. This approach consists in partitioning the original circuit into structural sub-circuits so that each sub-circuit can be successively tested through different BIST sessions. In partitioning the circuit and planning the test session, the average power, the peak power and the energy consumption during BIST are minimized at a low expense in terms of area overhead and with no loss of fault coverage. The only drawback of this approach is that it requires circuit design modification. The above mentioned approaches can be easily adapted for testing sequential circuits though customized full-scan architectures.

A. Implementation of BIST:

The reduction of the power consumption in a test-per-clock BIST environment is commonly achieved by reducing the switching activity in the CUT. Furthermore, it has been demonstrated in [5] that the switching activity in a time interval (i.e. The average power) dissipated in a CUT during BIST is proportional to the transition density at the circuit inputs. Thereby, several low power test pattern generators have been proposed to reduce the activity at circuit inputs (see above description in part 2.2). Among these techniques, the DS-LFSR proposed in [5] consists in using two LFSRs, a slow LFSR and a normal speed LFSR, as TPG. A typical BIST architecture consists of Test Pattern Generator (TPG) usually implemented as a LFSR, Test Response Analyzer (TRA), Multiple Input Signature Register (MISR), CUT and BIST control unit as shown in figure 1.

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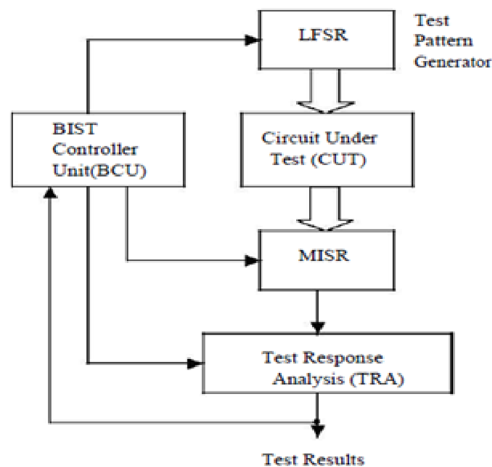

Figure 1: BIST Architecture

CUT: It is the portion of the circuit tested in BIST mode. It can be sequential, combinational or a memory. Their Primary Input (PI) and Primary output (P0) delimit it.

TPG: It generates the test patterns for the CUT. It is dedicated circuit or a microprocessor. The patterns may be generated in pseudorandom or deterministically.

MISR: It is designed for signature analysis, which is a technique for data compression. MISR efficiently map different input streams to different signatures with every small probability of alias.

TRA: It will check the output of MISR & verify with the input of LFSR & give the result as error or not.

BIST Control Unit: Control unit is used to control all the operations. Mainly control unit will do configuration of CUT in test mode/Normal mode, feed seed value to LFSR, Control MISR & TRA. It will generate interrupt if an error occurs. In BIST, LFSR generates pseudorandom test patterns for primary inputs (PIs) or scan chains input. MISR compacts test responses received from primary output or scan chains output.

Test vectors applied to a CUT at nominal operating frequency, often cause more average and/or peak power dissipation than in normal mode. The result in more switching's and power dissipation in test mode. As in [5], the low power/energy BIST technique proposed in this paper is based on a modified clock scheme for the pseudo-random TPG. Basically, a clock whose speed is half of the normal speed is used to activate one half of the D flip-flops in the TPG (i.e. a modified LFSR) during one clock cycle.

During the next clock cycle, the second half of the D flip-flops is activated by another clock whose speed is also half of the normal speed. The two clocks are synchronous with a master clock CLK and have the same but shifted in time period. The clock CLK is the clock of the circuit in the normal mode and has a period equal to T. The basic scheme of the proposed low power test pattern generator with the corresponding clock waveforms are depicted in Figure 1. As one can observe, a test vector is applied to the CUT at each clock cycle of the test session.

However, only one half of the circuit inputs can be activated during this time. Consequently, the switching activity in a time interval (i.e. the average power) as well as the peak power consumed in the CUT are minimized. Moreover, the power consumed in the TPG is also minimized since only one half of the D flip-flops in the TPG can be activated in a given time interval.

Another important feature of the proposed solution is that the total energy consumption during BIST is reduced since the test length produced by the modified LFSR is roughly the same than the test length produced by a conventional LFSR-based TPG to reach the same or sometimes a better fault coverage.

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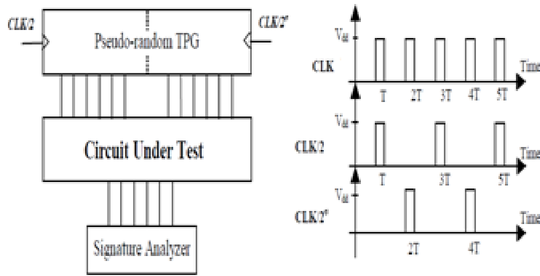

Figure 2: Basic scheme of the low power test pattern generator

The low power TPG:

The idea behind the use of such a low power TPG is to reduce the number of transitions on primary inputs at each clock cycle of the test session, hence reducing the overall switching activity generated in the CUT. Let us consider a CUT with n primary inputs. A n-stage primitive polynomial LFSR with a clock CLK would be used in a conventional pseudorandom BIST scheme. Here, we use a modified LFSR composed of n D-type flip-flops and two clocks CLK/2 and CLK/2_ , and constructed as depicted in Figure 2 (n=6 in the example of Figure 2). As one can observe, this modified LFSR is actually a combination of two n/2-stage primitive polynomial LFSRs, each of them being driven by a single clock CLK/2 or CLK/2_ . The D cells belonging to the first LFSR (referred to as LFSR-1 in the sequel) are interleaved with the cells of the second LFSR (referred to as LFSR-2 in the sequel), thus allowing to better distribute the signal activity at the inputs of the CUT.

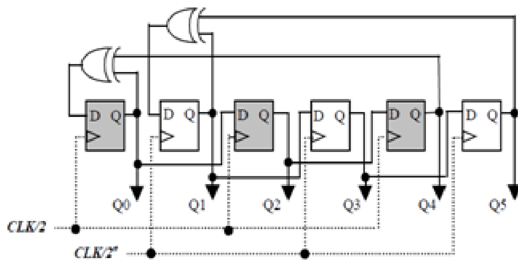

Figure 3: An example of the modified LFSR TPG

In order to better describe the functioning of the low power TPG, the timing diagram of the test sequence generated by the example TPG shown in Figure 2 is reported in Table 1. Assume that the seed <001> has been chosen for both LFSRs, such that the first vector applied to the CUT at time T is <100001>. Only LFSR-1 is active during the first clock cycle (LFSR-2 is in stand-by mode). This is illustrated in the two last columns of Table 1 in which a 8 grey cell represents the active LFSR in the corresponding clock cycle. During the next clock cycle, LFSR-2 is active (LFSR-1 is in stand-by mode) and vector <110000> is applied to the CUT. The advantage of the modified LFSR composed of two interleaved *n/2*-stage LFSRs (over a simpler structure composed of two separated *n/2*-stage LFSRs) is that it allows to better distribute the signal activity at the circuit inputs during the BIST session. This is particularly important for circuits in which the input cones of the primary outputs are highly non-overlapping.

A. Implementation of low transition test pattern:

The basic idea behind low power BIST is to reduce the PI activities. The paper proposes a new transition test pattern generation technique which generates three intermediate test patterns between each two consecutive random patterns generated by a conventional LFSR. The proposed test pattern generation method does not decrease the random nature of the test patterns. The technique reduces the PI‟s activities and eventually switching activities in the circuit under test. Let us assume that Ti and Ti+1 are two consecutive test patterns generated by a pseudorandom pattern generator (e.g. a conventional LFSR). The new low transition LFSR (LTLFSR) generates three intermediate patterns (Ti1, Ti2 and Ti3) between Ti and Ti+1. The total number of signal transition occurs between these five vectors are equivalent to the number of transition occurs between the two vectors. Hence the power consumption is reduced. Additional circuit is used for few logic gates in order to generate three intermediate vectors. The area overhead of the additional components to the LFSR is negligible compared to the large circuit sizes.

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The three intermediate vectors (Ti1, Ti2 and Ti3) are achieved by modifying conventional flip-flops outputs and low power outputs.

B. Implementing algorithm for LT-LFSR:

The proposed approach consists of two half circuits. The algorithm steps says the functions of both half circuits is Step1: First half is active and second half is idle and gives out is previous, the generating test vector is Ti.

Step2: Both halves are idle First half sent to the output and second half‟s output is sent by the injection circuit, the generating test vector is Ti1.

Step3: Second half is active First half is in idle mode and gives out as previous, the generating test vector is Ti2.

Step4:Both halves are in idle mode, First half is given by injection circuit and Second half is same as previous, the generating test vector is Ti3.

After completing step 4 again goes to step1 for generating test vector Ti+1. The first level of hierarchy from top to down includes logic circuit design for propagation either the present or next state of flip- flop to second level of hierarchy. Second level of hierarchy is implementing Multiplexed (MUX) function i.e. selecting two states to propagate to output which provides more power reduction compared to having only one of the R Injection and Bipartite LFSR techniques in a LFSR due to high randomness of the inserted patterns.

V. RESULTS

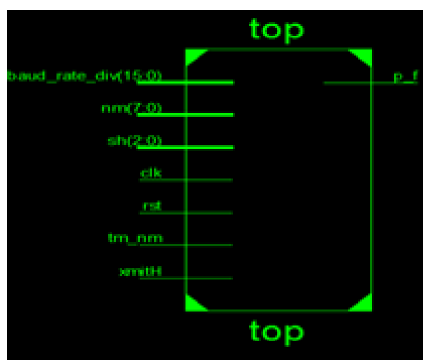

Figure 4: RTL Schematic for top module

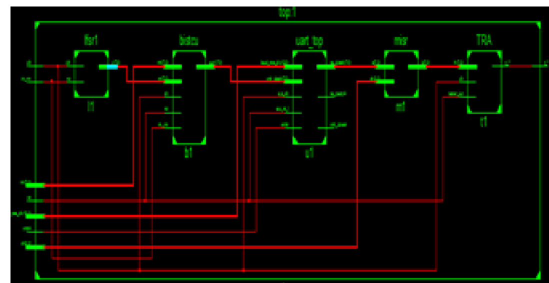

Figure 5: RTL Schematic for detailed architecture

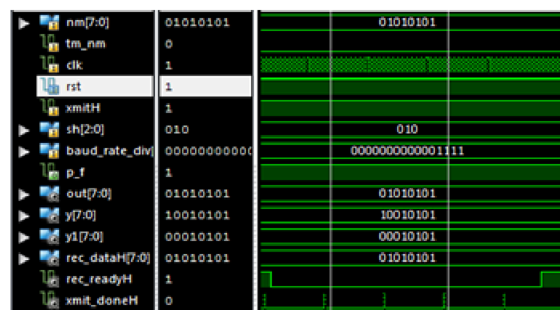

Figure 6: Simulation results for proposed system (normal mode)

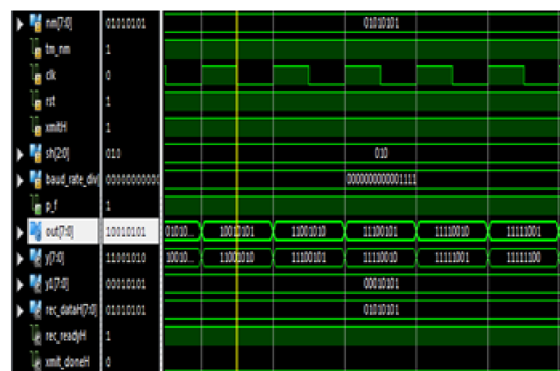

Figure 7: Simulation results for proposed system (test mode)

VI. CONCLUSION:

The proposed approach is a new low power pattern generation technique is implemented using a modified conventional LFSR. Comparisons of the number of test patterns (NP) required to hit target fault coverage (FC), the average and peak power of LT-LFSR, LPATPG and modified clock scheme. The used 50 different seeds for 10 different polynomials in the experiment. The performance of LT-LFSR is seed and polynomial-independent.

The required number of patterns provides target FC does not quadruples, and preserving randomness. By using this low transition test pattern generator using LFSR for Test Pattern Generation (TPG) technique we conclude that power dissipation is reduced during testing. The transition is reduced by increasing the correlation between the successive bits, reduces the average and peak power of a circuit during the test mode. By increasing the correlation between the test patterns in the CUT and eventually the power consumption is reduced. Additional intermediate test patterns inserted between the original random patterns reduces the PI activities, average and peak power of combinational and sequential circuits during the test mode with do not effect on FC.

REFERENCES:

[1] S. Sde-Paz and E. Salomon, “Frequency and power correlation between at-speed scan and functional tests,” inProc. Int. Test Conf., 2008, pp. 1–9, Paper 13.3.

[2] I. Pomeranz and S. M. Reddy, “Generation of functional broadside tests for transition faults,”IEEE Trans. Comput.-Aided Design Integr. Circuits Syst., vol. 25, no. 10, pp. 2207–2218, Oct. 2006.

[3] J. Savir and S. Patil, “Broad-side delay test,”IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.,vol. 13, no. 8, pp. 1057–1064, Aug. 1994. Pomeranz, “On the generation of scan-based test sets with reachable states for testing under functional operation conditions,” inProc. Design Autom. Conf., 2004, pp. 928–933.

[4] Y.-C. Lin, F. Lu, K. Yang, and K.-T. Cheng, “Constraint extraction for pseudo-functional scan based delay testing,” in Proc. Asia South Pacific Design Autom. Conf., 2005, pp. 166–171.

[5] Z.Zhang, S.M.Reddy, and I.Pomeranz, “On generating pseudo-functional delay fault tests for scan designs,” in Proc. Int. Symp. Defect Fault Toler. VLSI Syst., 2005, pp. 398–405. Polian and F. Fujiwara, “Functional constraints vs. test compression in scan-based delay testing,” inProc. Design, Autom. Test Euro. Conf., 2006, pp. 1–6.

[6] M. Syalet al., “A study of implication based pseudo functional testing,” inProc. Int. Test Conf., 2006, pp. 1–10.

[7] F. Corno, P. Prinetto, M. Rebaudengo, M. Sonza Reorda," A Test Pattern Generation methodology for low power onsumption," pp.1-5, 2008.

[8] P.Glard et al "Survey 0 F Low-Power Testing Of Vlsi Circuits"IEEE Design & Test Of Computers, vol. 19, no. 3. (2002), pp. 80-90.