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Design of 3- Φ Current-Fed Unfolded Inverter

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Abstract:

Current fed converters are used for PV, fuel cell and battery applications. Fuel cells deliver electrical energy as long as fuel supply is maintained. In this project a current fed phase modulated interleaved unfolded inverter is existing to obtain a single phase voltage by simply unfolded the rectified sine wave using H-bridge inverter. Proposed system will achieve a three phase AC power through a Two active-clamped Zero Voltage Switching (ZVS) half-bridge isolated converters interleaved in parallel input and series output configuration. The power converter is simulated with MATLAB/SIMULINK.

Index Terms: Current-fed dc/dc converter, fuel cells, Zero Voltage Switching (ZVS), high-frequency (HF), inverter, photovoltaic (PV).

I. INTRODUCTION:

CURRENT-SOURCE INVERTER (CSI) is mostly adopted for high power applications why because, it supplies a constant input DC current[1], CSI will also performs bidirectional operation[2], shoot through protection and sinusoidal output voltage necessary to run a AC motor without stress and losses[3]. CSI also have some disadvantages, i.e., poor torque dynamic response and bulky in size. CSI is reliable for high power usages even though it has some disadvantages, it is preferred. The usage of CSI has gradually growing day-by-day[4]-[5], and preferred for both low and high power applications. Studies clearly says that CSI is also used for low power range applications[5], CSI become more convenient after adding the reverse blocking switches in its construction.With these researchers are researching to form a hybrid topology by combining merits of VSI & CSI to obtain better output waveform when only single CSI or VSI is used[6]. Researchers are also going on to develop multilevel CSI and to bring the advantages equal to VSI [7].

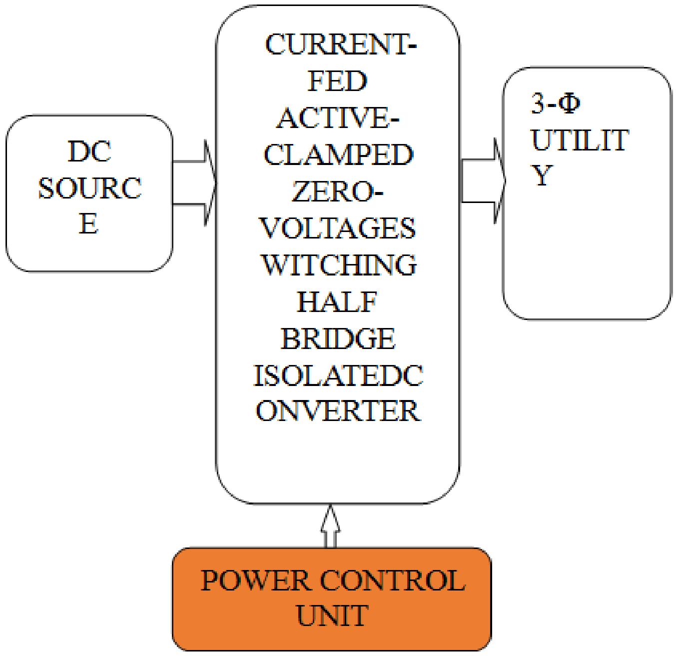

Fig.1. System Block Diagram

Actually multilevel CSI's uses a five-level topology shown in fig.(2). Fig.2 (a) has two CSI bridges connected by two inductors L_1&L_2, and supply is given by a current source [8]. Here inductors L_1&L_2 are used to maintain constant current. The cost of these mechanisms is low because only a single input source is used. To maintain the current ratio between the two bridges is necessary, for these some mechanisms are used and this makes the system complex.

In order to overcome this, two CSI bridges are connected parallel as shown in Fig. 2(b), is straightforward [9], but it is more costly compared with the above one, as it is using two independent current sources. The usage of these two topologies will produce five-level AC current switching but the cost is high and the system is also complicated. The usage of DC inductors in series with the voltage sources makes the system size larger and current rating is also high.

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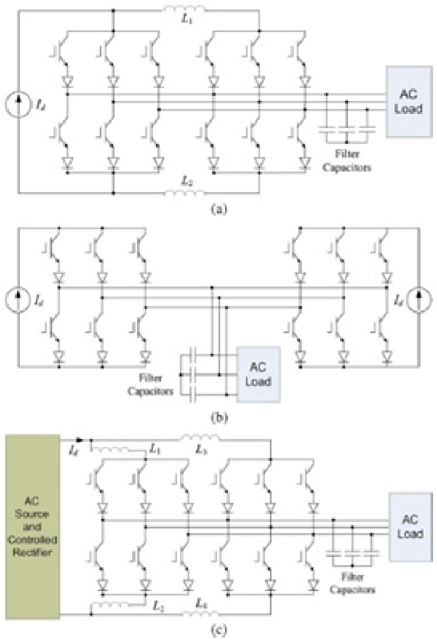

Fig.2 3-Φfive-level CSI's reported in (a) [10], [11], (b) [12], [13], & (c) [14].

To overcome these problems Fig. 2(c). is not using a common DC source inductor[10], by using smaller inductor pairs the current is smoothed and becomes a cost-saving option for filtering. The obtained input source will rectify the AC mains easily, but to balance DC inductive current between two bridges is a major problem [11] and necessary control modifications is required.

II. Steady State Analysis:

The Two active-clamped Zero Voltage Switching (ZVS) unfolded inverter is a proposed current fed and phase modulated one. In this two identical active clamped current fed DC/DC converter cells are connected parallel to the input DC source. The two inverters are modulated with a phase shift as the phase difference between them is sine function at line frequency. In this secondaries of the HF transformer are in series, they are followed by a diode bridge rectifier.A low pass filter filters HF components of voltage so as to achieve rectified sinusoidal voltage across filter capacitor C_0 at twice the line frequency. The rectified sine wave is unfolded to obtain 3 Φ AC voltages by using the H-bridge inverter switching at line frequency i.e.., unfolded. MPPT can be performed by the front end DC/DC converter in two ways.

1.Varying the duty ratio.

2.Phase difference between the gate signals of two cells.

The current injected in to the grid is proportional to power available from the PV array. The injected current at MPP can be optimized by front end control. Similarly any traditional technique may be adopted.

Assumptions to understand the steady state operation of the converter:

1.All devices and components are ideal.

2.Both converter cell components are identical.

3.Constant current over a HF switching cycle can be maintained by L_1-L_4 inductors.

4.Constant voltage over a HF switching cycle can be maintained byC_CL_1 andC_CL_2clamp capacitors.

5.Leakage inductance of the particular transformers can be denoted withL_S_1 andL_S_2 series inductors.

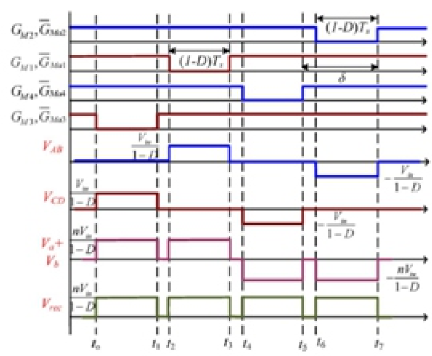

Fig.3. Waveforms for main switchesM_1–M_4 and voltagesV_AB, V_CD, V_a+V_b, and V_REC.

Gating signals operate the main switches M_1&M_2 so as the phase is shifted by 180 with an overlap which varies duty ratio D. Increased circulating current through the devices at low duty cycle values always keep the duty cycle of the main switch is greater than 50%. Gating signals control the auxiliary switches complementary to the appropriate gating signals of the main switch. Here the duty cycle ratio of the auxiliary switches is (1-D) and less than 50%. Controlling is done through the fixed frequency duty cycle modulation.

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Transformer primary and secondary voltages i.e.., V_AB,V_CD, andV_a+V_bis shown in the above Fig.3.Another similar converter is connected except the phase shift between the two converter cells.Gate signals between switches M_1&M_3 are phase shifted by time,

$$\delta=\frac{T_s}{2} + \alpha \sin(\omega t) \quad [1]$$

where,
T_s is the time period,
ω is the frequency,
α is the Magnitude of the output voltage.

In the same way switch pairs M_2&M_4, $M_{a_1}-M_{a_3}$ and $M_{a_2}-M_{a_4}$ have the same duty ratio and phase shifted by time δ. If the main switch is turned off, a corresponding auxiliary switch is turned on. This leads to clamping capacitor voltage across the transformer primary terminals i.e..,

$$V_{C_{cl_1}} = V_{C_{cl_2}} = \frac{D}{1-D} V_{in} \quad [2]$$

When switch M_1 is turned off as in Fig.3.$t_2 < t < t_3$, transformer primary voltage (V_{AB}) is

$$V_{AB} = V_{in} + V_{C_{cl_1}} = \frac{1}{1-D} V_{in}$$

When switch M_2 is turned off as in Fig.3.$t_6 < t < t_7$, transformer primary voltage (V_{AB}) is

$$V_{AB} = -V_{in} - V_{C_{cl_1}} = -\frac{1}{1-D} V_{in} \quad [3]$$

Second converter transformer primary voltage (V_CD) is also derived in the same way. Both converter cells transformer secondary voltage can be calculated as multiple of turn ratio n. A full bridge diode rectifier is used to rectify secondary transformer.

Rectifier output voltage (V_REC)is followed by a low pass filter, which is used to absorb HF switching components results in average voltage (V_Co) across capacitor(C_o).

III. DESIGN PROCEDURE:

Converter Specifications:
Input voltage(V_{in}) = 40 V,
Output RMS voltage(V_0) = 440 V,
Output frequency (f_0)= 50 Hz,
Output power(P_0)= 200 W,
Switching frequency (f_s)= 100 kHz
Dutyratio (D)= 0.8.

(1) Average input current:
$I_{in} = P_0/(\eta V_{in})$ [4]
Assumed ideal η of 100%, I_{in} =9.09 A. As they are sharing equal current, Input current in each converter will be half.

(2) Values of boost inductors:

$$L_1=L_2=L_3=L_4= (V_{in})(D)/[(\Delta I_{in})(f_s)] \quad [5]$$

Where,
ΔI_{in} = boost inductor ripple current.
For ΔI_{in}=1A, L_1=L_2=176µh. Maximum voltage across the inductors=V_{Ca_1}=V_{Ca_2}=88V, Average current through the inductors=$I_{in}/4$ = 2.3 A.

(3) Transformer turns ratio: Modulation index is considered as 0.75 for maximum desired output voltage then

$$n == \frac{V_{0,peak}.\sqrt{2}}{4\, V_{in,min}.m_a} = \frac{110\sqrt{2}}{39} \quad [6]$$

Here, turns ratio is 4 when assumed minimum input voltage is 13V.

(4) Filter Design: By assuming voltage drop is less than 2% of the nominal voltage, filter inductor is

$$L_0 = \frac{V_0.0.02}{2\pi.f_0.I_0} \quad [7]$$

Where,
f_(o)= output frequency,
I_o= output current.

As specifications $L_0$is obtained as 3.85mh. According to the cut off frequency of the low pass filter, filter capacity is decided. Here one-tenth of converter switching Frequency (f_s) is selected as the cutoff frequency. Therefore calculated capacitor,

$$C_0 = \frac{1}{4\pi^2.f_C^2.L_0} \quad [8]$$

Where, f_c=cut off frequency=10khz, capacitor $C_0$is obtained as 0.63µf.

(5) Unfolded Circuit: Based on the maximum voltage acrossC_0, Switches voltage rating is selected. This is equal to peak value of maximum output voltage. RMS switch current rating,

$$I_{S1,RMS} = \frac{I_0}{\sqrt{2}} \qquad [9]$$

As specificated, voltage=200V, and current=2.57 A.

IV. SIMULATION RESULTS:

For an input voltage of 40 V, an output voltage of 440 V is obtained by switching the current-fed converter at 100 kHz with a fixed duty ratio of 0.8. The components' values obtained in Section III are used as parameters for simulation.

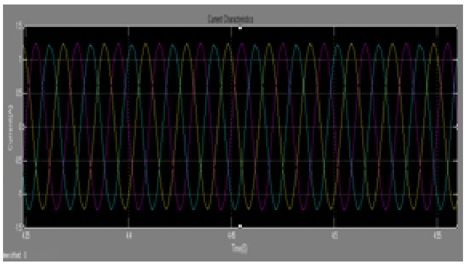

Fig.4. Simulation results of output current I_o.

Frequency of the delay function is selected as 50 Hz. Rectified sinusoidal voltage is obtained across capacitor (C_(0)). A filter Cut off frequency of 10 kHz is selected, which eliminates the 100Hz components from the voltage. Unfolded inverter switches are used for controlling the Square wave line frequency. By switching devices at a very low frequency of 50 Hz, output sine wave is obtained.

The current sharing between the two cells is not uniform over a half line frequency cycle due to the leakage inductance of the HF transformer, but have identical wave shape over one line cycle. However, the input current drawn from the source is of a 100Hz frequency with HF components riding over it. The low-frequency pulsation is absorbed by ultra-capacitor or low-voltage electrolytic capacitor placed at the input and blocks to appear across the source.

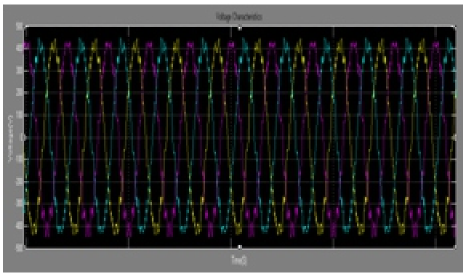

Fig.5. Simulation results of output voltage V_o

V. Advantages & Disadvantages :

(a)VSI Advantages:

1.Best and efficient results are obtained for low power applications.

2.Voltage stress can be reduced by using multilevel VSI's in the medium voltage applications.

(b) VSI Disadvantages:

1.It can't be applied/used for high power applications because losses in the switching are high.

2.It can't be applied/used for medium power applications because necessary voltage equipment ratings are not available.

3.There is no impedance path.

4.Due to shoot through there are chance to burn or collapse.

5.Emission of electro-magnet.

6.Flow of current in the bearing.

(c) CSI Advantages:

(1)Best and efficient results are obtained for low power applications.

(2)Protection of shoot through.

(3)Capable for regenerating.

(4)Fixed frequency is maintained.

(d) CSI Disadvantages:

(1)Poor torque dynamic response.

(2)Used only when the torque dynamic response is neglected.

VI. CONCLUSION:

For low-voltage, high-current applications,current fed converters are best suited. Unfolded type HF multilevel concept is not implemented in 3-Φ inverters so far. This is the first paper based on this concept for current fed topologies. Transformers of higher turns ratio is needed for voltage-fed converters to achieve high voltage. Another disadvantage of voltage-fed converters is ringing across secondary side diodes and duty cycle loss. This paper presents a current-fed unfolded inverter toproduce3-Φ voltage.By phase modulation, DC/AC inversion is easy and results in reducing the switching losses.

The following are the additional advantages:

(1)Voltage Distortion is decreased.

(2)Switching losses are reduced.

(3)Circuit resonances are minimized.
In future, input capacitor size can be totally minimized.

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