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An Efficient Implementation of VEDIC Multipliers Using Reversible Gates

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Abstract:

Multipliers are vital components of any processor or computing machine. More often than not, performance of microcontrollers and Digital signal processors are evaluated on the basis of number of multiplications performed in unit time. Hence better multiplier architectures are bound to increase the efficiency of the system. Vedic multiplier is one such promising solution. Its simple architecture coupled with increased speed forms an unparalleled combination for serving any complex multiplication computations. Tagged with these highlights, implementing this with reversible logic further reduces power dissipation.

In this paper we bring out a Vedic multiplier known as " Urdhva Tiryakbhayam multiplier". The Urdhva Tiryakbhayam literally means : crosswise and vertical"—.Thisis implemented using reversible logic. This multiplier may find applications in Fast Fourier Transforms (FFTs), and other applications of DSP like imaging, software defined radios, wireless communications. The purpose of this project is to implement a 8x8 vedic multiplier using reversible gates which are operated at very high speed. The functionality of RT is verified by using Mentor Graphics Tools and implemented on Spartan-3E FPGA kit.

Keywords-:
Multiplier, Vedic multiplier, Reversible logic,Urdhava Triyagbhyam,.

I. INTRODUCTION:

Vedic mathematics is an ancient Indian mathematical technique based on 16 sutras. The sutras of Vedic Mathematics are the software for the cosmic computer that runs this universe.

Vedic Mathematics introduces the wonderful applications to Arithmetical computations, theory of numbers, compound multiplications, algebraic operations, factorizations, simple quadratic and higher order equations, simultaneous quadratic equations, partial fractions, calculus, squaring, cubing, square root, cube root, coordinate geometry and wonderful Vedic Numerical code.

The multipliers are the most important part of all digital signal processors; they are very important in realizing many important functions such as fast Fourier transforms and convolutions. Since a processor spends considerable amount of time in performing multiplication, an improvement in multiplication speed can greatly improve system performance. Multiplication can be implemented using many algorithms such as array, booth, carry save, and Wallace tree algorithms.

Reversible logic is a promising area of study with regard to the future low power technology. It has applications in various research areas such as optical computing, low power CMOS design, DNA computing, Quantum computing, thermodynamic technology, bioinformatics and nanotechnology.
This paper proposes the implementation of reversible logic UT multiplier which has two main features. One is implementing the multiplier using vedic sutra increases the speed of the multiplication. Second is the use of reversible logic reduces the area and the hence the power dissipation.

The paper is partitioned into six sections. Section II gives literature survey, Section III explains reversible logic.Section IV explains Vedic multiplier algotithm Section V elaborates on the design aspects of Reversible Urdhva Tiryakbhayam Multipliers. Section VI results of our design with the literature. Section VII Conc1usions. Section VIII Acknowledgement and references follows

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II. LITERATURE REVIEW:

Energy dissipates whenever switching activity occurs in the CMOS circuits..Landauer's Principle [3] states that logical computations that are not reversible necessarily generate k*T*ln(2) joules of heat energy, where k is the Boltzmann's Constant k=1.38xlo-23 J/K, T is the absolute temperature at which the computation is performed. Although this amount of heat appears to be small, Moore's Law predicts exponential growth of heat generated due to information lost, which will be a noticeable amount of heat loss in next decade.

Bennett showed that zero energy dissipation would be possible only if the network consists of reversible logic gates, Thus reversibility will become an essential property in future circuit design technologies.Reversible circuits are those circuits that do not loose information. Reversible computation in a system can be performed only when the system comprises of reversible gates.

In paper [6] H. Thapliyal and M.B. Srinivas designed the multiplier using two units; one is the partial product generation unit constructed using Fredkin gates and other the summing unit constructed using 4x4 TSG gates. [7] has proposed a design of reversible multiplier which makes use of Peres gate for generation of partial products as compared to [10], which uses Fredkin gates. For the construction of adders the HNG gate was devised.[15] Proposes low quantum cost realization of reversible multipliers which mainly uses Peres full adder gate (PFAG) for its design. It also uses Peres gates for the generation of partial products.

III. REVERSIBLE LOGIC GATE:

Reversible circuits are those circuits that do not loose information. Reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector, and vice versa, that is, there is a one-to-one mapping between input and output vectors. Thus, an NXN reversible gate can be represented as

Iv = (I1,I2,I3,I4,……IN)

Ov = (O1,O2,O3,……ON).

Where Iv and Ov represent the input and output vectors respectively.

The reversible circuit/gate has the following characteristics [2]:

1.It has equal number of inputs and outputs .

2.The gate output, which is not used as primary output in the circuit, is called garbage output.

3.The input which is used as control input to the gates is called constant/garbage input .

4.The fan-out of each gate is equal to one. A copying circuit is used if two copies of a signal are required .

5.The resulting circuit is acyclic .

An efficient design in reversible logic should have the following features: (a) use minimum number of reversible logic gates, (b) should have less number of garbage outputs

(c) less number of constant inputs and (d) minimization of quantum cost.

The basic reversible logic gates that are used in this design are shown below.

Feynman gate:

Fig 1 shows a 2*2 Feynman gate. The input vector is I (A, B) and the output vector is O (P, Q). The outputs are defined by P=A, Q=AB. Quantum cost of a Feynman gate is 1.

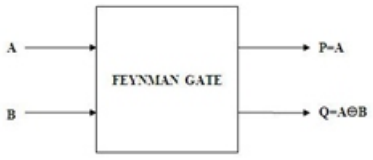

Fig 1 FEYNMAN gate

Peres gate:

Fig 2 shows a 3*3 Peres gate [4]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = AB and R=ABC. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost.

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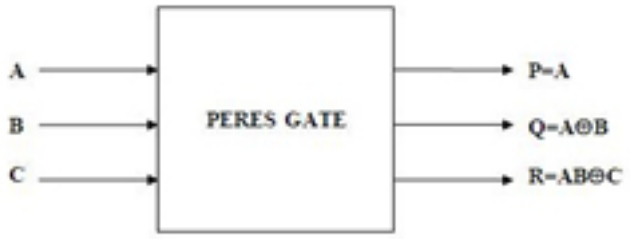

Fig 2 PERES gate

HNG gate:

Fig 3 shows a HNG Gate. The input vector is I (A, B, C, D) and the output vector is O (P, Q, R, S).The full adder using HNG is obtained with C= Cin and D=0.

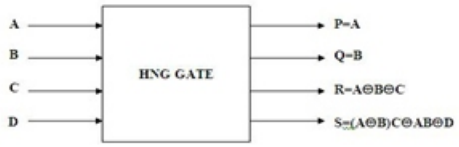

Fig 3 HNG gate

IV. VEDIC MULTIPLIER:

The "Urdhva Tiryagbhyam" Sutra is a general multiplication formula applicable to all cases of multiplication such as binary, hex, decimal and octal. The Sanskrit word "Urdhva" means "Vertically" and "Tiryagbhyam" means "crosswise". Fig 4 shows an example of Urdhva Tiryagbhyam.

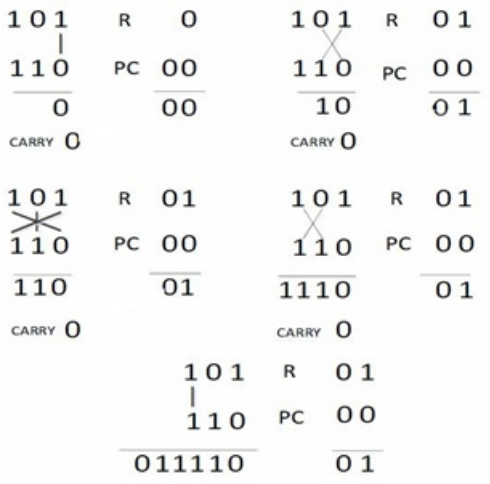

Fig 4 Example of Urdhva Tiryagbhyam algorithm

The partial products are generated parallel and concurrent additions of the partial products are done using this algorithm. Because of this the speed of the multiplier is increased considerably when compared to other techniques.The partial products are generated parallel and concurrent additions of the partial products are done using this algorithm. Because of this the speed of the multiplier is increased considerably when compared to other techniques.

V. VEDIC MULTIPLIERS USING REVERSIBLE LOGIC:

A .Design of 2x2 Urdhva Tiryakbhayam multiplier

The 2 X 2 UT multiplier using conventional logic will have 4 outputs. The logical expressions are given below.

q0= a0.b0

q1= (a1.b0) xor (a0.b1)

q2= (a0.a1.b0.b1) xor (a1.b1) q3= a0.a1.b0.b1

The reversible logic implementation of the above expressions requires four peres gate and one Feynmen (CNOT) gate. The reversible logic implementation of 2 X 2 UT multiplier is shown in the Fig 5. The quantum cost of the 2X2 Urdhva Tiryakbhayam Multiplier is found to be 21. The number of garbage outputs is 9 and number of constant inputs is 4.

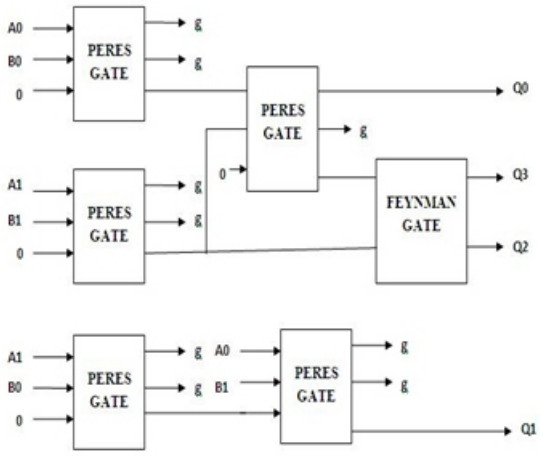

Fig 5 A 2 X 2 Urdhva Tiryagbhyam multiplier Unit

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B. Design of 4x4 Urdhva Tiryakbhayam multiplier:

The Reversible 4X4 Urdhva Tiryakbhayam Multiplier design emanates from the 2X2 multiplier. The block diagram of the 4X4 Vedic Multiplier is presented in the figure 6. It consists of four 2X2 multipliers each of which procures fourbits as inputs; two bits from the multiplicand and two bits fromthe multiplier. The lower two bits of the output of the first 2X2multiplier are entrapped as the lowest two bits of the final result of multiplication. Two zeros are concatenated with the upper two bits and given as input to the four bit ripple carry adder. The other four input bits for the ripple carry adder are obtained from the second 2X2 multiplier. Likewise the outputs of the third and the terminal 2X2 multipliers are given as inputs to the second four bit ripple carry adder. The outputs of these four bit ripple carry adders are in turn 5 bits each which need to be summed up. This is done by a five bit ripple carry adder which generates a six bit output. These six bits form the upper bits of the final result.

Design of ripple carry adder The design shown in [12] consists of only HNG gates. The number of HNG gates is 4 if the ripple carry adder is used in the second stage or five if the ripple carry adder is used in the last stage of the 4X4 UT Multiplier. The ripple carry adder can be modified as under. Since for any ripple carry adder the input carry for the first full adder is zero, this implicitly means the first adder is a half adder. Thus a Peres gate can efficiently replace a HNG. This cut down the quantum cost by two for any ripple carry adder and the garbage output by one. The constant inputs and the gate count remain unchanged.

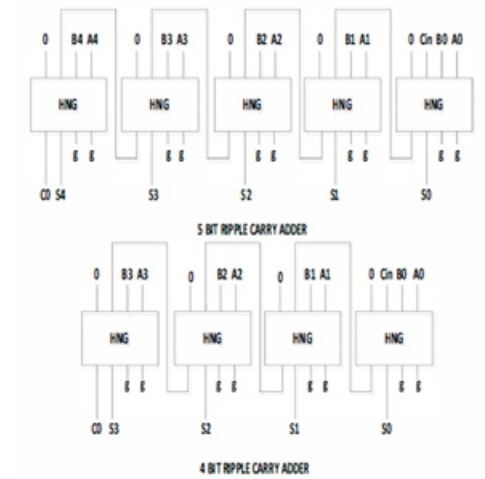

Fig 6 Ripple Carry Adders

Fig 7 A 4 X 4 Urdhva Tiryagbhyam multiplier Unit

C.Design of 8x8 Urdhva Tiryakbhayam multiplier:

The block diagram for proposed multiplier is shown in the figure 10. As we are using binary numbers in digital signal processing applications we have implemented for binary system. The multiplication can be done using the 4x4 multiplier and bit adders. This can be used for the multiplication of 255 number of bits. In this paper, we have presented a 8x8 architecture applying the Urdhava-Triyagbhyam Algorithm. In the figure , the two inputs a and b represents the 8 bit multiplier and 8 bit multiplicand respectively. of ripple carry adders The ripple carry adder is consummated (realized) using the HNG Gate. The number of bits that need to be ripple carried verdicts the number of HNG gates to be used. Thus a 8 bit ripple carry adder needs 8 HNG gates and the 9 bit adder requires 9 HNG gates. This design also does not take into consideration the fan out gates. Here "a" and "b" are two numbers to be multiplied and "y" is the product. With this design we are now ready to code this in verilog easily using reversible gates. To make the design more modular we write code for gates first and then instantiate it to have the final product.

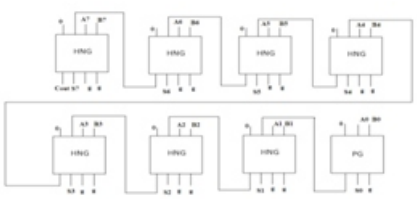

Fig 8 8-bit Ripple Carry Adder

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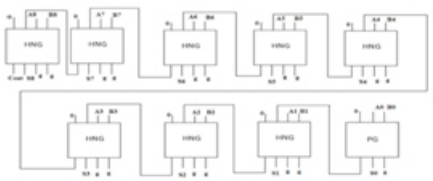

Fig 9 9-bit Ripple Carry Adder

Fig 10 A 8X8 Urdhva Tiryagbhyam multiplier

VI.EVALUATION:

The design of the reversible 2,4,8 bit multiplier is logically verified using XILINX 10.1 and MODELSIM SE 6.3. Synthesis and Implementation is done using Xilinx Spartan-3E Fpga Board of device family xc3s500e-4-fg320.The simulation results are as shown in figures.

Results:

In this section we show results for the Vedic multiplier based on UT . Multiplier based on UT Algorithm utilizes smaller area and produces littler delay than the conventional multiplier. The synthesis results shows that thetotal combinational path delay is 23.576ns.The memory used is 218520 kilobytes.

Simulation Results for 8 bit Multiplication:

For inputs a= '111111111' and b='11111111' and output m is the product of a and b .

Simulation Results for 4 bit Multiplication:

For inputs a= '1111' and b='1111' and output m is the product of a and b .

Simulation Results for 2 bit Multiplication:

For inputs a= '1111' and b='1111' and output 'i' is the product of a and b .

Schematic

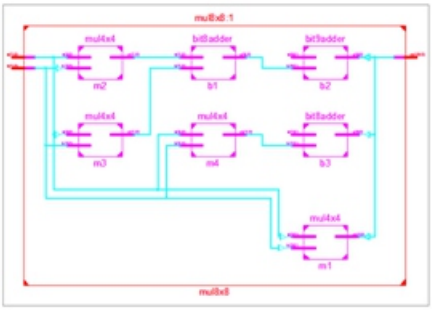

Fig:RTL Schematic

VII CONCLUSION:

This paper presents the Urdhva Tiryakbhayam Vedic Multiplier realized using reversible logic gates. First 2X2 UT multiplier is designed using Peres gate and Feynmen gate.

The ripple carry adders which were required for adding the partial products were constructed using HNG gates. This design has high speed, smaller area and less power consumption when compared with other reversible logic multipliers.

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