Design of Vedic multipliers for High Speed, Low Power using OptimisedReversible Logic Gate

Umarani.U.Joshi
M.Tech(VLSI),
Avanthi Institute.

N.Ashok Kumar, M.Tech
Associate Professor, & HOD,
ASRA, Hyderabad.

Abstract:

A systems performance is generally determined by the speed of the multiplier since multiplier is one of the key hardware component in high performance systems such as FIR filters, digital signal processors and microprocessors etc. Multipliers have large area, long latency and consume considerable power. Hence good multiplier architecture increases the efficiency and performance of a system. Vedic multiplier is one such high speed, low area multiplier architecture. Further implementing this in reversible logic reduces power. In this paper a 4 X 4 Vedic multiplier is designed using reversible logic gates which is efficient in terms of constant inputs, garbage outputs, quantum cost, area, speed and power. The design is simulated using Verilog.

I. INTRODUCTION:

Vedic mathematics is an ancient Indian mathematical technique based on 16 sutras. The sutras of Vedic Mathematics are the software for the cosmic computer that runs this universe. Vedic Mathematics introduces the wonderful applications to Arithmetical computations, theory of numbers, compound multiplications, algebraic operations, factorizations, simple quadratic and higher order equations, simultaneous quadratic equations, partial fractions, calculus, squaring, cubing, square root, cube root, coordinate geometry and wonderful Vedic Numerical code. The multipliers are the most important part of all digital signal processors; they are very important in realizing many important functions such as fast Fourier transforms and convolutions. Since a processor spends considerable amount of time in performing multiplication, an improvement in multiplication speed can greatly improve system performance. Multiplication can be implemented using many algorithms such as array, booth, carry save, and Wallace tree algorithms.

Reversible logic is a promising area of study with regard to the future low power technology. It has applications in various research areas such as optical computing, low power CMOS design, DNA computing, quantum computing, thermodynamic technology, bioinformatics and nanotechnology.This paper proposes the implementation of reversible logic UrdhavaTriyagbhyam multiplier which has two main features. One is implementing the multiplier using vedic sutra increases the speed of the multiplication. Second is the use of reversible logic reduces the area and the hence the power dissipation. The paper is partitioned into six sections. Section II gives literature survey, Section III deals with the UrdhvaTiryakbhayam algorithm. Section IV explains reversible logic. Section V elaborates on the design aspects of Reversible UrdhvaTiryakbhayam Multiplier. Section VI compares the results of our design with the literature. Conc1usions and references follow.

II. LITERATURE REVIEW :

Energy dissipates whenever switching activity occurs in the CMOS circuits..Landauer's Principle [3] states that logical computations that are not reversible necessarily generate $k*T*ln(2)$ joules of heat energy, where k is the Boltzmann's Constant k=1.38xl0-23 J/K, T is the absolute temperature at which the computation is performed. Although this amount of heat appears to be small, Moore's Law predicts exponential growth of heat generated due to information lost, which will be a noticeable amount of heat loss in next decade. Bennett showed that zero energy dissipation would be possible only if the network consists of reversible logic gates, Thus reversibility will become an essential property in future circuit design technologies. Reversible circuits are those circuits that do not loose information. Reversible computation in a system can be performed only when the system comprises of reversible gates. In paper [6] H. Thapliyal and M.B. Srinivas designed the multiplier using two units; one is the partial product generation unit constructed using Fredkin gates

and other the summing unit constructed using 4x4 TSG gates. [7] has proposed a design of reversible multiplier which makes use of Peres gate for generation of partial products as compared to [10], which uses Fredkin gates. For the construction of adders the HNG gate was devised.[15] Proposes low quantum cost realization of reversible multipliers which mainly uses Peres full adder gate (PFAG) for its design. It also uses Peres gates for the generation of partial products.

III. REVERSIBLE LOGIC GATE :

Reversible circuits are those circuits that do not loose information. Reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector, and vice versa, that is, there is a one-to-one mapping between input and output vectors. Thus, an NXN reversible gate can be represented as

$Iv = (I_1, I_2, I_3, I_4, \ldots\ldots\ldots\ldots\ldots IN)$
$Ov = (O_1, O_2, O_3, \ldots\ldots\ldots\ldots\ldots ON)$.

Where Iv and Ov represent the input and output vectors respectively.
The reversible circuit/gate has the following characteristics [2]:

• has equal number of inputs and outputs .
• the gate output, which is not used as primary output in the circuit is called garbage output .
• the input which is used as control input to the gates is called constant/garbage input .
• the fan-out of each gate is equal to one. A copying circuit is used if two copies of a signal are required .
• the resulting circuit is acyclic .

An efficient design in reversible logic should have the following features: (a) use minimum number of reversible logic gates, (b) should have less number of garbage outputs (c) less number of constant inputs and (d) minimization of quantum cost. The basic reversible logic gates that are used in this design are shown below. oFeynman gate:
Fig 1 shows a 2*2 Feynman gate. The input vector is I (A, B) and the output vector is O (P, Q). The outputs are defined by P=A, Q=AB. Quantum cost of a Feynman gate is 1.
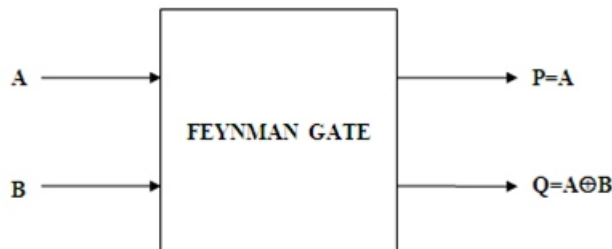

Peres gate:

Fig 2 shows a 3*3 Peres gate [4]. The input vector is I (A, B, C) and the output vector is O (P, Q, R). The output is defined by P = A, Q = AB and R=ABC. Quantum cost of a Peres gate is 4. In the proposed design Peres gate is used because of its lowest quantum cost.
oHNG gate:

Fig 3 shows a HNG Gate. The input vector is I (A, B, C, D) and the output vector is O (P, Q, R, S).The full adder using HNG is obtained with C= Cin and D=0.
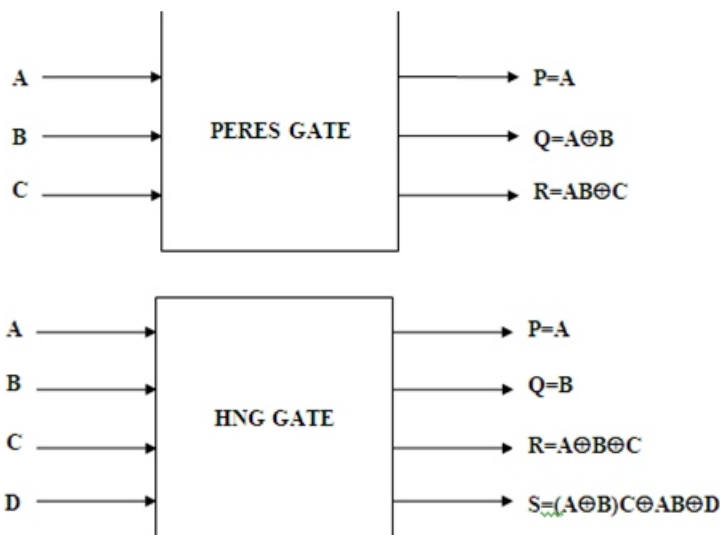
IV. VEDIC MULTIPLIER :

The "UrdhvaTiryagbhyam" Sutra is a general multiplication formula applicable to all cases of multiplication such as binary, hex, decimal and octal. The Sanskrit word "Urdhva" means "Vertically" and "Tiryagbhyam means "crosswise". Fig 4 shows an example of UrdhvaTiryagbhyam.
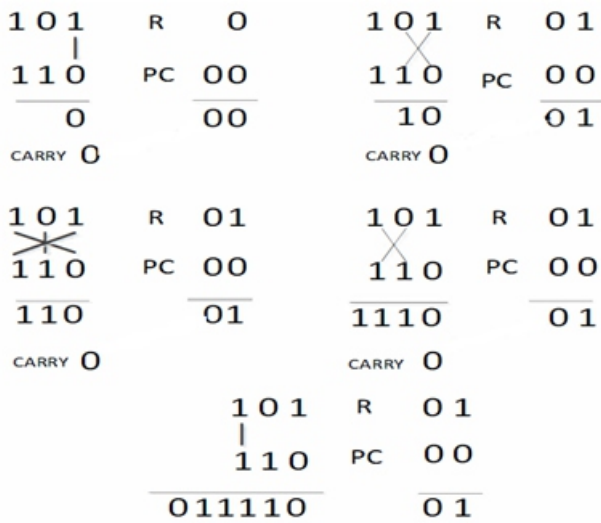
Fig 4 Example of UrdhvaTiryagbhyam algorithm

The partial products are generated parallel and concurrent additions of the partial products are done using this algorithm. Because of this the speed of the multiplier is increased considerably when compared to other techniques.

V. VEDIC MULTIPLIER USING REVERSIBLE LOGIC :

The 2 X 2 UrdhvaTiryagbhyam multiplier using conventional logic will have 4 outputs. The logical expressions are given below.

$q_0 = a_0.b_0$

$q_1 = (a_1.b_0)$ xor $(a_0.b_1)$

$q_2 = (a_0.a_1.b_0.b_1)$ xor $(a_1.b_1)$

$q_3 = a_0.a_1.b_0.b_1$

The reversible logic implementation of the above expressions requires four peres gate and one Feynmen (CNOT) gate. The reversible logic implementation of 2 X 2 UT multiplier is shown in the Fig 5. The quantum cost of the 2X2 UrdhvaTiryakbhayam Multiplier is found to be 21. The number of garbage outputs is 9 and number of constant inputs is 4. The partial products generated using the 2 X 2 UT multiplier are need to be added using the four bit adder. The four bit ripple carry adder unit was designed using the HNG reversible gate. The four bit ripple carry adder unit using HNG gate is shown in the Fig 7. The quantum cost of 4 bit adder unit using HNG gate is 24. The number of garbage output is 8 and constant input is 4.
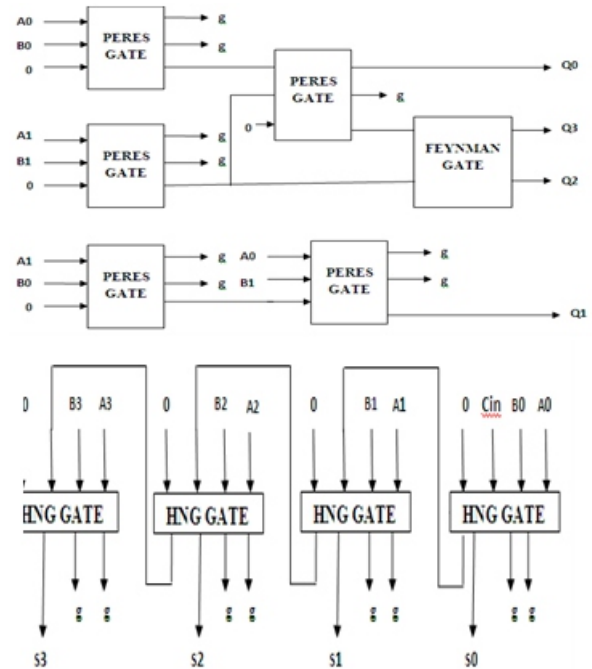
The architecture of 4 X 4 UrdhvaTiryagbhyam multiplier circuit is shown in the fig 7.It consist of four 2X 2 UT multiplier unit and three 4 bit binary adders.

VI. RESULTS AND COMPARISON :

The design of the reversible 2x2 and 4x4 multipliers is logically verified using XILINX 9.2i. The simulation results and design summary are as shown in figures 6 and 7 respectively.

The design is also implemented using Spartan 3E kit. The device utilization summary is as follows.

Selected Device: 3s250Epq208-5

Number of Slices: 20 out of 3584 0%

Number of 4 input LUTs: 35 out of 7168 0%

Number of IOs: 17
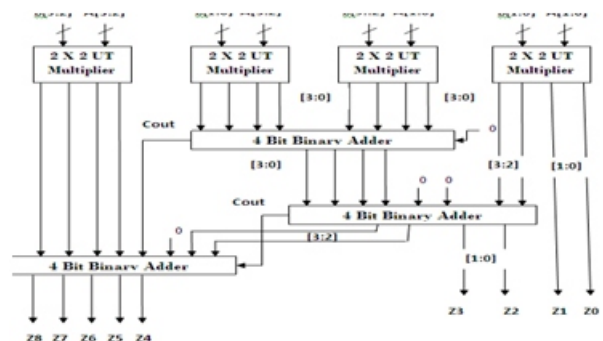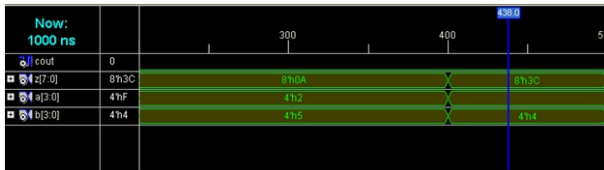
Number of bonded IOBs: 17 out of 141 12%

Fig . 7 A 4X4 UT multiplier using reversible logic gate

Fig. 8 Multiplication output

Since Vedic multiplier is designed the delay has been considerably reduced to 16.910 ns. For the array reversible logic multiplier is delay is found to be 22.035ns. The gate count is also reduced to 35 instead of 52 for the array reversible logic multiplier. The power consumption is found to be 52 mW.

Fig . 8 Performance measures

The comparison of Array multiplier & Vedic multiplier designed using HNG & Peres logic gate is given below.

TABLE I
COMPARISION OF ARRAY AND VEDIC MULTIPLIER

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Parameter	Array multiplier	Vedic multiplier
No. of gates	52	35
Number of slices	28	20
Constant inputs	56	29
Garbage output	56	62
Delay	22.035ns	16.910ns
Total equivalent gate count	318	210
Power	56mW	52mW
Quantum cost	208	162

Thus we can say that the design is optimized in terms of area, speed, power and quantum cost

VII. CONCLUSION :

This paper presents the UrdhvaTiryakbhayam Vedic Multiplier realized using reversible logic gates. First 2X2 UT multiplier is designed using Peres gate and Feynmen gate.

The ripple carry adders which were required for adding the partial products were constructed using HNG gates. This design has high speed, smaller area and less power consumption when compared with other reversible logic multipliers.

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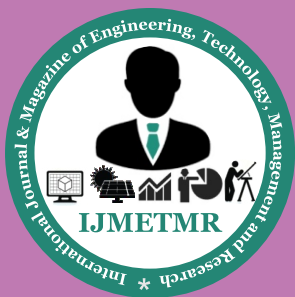
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