

## Design & Simulation of Reduced Switch Three-phase MLI for Induction Motor Applications

**Ch.Lakshmana Rao**

M.Tech Student Scholar,  
Department of Electrical & Electronics Engineering,  
AIMS Engineering College,  
Mummidivaram, East Godhavari (Dt),  
Andhra Pradesh, India.

**B.Vinod Kumar**

Assistant Professor,  
Department of Electrical & Electronics Engineering,  
AIMS Engineering College,  
Mummidivaram, East Godhavari (Dt),  
Andhra Pradesh, India.

### Abstract:

The MULTI-LEVEL INVERTER [MLI] system is very promising in ac drives, when both reduced harmonic contents and high power are required. In this paper, a new topology for symmetrical and asymmetrical multilevel inverter is introduced. Both types have many steps with fewer power electronic switches, which results in reduction of installation area and cost and have simplicity of control system. Firstly, we describe briefly the structural parts of the inverter then switching strategy and operational principles of the proposed inverter are explained and operational topologies are given.

A new algorithm for determination of dc voltage sources' magnitudes has also been presented. The fundamental frequency staircase modulation technique is easily used to generate the appropriate switching gate signals. For the purpose of increasing the number of voltage levels with fewer number of power electronic components, the structure of the proposed inverter is extended and different methods to determine the magnitudes of utilized dc voltage supplies are suggested. In this project, a new topology for cascaded multilevel converter based on sub multilevel converter units and full-bridge converters is proposed. The proposed topology significantly reduces the number of dc voltage sources, switches, IGBTs, and power diodes as the number of output voltage levels increases. Also, an algorithm to determine dc voltage sources magnitudes is proposed. To synthesize maximum levels at the output voltage, the proposed topology is optimized for various objectives, such as the minimization of the number of switches, gate driver circuits and capacitors, and blocking voltage on switches.

The analytical analyses of the power losses of the proposed converter are also presented, The operation and performance of the proposed multilevel converter have been evaluated. The proposed concept can be implemented with induction motor drive using MATLAB/SIMULINK software.

IndexTerms—Bidirectional switch, fundamental frequency staircase modulation, multilevel inverter.

### I. INTRODUCTION:

Multilevel inverters are composed of a number of power electronic switches and DC voltage sources that produce a stepped voltage waveform in its output. Generally, multilevel inverters are divided into three categories as follows: neutral-point clamped inverter (NPC), flying capacitor inverter (FC), and cascaded H-bridge inverter (CHB). These inverters can surrender higher power with lower dv/dt and di/dt in output waveform which is to reduce EMI noise and Size of the output filter. Therefore, using these inverters is very common nowadays. In recent years, several architectures have been proposed for cascade multilevel inverters. This kind of inverters can produce more voltage levels and also provide higher quality of power in its output.

As a result, this kind of inverter is considered more than other kinds of inverters. Cascade inverters are made of series separate single phase inverters with separate dc voltage sources. On the other hand, this inverter consists of a number of basic blocks (sub multilevel inverter) that each of these blocks has similar control system. One of the major advantages of this type of inverters is the ability of its modulation.

So, if an error occurs in one of the blocks, it can replace or fix by using a control system, but there are some disadvantages such as high number of dc voltage sources and power electronic switches. Increasing the number of power electronic switches leads to increase the number of driver circuits too. Both of these issues caused to increase in complexity, size, and cost of the circuit. Thus, reducing the number of power electronic switches is very vital and should be considered. Some applications for these new converters include industrial drives, flexible ac transmission systems (FACTS), and vehicle propulsion. One area where multilevel converters are particularly suitable is that of renewable photovoltaic energy that efficiency and power quality are of great concerns for the researchers.

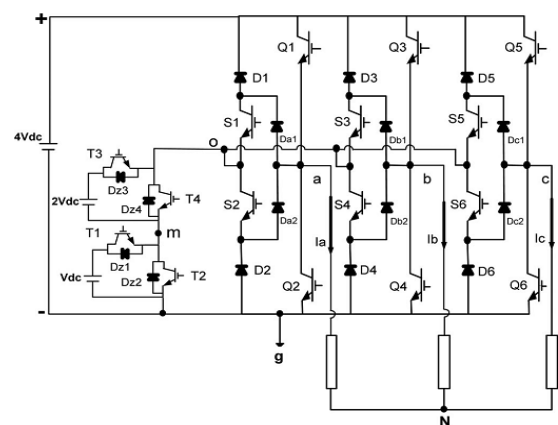
Some new approaches have been recently suggested such as the topology utilizing lowswitching-frequency high-power devices. Although the topology has some modification to reduce output voltage distortion, the general disadvantage of this method is that it has significant low-order current harmonics. The purpose of improving the performance of the conventional single- and three-phase inverters, different topologies employing different types of bidirectional switches. Comparing to the unidirectional one, bidirectional switch is able to conduct the current and withstanding the voltage in both directions. Bidirectional switches with an appropriate control technique can improve the performance of multilevel inverters in terms of reducing the number of semiconductor components, minimizing the withstanding voltage and achieving the desired output voltage with higher levels.

Based on this technical background, this paper suggests a novel topology for a three-phase five-level multilevel inverter. The number of switching devices, insulated-gate driver circuits, and installation area and cost are significantly reduced. The magnitudes of the utilized dc voltage supplies have been selected in a way that brings the high number of voltage level with an effective application of a fundamental frequency staircase modulation technique. Extended structure for N-level is also presented and compared with the conventional well-known multilevel inverters. Simulation results are explained.

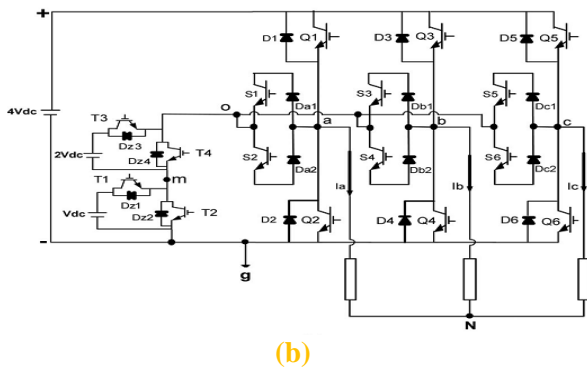
## II. PROPOSED CONFIGURATION:

Fig. 1(a) and (b) shows the typical configuration of the proposed three-phase five-level multilevel inverter. Three bidirectional switches ( $S1-S6$ ,  $Da1-Dc2$ ), two switches–two diodes type, are added to the conventional three-phase two-level bridge ( $Q1-Q6$ ). The function of these bidirectional switches is to block the higher voltage and ease current flow to and from the midpoint (o). A multilevel dc link built by a single dc voltage supply with fixed magnitude of  $4V_{dc}$  and CHB having two unequal dc voltage supplies of  $V_{dc}$  and  $2V_{dc}$  are connected to (+, -) bridge terminals.

Based on the desired number of output voltage levels, a number of CHB cells are used. Since the proposed inverter is designed to achieve five voltage levels, the power circuit of the CHB makes use of two series cells having two unequal dc voltage supplies. In each cell, the two switches are turned ON and OFF under inverted conditions to output two different voltage levels. The first cell dc voltage supply  $V_{dc}$  is added if switch  $T1$  is turned ON leading to  $V_{mg} = +V_{dc}$  where  $V_{mg}$  is the voltage at node (m) with respect to inverter ground (g) or bypassed if switch  $T2$  is turned ON leading to  $V_{mg} = 0$ . Likewise, the second cell dc voltage supply  $2V_{dc}$  is added when switch  $T3$  is turned ON resulting in  $V_{om} = +2V_{dc}$  where  $V_{om}$  is the voltage at midpoint (o) with respect to node (m) or bypassed when switch  $T4$  is turned ON resulting in  $V_{om} = 0$ . The peak voltage rating of the switches of the conventional two-level bridge ( $Q1-Q6$ ) is  $4V_{dc}$  whereas the bidirectional switches ( $S1-S6$ ) have a peak voltage rating of  $3V_{dc}$ . In CHB cells, the peak voltage rating of second cell switches ( $T3$  and  $T4$ ) is  $2V_{dc}$  while the peak voltage rating of  $T1$  and  $T2$  in the first cell is  $V_{dc}$ .



(a)



(b)

Fig. 1. Circuit diagram of the proposed three-phase five-level multilevel inverter.

TABLE I: Switching State  $S_a$  and Inverter Line-to-Ground Voltage  $V_{ag}$

$S_a$	Q1	S1	S2	Q2	T1	T2	T3	T4	$V_{ag}$
4	on	off	off	off	on	off	on	off	$+4V_{dc}$
3	off	on	on	on	off	on	off	off	$+3V_{dc}$
2	off	on	on	off	off	on	on	off	$+2V_{dc}$
1	off	on	on	off	on	off	off	on	$+V_{dc}$
0	off	off	off	on	on	off	off	on	0

It is easier to define the inverter line-to-ground voltages  $V_{ag}$ ,  $V_{bg}$ , and  $V_{cg}$  in terms of switching states  $S_a$ ,  $S_b$ , and  $S_c$  as

$$\begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} = \frac{4V_{dc}}{N-1} * \begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} \quad (1)$$

Where  $N=5$  is the maximum number of voltage levels.

The balanced load voltages can be achieved if the proposed inverter operates on the switching states depicted in Table II. The inverter may have 24 different modes within a cycle of the output waveform. According to Table II, it can be noticed that the bidirectional switches operate in 18 modes. For each mode, there is no more than one bidirectional switch in on state.

As a result, the load current commutates over one switch and one diode (for instance: in (410), the load current  $I_b$  can flow in S3 and Db1 or S4 and Db2). Since some insulated gate bipolar transistors (IGBTs) share the same switching gate signals, the proposed configuration significantly contributed in reducing the utilized gate driver circuits and system complexity. The inverter line-to-line voltage waveforms  $V_{ab}$ ,  $V_{bc}$ , and  $V_{ca}$  with corresponding switching gate signals are

depicted in Fig. 2 where  $V_{ab}$ ,  $V_{bc}$ , and  $V_{ca}$  are related to  $V_{ag}$ ,  $V_{bg}$ , and  $V_{cg}$  by

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} * \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} \quad (2)$$

The inverter line-to-neutral voltages  $V_{aN}$ ,  $V_{bN}$ , and  $V_{cN}$  may be expressed as

$$\begin{bmatrix} V_{aN} \\ V_{bN} \\ V_{cN} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} * \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} \quad (3)$$

It is useful to recognize that the inverter voltages at terminals a, b, and c with respect to the midpoint (o) are given by

$$\begin{bmatrix} V_{ao} \\ V_{bo} \\ V_{co} \end{bmatrix} = \begin{bmatrix} V_{ag} \\ V_{bg} \\ V_{cg} \end{bmatrix} - \begin{bmatrix} V_{og} \\ V_{og} \\ V_{og} \end{bmatrix} \quad (4)$$

Where  $V_{og}$  is the voltage at midpoint(o) with respect to ground (g).  $V_{og}$  routinely fluctuates among three different voltage values  $V_{dc}$ ,  $2V_{dc}$ , and  $3V_{dc}$  as follows:

$$V_{og} = \begin{cases} V_{dc}, & \text{if } S_a + S_b + S_c \leq 5 \\ 2V_{dc}, & \text{if } S_a + S_b + S_c = 6 \\ 3V_{dc}, & \text{if } S_a + S_b + S_c \geq 7. \end{cases} \quad (5)$$

TABLE II: SWITCHING STATES SEQUENCE OF THE PROPOSED INVERTER WITHIN ONE CYCLE

$S_a S_b S_c$	Period T [s]	ON switches Leg a	ON switches Leg b	ON switches Leg c	ON switches cascaded half-bridge	$V_{ag}$ [V]	$V_{bg}$ [V]	$V_{cg}$ [V]
400	0	Q1	Q4	Q6	T1, T4	$4V_{dc}$	0	0
410	0	Q1	S3, S4	Q6	T1, T4	$4V_{dc}$	$2V_{dc}$	0
420	0	Q1	S3, S4	Q6	T2, T3	$4V_{dc}$	$2V_{dc}$	0
430	0	Q1	S3, S4	Q6	T1, T3	$4V_{dc}$	$2V_{dc}$	0
440	0	Q1	Q4	Q6	T1, T3	$4V_{dc}$	$2V_{dc}$	0
400	0	S1, S2	Q3	Q6	T1, T3	$4V_{dc}$	$2V_{dc}$	0
340	0	S1, S2	Q3	Q6	T2, T3	$4V_{dc}$	$2V_{dc}$	0
300	0	S1, S2	Q3	Q6	T1, T4	$4V_{dc}$	0	0
040	0	Q2	Q3	Q6	T1, T4	0	$4V_{dc}$	0
041	0	Q2	Q3	S5, S6	T1, T4	0	$4V_{dc}$	$2V_{dc}$
042	0	Q2	Q3	S5, S6	T2, T3	0	$4V_{dc}$	$2V_{dc}$
043	0	Q2	Q3	S5, S6	T1, T3	0	$4V_{dc}$	$2V_{dc}$
044	0	Q2	Q3	Q5	T1, T3	0	$4V_{dc}$	$2V_{dc}$
034	0	Q2	S3, S4	Q5	T1, T3	0	$4V_{dc}$	$2V_{dc}$
024	0	Q2	S3, S4	Q5	T2, T3	0	$4V_{dc}$	$2V_{dc}$
014	0	Q2	S3, S4	Q5	T1, T4	0	$4V_{dc}$	0
004	0	Q2	Q4	Q5	T1, T4	0	$4V_{dc}$	0
104	0	S1, S2	Q4	Q5	T2, T3	$2V_{dc}$	0	$4V_{dc}$
204	0	S1, S2	Q4	Q5	T1, T3	$2V_{dc}$	0	$4V_{dc}$
404	0	Q1	Q4	Q5	T1, T3	$4V_{dc}$	0	$4V_{dc}$
403	0	Q1	Q4	S5, S6	T1, T3	$4V_{dc}$	0	$2V_{dc}$
402	0	Q1	Q4	S5, S6	T2, T3	$4V_{dc}$	0	$2V_{dc}$
401	0	Q1	Q4	S5, S6	T1, T4	$4V_{dc}$	0	$2V_{dc}$

### III. SWITCHING ALGORITHM:

The staircase modulation can be simply implemented for the proposed inverter. Staircase modulation with selective harmonic is the most common modulation technique used to control the fundamental output voltage as well as to eliminate the undesirable harmonic components from the output waveforms. An iterative method such as the Newton-Raphson method is normally used to find the solutions to  $(N-1)$  nonlinear transcendental equations. The difficult calculations and the need of high performance controller for the real application are the main

disadvantages of such method. Therefore, an alternative method is proposed to generate the inverter's switching gate signals. It is easier to control the proposed inverter and achieve the required output voltage waveforms in terms of  $S_a$ ,  $S_b$ , and  $S_c$ . The operation of the proposed inverter, the switching states  $S_a$ ,  $S_b$ , and  $S_c$  are determined instantaneously. The on-time calculations of  $S_a$ ,  $S_b$ , and  $S_c$  directly depend on the instantaneous values of the inverter line-to-ground voltages. It is well known that the reference values of  $V_{ag}$ ,  $V_{bg}$ , and  $V_{cg}$  are normally given by

$$\begin{bmatrix} V_{ag\_ref} \\ V_{bg\_ref} \\ V_{cg\_ref} \end{bmatrix} = \frac{M_a * 4V_{dc}}{2} * \begin{bmatrix} \cos(wt) \\ \cos(wt - \frac{2\pi}{3}) \\ \cos(wt + \frac{2\pi}{3}) \end{bmatrix} + \frac{4V_{dc}}{2} * \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \quad (6)$$

Where  $w t$  is the electrical angle. Or

$$\begin{bmatrix} V_{ag\_ref} \\ V_{bg\_ref} \\ V_{cg\_ref} \end{bmatrix} = \frac{M_a * 4V_{dc}}{2} * \begin{bmatrix} \cos(wt) \\ \cos(wt - \frac{2\pi}{3}) \\ \cos(wt + \frac{2\pi}{3}) \end{bmatrix} + \frac{4V_{dc}}{2} * \left[ 1 - \frac{M_a}{6} \cos(3wt) \right] * \begin{bmatrix} 1 \\ 1 \\ 1 \end{bmatrix} \quad (7)$$

From (10), it can be noticed that the third harmonic component is added to the three-line-to-ground voltages. The third harmonic injection may increase the inverter fundamental voltage without causing over modulation. As a result,  $M_a$  can reach to 1.15 and  $S_a$ ,  $S_b$ , and  $S_c$  can be simply determined by integerizing the reference line-to-ground voltages as

$$\begin{bmatrix} S_a \\ S_b \\ S_c \end{bmatrix} = \text{integer} \left( \frac{N-1}{4V_{dc}} * \begin{bmatrix} V_{ag\_ref} \\ V_{bg\_ref} \\ V_{cg\_ref} \end{bmatrix} \right) \quad (8)$$

Comparison of the proposed modulation method with the staircase modulation with the selective harmonic method shows that the proposed modulation features less time and needs simple calculations.

**Table III: Switching State  $S_{a1}$  and Inverter Line-To-Ground Voltage  $V_{ag}$  at  $M_a < 0.9$  (Leg A)**

$S_{a1}$	Q1	S1	S2	Q2	T1	T2	T3	T4	$V_{ag}$
2	on	off	off	off	off	on	on	off	$+4V_{dc}$
1	off	on	on	off	off	on	on	off	$+2V_{dc}$
0	off	off	off	on	off	on	on	off	0

Since the proposed inverter has been designed to achieve five voltage levels, the modulation index must be within range  $0.9 \leq M_a \leq 1.15$ . For modulation index  $M_a < 0.9$ , only two dc voltage supplies  $4V_{dc}$  and  $2V_{dc}$  are utilized and the behavior of the proposed inverter becomes similar to the three-level multilevel inverter. Using (9)–(11) and substituting  $N=3$ , the inverter's operating switching states  $S_a$ ,  $S_b$ , and  $S_c$  at  $M_a < 0.9$  can be defined. The operation principle of the proposed inverter at  $M_a < 0.9$  is illustrated in Table III.

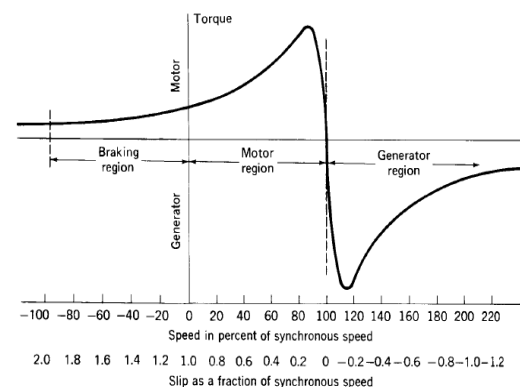
## V. INDUCTION MOTOR:

**Induction Motor (IM)** An induction motor is an example of asynchronous AC machine, which consists of a stator and a rotor. This motor is widely used because of its strong features and reasonable cost. A sinusoidal voltage is applied to the stator, in the induction motor, which results in an induced electromagnetic field. A current in the rotor is induced due to this field, which creates another field that tries to align with the stator field, causing the rotor to spin. A slip is created between these fields, when a load is applied to the motor.

Compared to the synchronous speed, the rotor speed decreases, at higher slip values. The frequency of the stator voltage controls the synchronous speed [12]. The frequency of the voltage is applied to the stator through power electronic devices, which allows the control of the speed of the motor. The research is using techniques, which implement a constant voltage to frequency ratio. Finally, the torque begins to fall when the motor reaches the synchronous speed. Thus, induction motor synchronous speed is defined by following equation,

$$=$$

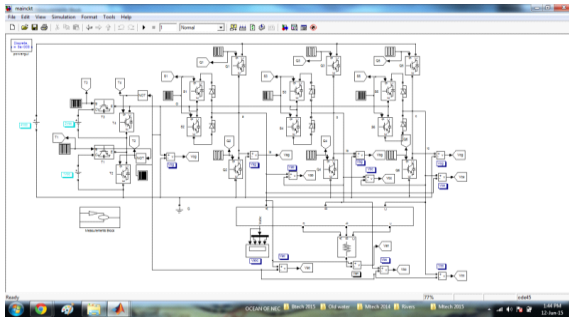
Where  $f$  is the frequency of AC supply,  $n$ , is the speed of rotor;  $p$  is the number of poles per phase of the motor. By varying the frequency of control circuit through AC supply, the rotor speed will change.



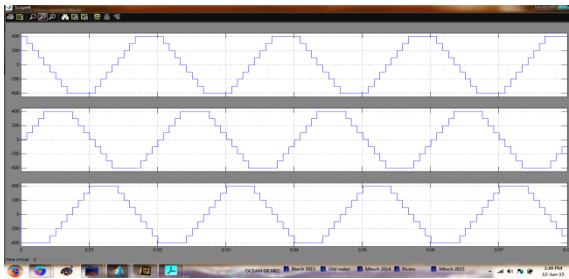
**Fig.2. Speed torque characteristics of induction motor**

## V. MATLAB/SIMULINK RESULTS

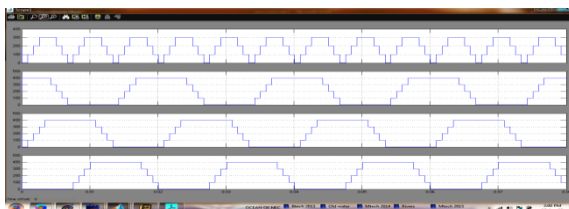




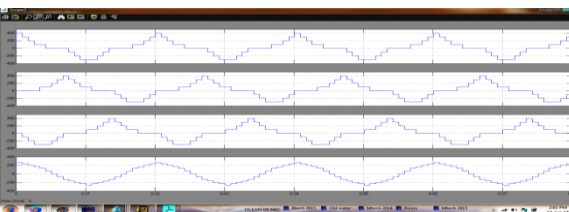
**Fig .3.Simulink model of the proposed three-phase five-level multilevel inverter.**



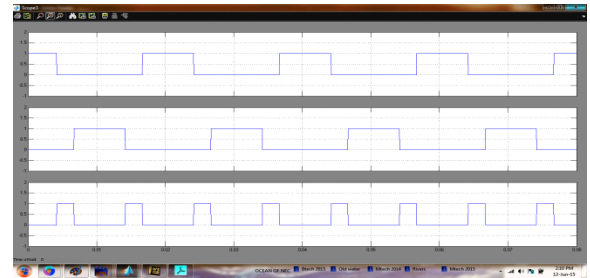
**Fig .4. Simulation output Vab,Vbc and Vca of proposed five level inverter.**



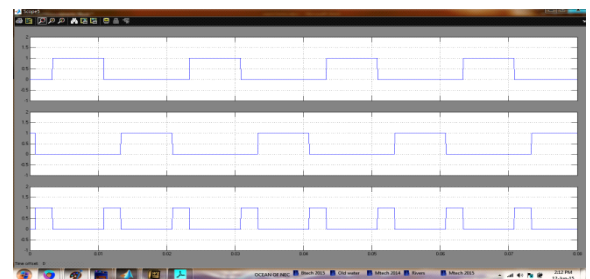
**Fig .5. Simulation output Vag,Vbg and Vcg of proposed five level inverter.**



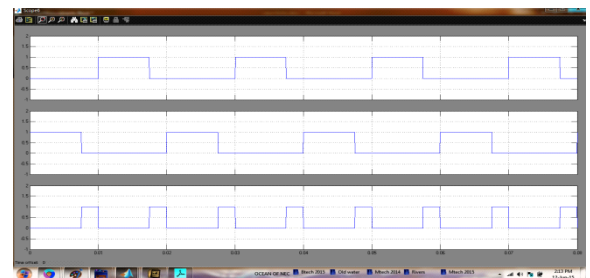
**Fig .6. Simulation output Vao,Vbo and Vco of proposed five level inverter.**



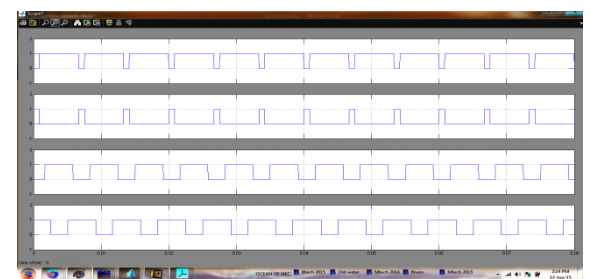
**Fig .7. Simulated output wave forms of Q1, Q2 and S1.**



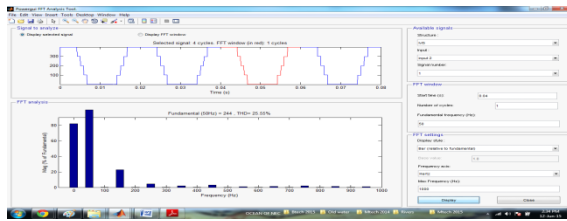
**Fig .8. Simulated output wave forms of Q3, Q4 and S3.**



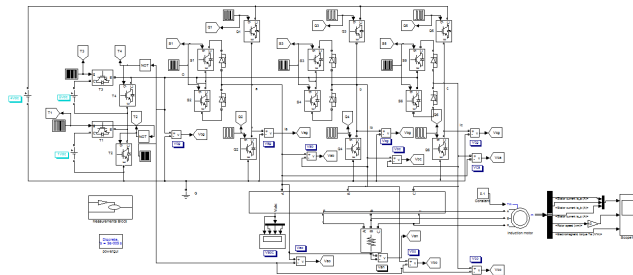
**Fig .9.Simulated output wave forms of Q5, Q6 and S5.**



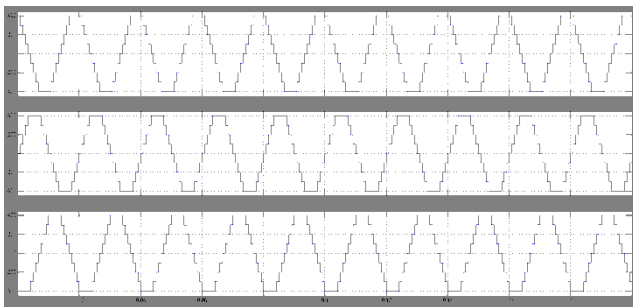
**Fig .10. Simulated output wave forms of T1, T2, T3 and T4.**



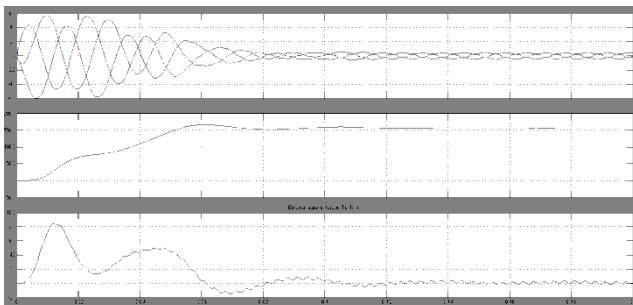
**Fig .11. Total Harmonic Distortion of 5 level phase voltage shows 25.55%.**



**Fig .12. Simulink model of the proposed three-phase five-level multilevel inverter with induction motor**



**Fig.13.Simulation result for three phase voltages**



**Fig.14.Simulation result for stator currents, speed and electromagnetic torque of induction motor**

## VI. CONCLUSION:

A new topology of the three-phase seven-level multilevel inverter was introduced. The suggested configuration was obtained from reduced number of power electronic components. Therefore, the proposed topology results in reduction of installation area and cost. The fundamental frequency staircase modulation technique was comfortably employed and showed high flexibility and simplicity in control. Moreover, the proposed configuration was extended to N-level with different methods. Furthermore, the method employed to determine the magnitudes of the dc voltage supplies was well executed. In order to verify the performance of the proposed multilevel inverter, the proposed configuration was simulated and its prototype was manufactured. The obtained simulation results met the desired output. Hence, subsequent work in the future may include an extension to higher level with other suggested methods. For purpose of minimizing THD%, a selective harmonic elimination pulse width modulation technique can be also implemented.

## REFERENCES:

- [1] J. A. Ferreira, "The multilevel modular DC converter,"IEEE Trans. Power Electron., vol. 28, no. 10, pp. 4460–4465, Oct. 2013.
- [2] K. Ilves et al., "A new modulation method for the modular multilevel converter allowing fundamental switching frequency,"IEEE Trans. Power Electron., vol. 27, no. 8, pp. 3482–3494, Aug. 2012.
- [3] W. Yong and W. Fei, "Novel three-phase three-level-stacked neutral point clamped grid-tied solar inverter with a split phase controller,"IEEE Trans. Power Electron., vol. 28, no. 6, pp. 2856–2866, Jun. 2013.
- [4] Y. Yuanmao and K. W. E. Cheng, "A family of single-stage switchedcapacitor-inductor PWM converters," IEEE Trans. Power Electron., vol. 28, no. 11, pp. 5196–5205, Nov. 2013.
- [5] N. A. Rahim et al., "Transistor-clamped H-bridge based cascaded multilevel inverter with new method of capacitor voltage balancing," IEEE Trans. Ind. Electron., vol. 60, no. 8, pp. 2943–2956, Aug. 2013.

- [6] I. Abdalla et al., "Multilevel DC-link inverter and control algorithm to overcome the PV partial shading," IEEE Trans. Power Electron., vol. 28, no. 1, pp. 14–18, Jan. 2013.
- [7] Z. Li et al., "A family of neutral point clamped full-bridge topologies for transformerless photovoltaic grid-tied inverters," IEEE Trans. Power Electron., vol. 28, no. 2, pp. 730–739, Feb. 2013.
- [8] L. Zixin et al., "A novel single-phase five-level inverter with coupled inductors," IEEE Trans. Power Electron., vol. 27, no. 6, pp. 2716–2725, Jun. 2012.
- [9] S. Mariethoz, "Systematic design of high-performance hybrid cascaded multilevel inverters with active voltage balance and minimum switching losses," IEEE Trans. Power Electron., vol. 28, no. 7, pp. 3100–3113, Jul. 2013.
- [10] H. Belkamel, S. Mekhilef, A. Masaoud, and M. Abdel Naiem, "Novel three phase asymmetrical cascaded multilevel voltage source inverter," IET Power Electron., vol. 6, pp. 1696–1706, 2013.
- [11] J. Meiet al., "Modular multilevel inverter with new modulation method and its application to photovoltaic grid-connected generator," IEEE Trans. Power Electron., vol. 28, no. 11, pp. 5063–5073, Nov. 2013.
- [12] S. Mekhilefet al., "Digital control of three phase three-stage hybrid multilevel inverter," IEEE Trans. Ind. Electron., vol. 9, no. 2, pp. 719–727, May 2013.
- [13] J. Mathewet al., "A hybrid multilevel inverter system based on dodecagonal space vectors for medium voltage IM drives," IEEE Trans. Power Electron., vol. 28, no. 8, pp. 3723–3732, Aug. 2013.
- [14] M. Saeedifard et al., "Operation and control of a hybrid seven-level converter," IEEE Trans. Power Electron., vol. 27, no. 2, pp. 652–660, Feb. 2012.
- [15] S. Mekhilef and A. Masaoud, "Xilinx FPGA based multilevel PWM single phase inverter," in Proc. IEEE Int. Conf. Ind. Technol., 2006, pp. 259–264.
- [16] E. A. Mahrous and S. Mekhilef, "Design and implementation of a multi level three-phase inverter with less switches and low output voltage distortion," J. Power Electron., vol. 9, pp. 593–603, 2009.
- [17] H. W. Ping, N. A. Rahim, and J. Jamaludin, "New three-phase multilevel inverter with shared power switches," J. Power Electron., vol. 13, pp. 787–797, 2013.
- [18] S. Suroso and T. Noguchi, "Multilevel current waveform generation using inductor cells and H-bridge current-source inverter," IEEE Trans. Power Electron., vol. 27, no. 3, pp. 1090–1098, Mar. 2012.
- [19] M. F. Kangarlu and E. Babaei, "A generalized cascaded multilevel inverter using series connection of submultilevel inverters," IEEE Trans. Power Electron., vol. 28, no. 2, pp. 625–636, Feb. 2013.