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Generation of Built-In Broadside Test based on FPGA

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Abstract:

In the proposed method we test the C17 circuit by using Built in Self Test.This paper describes an on-chip test generation method for functional broadside tests. The hardware was base on the application of primary input sequences initial from a well-known reachable state, therefore using the circuit to produce additional reachable states. Random primary enter sequences were changed to avoid repeated synchronization and thus defer varied sets of reachable states. Functional broadside tests are two-pattern scan based tests that avoid over testing by ensuring that a circuit traverses only reachable states in the functional clock cycles of a check. These consist of the input vectors and the equivalent responses. They check for proper operation of a verified design by testing the internal chip nodes. Useful tests cover a very high percentage of modeled faults in logic circuits and their generation is the main topic of this method. Often, functional vectors are understood as verification vectors, these are used to verify whether the hardware actually matches its specification. Though, in the ATE world, any one vectors applied are understood to be functional fault coverage vectors applied during developing test. This paper show the on chip test Generation for a bench mark circuit using simple fixed hardware design with small no of parameters altered in the design for the generation of no of patterns. If the patterns of the input test vector results a fault simulation then circuit test is going to fail.

Keyword: BIST, ATE, Functional Vectors.

1.INTRODUCTION:

Functional broadside tests are two-pattern scan based tests that avoid over testing by ensuring that a circuit traverses only reachable states during the functional clock cycles of a test. In addition, the power dissipation during the fast functional clock cycles of functional broadside tests does not exceed that possible during functional operation. On-chip test generation has the added advantage that it reduces test data volume and facilitates at-speed test application.

This paper shows that on-chip generation of functional broadside tests can be done using a simple and fixed hardware structure, with a small number of parameters that need to be tailored to a given circuit, and can achieve high transition fault coverage for testable circuits. With the proposed on-chip test generation method, the circuit is used for generating reachable states during test application. This alleviates the need to compute reachable states offline.Over testing due to the application of two-pattern scan-based tests. Over testing is related to the detection of delay faults under non-functional operation conditions. One of the reasons for these non-functional operation conditions is the following. When an arbitrary state is used as a scan-in state, a two-pattern test can take the circuit through state-transitions that cannot occur during functional operation. As a result, slow paths that cannot be ensitized during functional operation may cause the circuit to fail. In addition, current demands that are higher than those possible during functional operation may cause voltage drops that will slow the circuit and cause it to fail. In both cases, the circuit will operate correctly during functional operation.

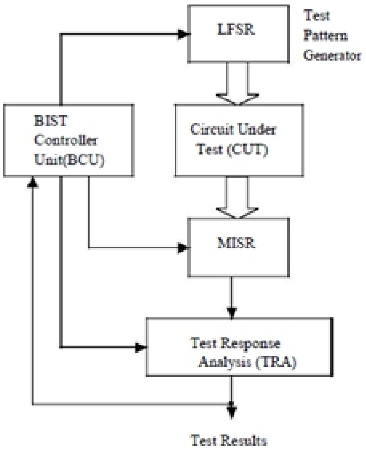


Figure : 1- Block Diagram Of BIST

Functional broadside tests ensure that the scan-in state is a state that the circuit can enter during functional operation, or a reachable state. As broadside tests, they operate the circuit in functional mode for two clock cycles after an initial state is scanned in. This results in the application of a two-pattern test.

Since the scan-in state is a reachable state, the two-pattern test takes the circuit through state-transitions that are guaranteed to be possible during functional operation. Delay faults that are detected by the test can also affect functional operation, and the current demands do not exceed those possible during functional operation. This alleviates the type of over testing. In addition, the power dissipation during fast functional clock cycles of functional broadside tests does not exceed that possible during functional operation.Test generation procedures for functional and pseudo-functional scan-based tests. The procedures generate test sets offline for application from an external tester. Functional scan-based tests use only reachable states as scan-in states. Pseudo-functional scan-based tests use functional constraints to avoid unreachable states that are captured by the constraints.This work considers the on-chip (or built-in) generation of functional broadside tests. On-chip test generation reduces the test data volume and facilitates at-speed test application.

2.EXISTING METHOD:

This section gives an overview about on-chip generation of functional broadside tests. The discussion in this paper assumes that the circuit is initialized into a known state before functional operation starts. Initialization may be achieved by applying a synchronizing sequence, by asserting a reset input, or by a combination of both. The initial state of the circuit is denoted by. The discussion also assumes that functional operation consists of the application of primary input sequences starting from state. With Sr, as the initial state for functional operation, Sr is a reachable state. In addition, the set of reachable states consists of every state such that there exists a primary input sequence that takes the circuit from too.

Since can be entered during functional operation starting from Sr.Si is a reachable state.It is possible to obtain reachable states on-chip by placing the circuit in state Sr and applying a primary input sequence A=a (0) a(1) a(2)……a(L-1) of length in functional mode. The circuit can be brought into state Sr by using a scan-in operation, or by using its initializing sequence. Let s(u) be the state that the circuit reaches at time unit under , for 0<=u<=L. We have that S(0)=Sr. In addition, S(u) is a reachable state for 0<=u<=L. Therefore, every state S(u) can be used as the initial state for a functional broadside test {s(u),a1,a2}, where S(u) plays the role of a scan-in state.

As in a broadside test, a1 and a2 are primary input vectors that are applied in two consecutive functional clock cycles starting from s(u) using a slow and a fast clock, respectively.In addition to producing reachable states, the primary input sequence A can also be used as a source for the primary input vectors of functional broadside tests. In particular, every subsequence of length two of defines a functional broadside test t(u) = (s(u),a(u),a(u+1)). By using a(u) and a(u+1) from A, it is possible to avoid the need for a different source for these primary input vectors during on-chip test generation.For illustration we consider ISCAS-89 benchmark with initial state Sr=000. The circuit is shown in Fig. 1. A primary input sequence for the circuit is shown in Table I. For every time unit, Table I shows the state s(u) and the primary input vector a(u). Table I yields the functional broadside tests t(0) = {000, 1001, 1110}, t(1) = {010, 1110, 0010},…. t(14) = { 101, 1111, 1110}.The proposed on-chip generation method of functional broadside tests is based on placing the circuit in the initial state, applying a primary input sequence, and using several of the functional broadside tests that can be extracted from in order to detect target faults. Next, we discuss how the application of A is affected by the need to observe fault effects created by a test t(u) = {s(u),a(u),a(u+1)}.

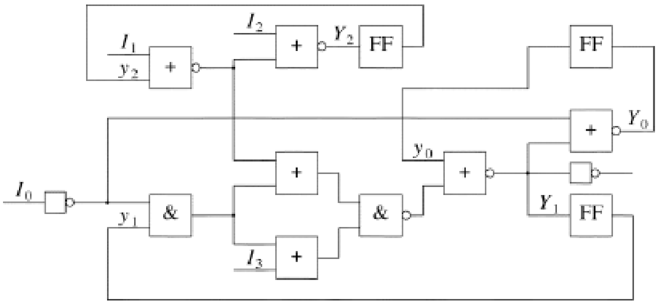


Figure:2-S27 BENCHMARK CIRCUIT

TABLE I
PRIMARY INPUT SEQUENCE FOR $s27$

u	$s(u)$	$a(u)$
0	000	1001
1	010	1110
2	100	0010
3	000	1001
4	010	1001
5	010	0010
6	010	1000
7	100	1101
8	101	1000
9	101	0111
10	000	1000
11	100	1001
12	100	1100
13	101	1101
14	101	1111
15	100	1110

At time unit the circuit is in state s(u). Applying a(u) and a(u+1) in functional mode will result in the application of t(u). A fault can be detected in one of the following two ways.

1) Based on the primary output vector z(u+1) obtained in response to a(u+1) if this vector is different from the expected fault free primary output vector.
2) Based on the final state s(u+2) of the test, if this state is different from the expected fault free state.

3.PROPOSED METHOD:

To better diagnose a failing CUT, the more unique output responses we get the more accurate a conclusion we can reach. The purpose of a DATPG system is to generate additional test vectors that target pairs of faults, which can produce different output responses for that pair, thus increasing the resolution of the diagnosis. The final fault candidate list can be narrowed down with such tests. Fault candidates are those faults that have same or similar signatures as observed signatures for a failing CUT.Although nearly all circuits are sequential, in testing/diagnosis they are transformed into combinational logic through scan design (refer to figure 2.8) or other DFT techniques.

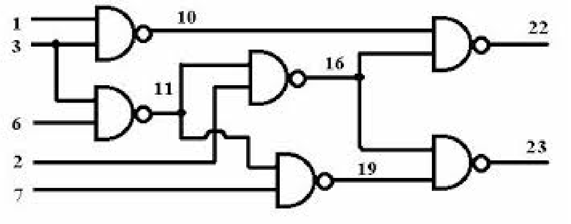


Figure:3- C17 BENCHMARK CIRCUIT

Since the detection of this fault and distinguishing of the targeted fault pair are equivalent problems (proved in the previous section using Boolean algebra) fault equivalence checks can be transferred to redundancy identification. The advantage is that redundancy identification is a well researched area for conventional ATPG algorithms. We can use ATPG to do equivalence check to aid the diagnosis process without any additional effort. These diagnosis problems can be easily solved using highly developed testing tools. And the complexity of diagnosis is reduced to a level similar to that of fault testing. In [12, 13, 100] the author presents equivalence check techniques based on implication of faulty values and evaluation of faulty functions in cones of dominator gates of fault pairs.

The major limitations are a special tool is needed and not all equivalence can be identified.To generate diagnostic tests we need a coverage criterion to measure how good the generated test vectors are. This would be similar to the fault coverage (FC) used in conventional ATPG systems where fault detection is the objective. 100% F C means that all modeled faults are detected by the test set. In [6] diagnostic resolution (DR) is introduced to measure the quality of a given test set for fault diagnosis. DR is defined as:

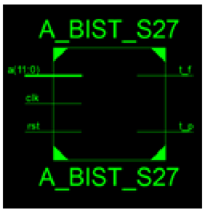
$$DR = \frac{Total\ number\ of\ faults}{Number\ of\ syndromes}$$

Fault syndrome is the same as fault signature. DR represents the average number of faults per fault class (faults with the same syndrome/signature). A perfect DR of 1.0 is achieved if all faults have unique syndromes and all equivalent faults are identified (only one fault from an equivalent class is kept in the calculation, others are dropped). Here is a simple example for calculating DR. In Table 4.1 signatures before "/" are from a pass-fail dictionary and those after "/" are from a full-response dictionary. For the pass-fail dictionary we have 3 unique signatures: (111, 010, 001). Thus DR = 4/3 = 1.33. For full-response there are 4 different signatures: (101010, 001000, 000001, 000010), and DR = 4/4 = 1.0. For perfect detection tests g0 will be a null set and for perfect diagnostic tests, n = N, where N is the total number of faults. We define diagnostic 33 coverage, DC, as:

$$DC = \frac{Number\ of\ detected\ fault\ groups}{Total\ number\ of\ faults} = \frac{n}{N}$$

Overview: We are comparing the S27 & C17 circuits which was designed and tested by using Built-In Self Test and analyzing its Power , Area, & Delay Reports.

4.RESULTS & DISCUSSION
4.1.EXISTNG METHOD(BIST Using S27)



a)

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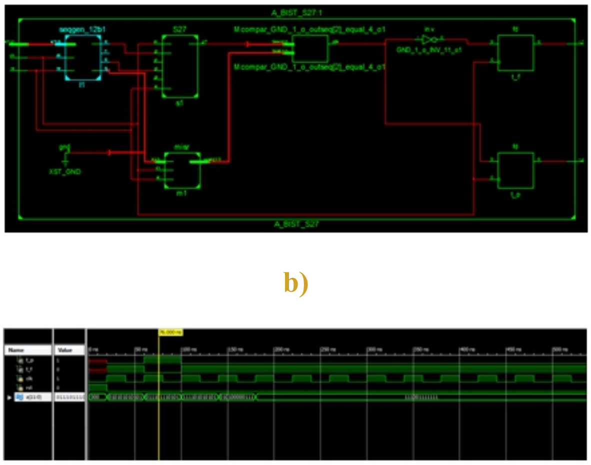
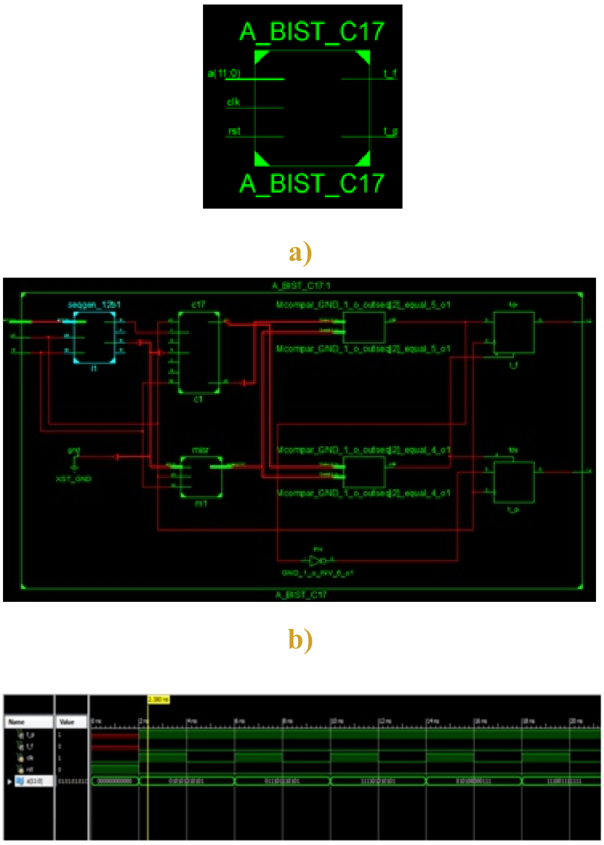


b)

c)

Figure:4- a) Block Diagram ,b) RTL Diagram , c) Waveform

4.2.PROPOSED METHOD (BIST Using C17)



a)

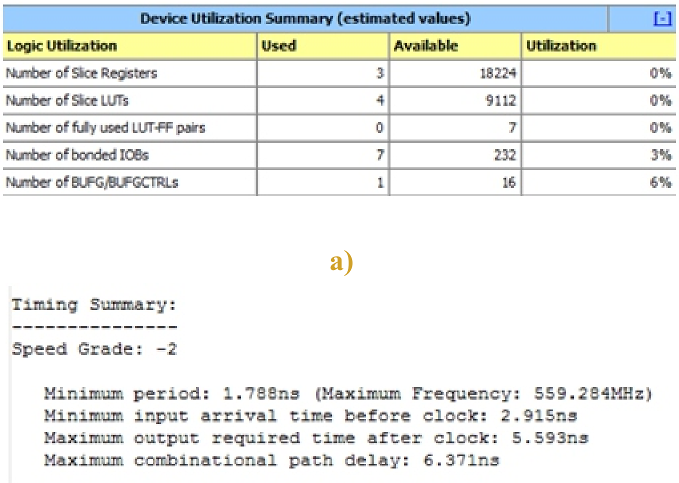
b)

c)

Figure :5- a) Block Diagram , b) RTL Diagram , c) Waveform

4.3.Area & Delay Reports

4.3.1.Existing Reports:



Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice Registers	3	18224	0%
Number of Slice LUTs	4	9112	0%
Number of fully used LUT-FF pairs	0	7	0%
Number of bonded IOBs	7	232	3%
Number of BUFG/BUFGCTRLs	1	16	6%

a)

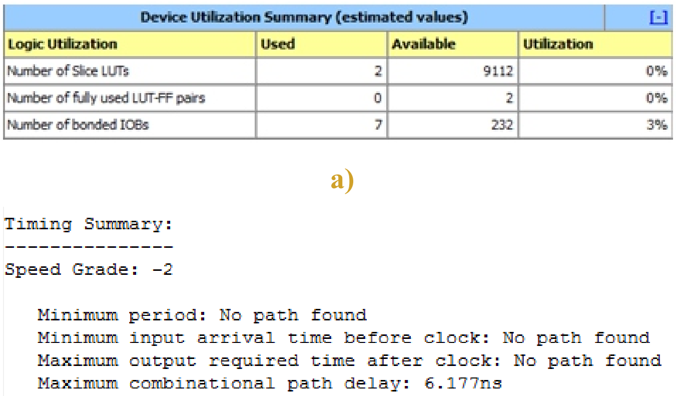
```
Timing Summary:
---------------
Speed Grade: -2

   Minimum period: 1.788ns (Maximum Frequency: 559.284MHz)
   Minimum input arrival time before clock: 2.915ns
   Maximum output required time after clock: 5.593ns
   Maximum combinational path delay: 6.371ns
```

b)

Figure :6- a)Area, b)Delay

4.3.2.Proposed Reports:



Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slice LUTs	2	9112	0%
Number of fully used LUT-FF pairs	0	2	0%
Number of bonded IOBs	7	232	3%

a)

```
Timing Summary:
---------------
Speed Grade: -2

   Minimum period: No path found
   Minimum input arrival time before clock: No path found
   Maximum output required time after clock: No path found
   Maximum combinational path delay: 6.177ns
```

b)

Figure:7- a)Area, b)Delay

5.CONCLUSION:

This paper described an on-chip test generation method for functional broadside tests. The hardwarewas based on the application of primary input sequences starting from a known reachable state, thus using the circuit to produce additional reachable states. Random primary input sequences were modified to avoid repeated synchronization and thus yield varied sets of reachable states. Two-pattern tests were obtained by using pairs of consecutive time units of the primary input sequences.

The hardware structure was simple and fixed, and it was tailored to a given circuit only through the following parameters: 1) the length of the LFSR used for producing a random primary input sequence; 2) the length of the primary input sequence; 3) the specific gates used for modifying the random primary input sequence; 4) the specific gate used for selecting applied tests; and 5) the seeds for the LFSR. The on-chip generation of functional broadside tests achieved high transition fault coverage for testable circuits.

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