ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

An Arithmetic and Logic Unit Optimized For Area and Power

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Abstract:

This paper presents a design of a 4-bit arithmeticlogic unit (ALU) by taking vantage of the concept of gated-iffusion input (GDI) technique. ALU is the most crucial andcore component of central processing unit as well as ofnumbers of embedded system and microprocessors. In this,ALU consists of 4x1 multiplexer, 2x1 multiplexer and fulladder designed to implements logic operations, such as AND,OR, etc. and arithmetic operations, as ADD and SUBTRACT.GDI cells are used in the design of multiplexers and full adderwhich are then associated to realize ALU. The simulation iscarried out Microwind 2.0 simulator using DSCH120nm technologies and compared with previous designsrealized with Pass transistor logic and CMOS logic. Thesimulation shows that the design is more efficient with lesspower consumption, less surface area and is faster ascompared to pass transistor and CMOS techniques.

Keywords:

GDI technique, ALU, Pass transistor gate.

I.INTRODUCTION:

In the era of growing technology and scaling of devices up to Nano-meter regime, the arithmetic logic circuits are to be designed with compact size, less power and propagation delay. Arithmetic operations are indispensable and basic functions for any high speed low power application digital signal processing, microprocessors, image processing etc. Addition is most important part of the arithmetic unit rather approximately all other arithmetic operation includes addition. Thus, the primary issue in the design of any arithmetic logic unit is to have low power high performance adder cell. There are various topologies and Methodologies proposed to design full adder cell efficiently.

This paper utilizes the concept of GDI technique in the design of ALU and its sub blocks as Multiplexer and Full adder. The rest of paper is organized as follows Section II describes previous works. Section III consists of the description of Gate Diffusion Input Technique. In section IV Arithmetic Logic Unit design, its operation and schematic is explained. Section V describes simulation result and analysis. At last conclusion is made in section VI.

II. PREVIOUS WORKS:

There are different types and designs of full adder which is discussed in various papers at state of the art level andprocess and circuit level. Twelve state of the art full adder cells are: conventional CMOS, CPL, TFA, TG CMOS,C2MOS, Hybrid, Bridge, FA24T, N-Cell, DPL and Mod2f. R. Shalem, E. John, and L.K. John, proposed a conventionalCMOS full adder consisting of 28 transistors [1]. Later, the number of transistor count is reduced to have less area andpower consumption.

A. Sharma, R Singh and R. Mehra, Member, IEEE, have improved performance with Transmission Gate Full adder using CMOS nano technology where 24 transistors are used [2]. The Complementary Passtransistor Logic (CPL) full Adder contains the 18 transistors. The power consumption of this structure is 2.5µw [3].A Transmission Function Full Adder (TFA) based on the transmission function theory has 16 transistors. The powerconsumption of this structure is 12µw. N-CELL contains the 14 transistors and utilizes the low power XOR/XNOR circuit.

The power consumption of this structure is 1.62µw. Mod2f Full Adder contains the 14 transistors, generates full swing XOR and XNOR signals by utilizing a pass transistor based DCVS circuit. The power consumption of this structure is 2.23µw [3]. Saradindu Panda, N. Mohan Kumar, C.K. Sarkar, optimized the full adder circuit to 18 Transistorusing Dual Threshold Node Design with Submicron Channel Length [4].

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T. Vigneswaran, B. Mukundhan, and P.Subbarami Reddy, designed 14 transistor high speed CMOS full adder and significantly improved threshold problem to50% [5]. Gate Diffusion Input Technique is a new method of reducing power dissipation, propagation delay with less area.T. Esther Rani, M. Asha Rani, Dr.RameshwarRao, designed an area optimized low power arithmetic and logic unit inwhich Arithmetic Logic Unit is implemented using logic gates, pass transistor logic, as well as GDI technique [6]. Manish Kumar, Md. Anwar Hussain, and L.L.K. Singh explained a Low Power High Speed ALU in 45nm UsingGDI Technique and Its Performance Comparison [7]. We have designed ALU in different way by using GDIcells to implement multiplexers and full adder circuit. The input and output sections consist of 4x1 and 2x1 multiplexersand ALU is implemented by using full adder.

III.GATE DIFUSSION INPUT TECHNIQUE:

Morgenshtein has proposed basic GDI cell shown in Fig.1 [8]. This is a new approach for designing low powerdigital combinational circuit.GDI technique is basically two transistor implementation of complex logic functions whichprovides in-cell swing restoration under certain operating condition. This approach leads to reduction in power consumption, propagation delay and area of digital circuits is obtained while having low complexity of logic design. Animportant feature of GDI cell is that the source of the PMOS in a GDI cell is not connected to VDD and the source of theNMOS is not connected to GND. Therefore GDI cell gives two extra input pins for use which makes the GDI design more flexible than CMOS design.

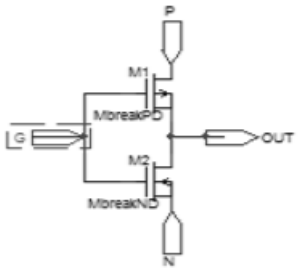

Fig. 1. Basic GDI Cell

There are three inputs in a GDI cell - G (common gateinput of NMOS and PMOS), P (input to the source/drain ofPMOS) and N (input to the source/drain of NMOS). Bulks ofboth NMOS and PMOS are connected to N and Prespectively.

Table 1 shows different logic functionsimplemented by GDI logic [8] based on different inputvalues. So, various logic functions can be implemented withless power and high speed with GDI technique as comparedto conventional CMOS design.

TABLE 1. LOGIC FUNCTIONS OF BASIC GDI CELL

S.No.	N I/P	P I/P	G I/P	Output	Function
1.	0	B	A	A'B	F_1
2.	B	1	A	A'+B	F_2
3.	1	B	A	A+B	OR
4.	B	0	A	AB	AND
5.	C	B	A	A'B+AC	MUX
6.	0	1	A	A'	NOT

A. Multiplexer:

Multiplexer is a digital switch. The multiplexer hasnumbers of input data lines and one output line. Theselection of a particular input line is controlled by a set ofselection line. There are '2n' input lines and 'n' selectionlines whose bit combinations determine which input isselected. Fig 2 shows implementation of basic 2x1multiplexer using GDI cell. The 4x1 multiplexer has four inputs, two selection lines and one output. Depending on thetwo selection lines, one output is selected at a time amongthe four input lines. Fig. 3 shows implementation of 4x1multiplexer using GDI cell.

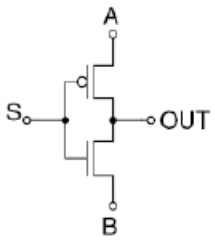

Fig. 2. 2x1 Multiplexer using GDI technique

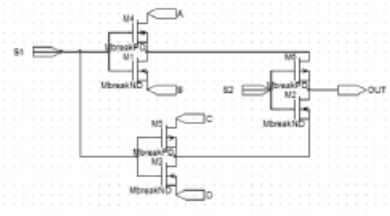

Fig 3. 4x1 Multiplexer using GDI technique

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B. XOR Gate:

The main building block of full adder circuit is XOR gatewhich gives sum output. So the overall performance of fulladder circuit can be improved by optimizing XOR gate.Fig.4 shows the implementation of XOR gate using GDItechnique [9]. It uses less number of transistors as comparedto conventional design of XOR gate using CMOS logicUnits.

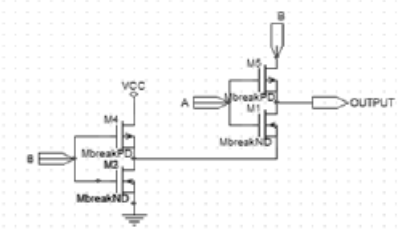

Fig. 4. GDI Based XOR Gate

C. Full Adder:

The Full Adder circuit adds three one-bit binary numbers(A, B & C) and outputs two one-bit binary numbers, a sum(S) and a carry (Cout). The full adder is usually a componentin cascade of adders, which add 4, 8, 16 etc. binary numbers.Implementation of full adder circuit using GDI techniquewhich is a basic building block of arithmetic and logic unithas been shown in Fig. 5.

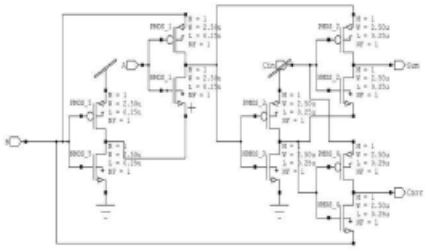

Fig. 5. GDI based 1-bit full adder cell

IV.DESIGN OF ARITHMETIC AND LOGIC UNIT(ALU):

An arithmetic logic unit (ALU) is a fundamental buildingblock of the Central Processing Unit (CPU) of a computer,and even the simplest microprocessors contain one. It isresponsible for performing arithmetic and logic operationssuch as addition, subtraction, increment, decrement, logicalAND, logical OR, logical XOR and logical XNOR ALU consists of eight 4x1 multiplexers, four 2x1multiplexers and four full adders.

The 4-bit ALU is designedin 250nm, n-well CMOS technology. When logic '1'andlogic '0' are applied as an input INCREMENT andDECREMENT operations takes place respectively.AnINCREMENT operation is analyzed as adding '1' to theaddend and DECREMENT is seen as a subtraction operation[6]. Two's complement method is used for SUBTRACTIONin which complement of B is used. The outputs obtainedfrom the full adder are SUM, EXOR, EXNOR, AND & OR.Fig. 6 shows the block diagram of 4-bit ALU where firststage to fourth stage is cascaded with the CARRY bit.Symbolic representation of 4-bit ALU has been visualized infig. 7.

The multiplexer stage selects the appropriate inputs basedon the condition of the select signals, and gives it to the fulladder which then computes the results. The multiplexer atthe output stage selects the appropriate output and route it tooutput port. Table II shows the truth table for the operationsperformed by the ALU based on the status of the selectsignal. The operation being performed and the inputs andoutputs being selected are determined by set of three selectsignals incorporated in the design. Fig 8.shows multiplexerlogic at input port and Fig 9.shows multiplexer logic atoutput port.The multiplexer stage selects the appropriate inputs basedon the condition of the select signals, and gives it to the fulladder which then computes the results. The multiplexer atthe output stage selects the appropriate output and route it tooutput port. Table 2 shows the truth table for the operationsperformed by the ALU based on the status of the selectsignal.

TABLE II. OPERATIONS OF ALU

Selection Lines			Operations
S2	S1	S0	
0	0	0	AND
0	0	1	EXOR
0	1	0	EXNOR
0	1	1	OR
1	0	0	ADDITION
1	0	1	SUBSTRACTION
1	1	0	INCREMENT
1	1	1	DECREMENT

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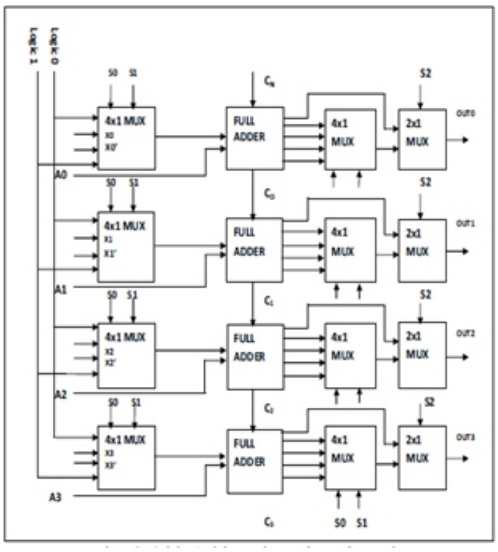

Fig. 6. 4-bit Arithmetic and Logic Unit

The schematic of ALU is designed using schematiceditor of Tanner EDA. It shows connectivity between thecomponents and describes aspect ratios of the transistor thatcan be modified along with the design. Figure 10 representsthe complete schematic view of ALU. The 4-bit ALUconsists of two 4-bit inputs, three selecting lines, and onecarry input, one carry output and four output bits.

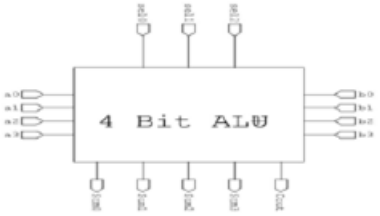

Fig 7. Symbol of 4-bit ALU

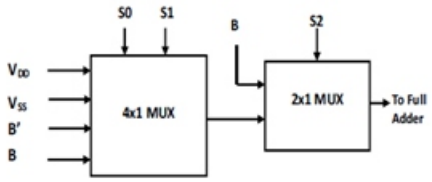

Fig .8. Block diagram of multiplexer logic at the input stage

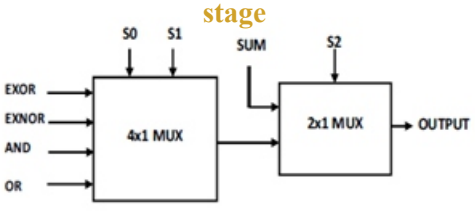

Fig .9. Block diagram of multiplexer logic at the output stage

This paper presents a new approach using concept of Gate Diffusion Input Technique to design an arithmetic andlogic unit. In an ALU, for appropriate selection of input to perform particular operation and for obtaining outputaccordingly multiplexer is the most applicable device. In earlier designs of ALU, the multiplexer unit is either implemented by conventional CMOS logic or by pass transistor logic which proven to have high power consumption. The approach gives better result than previous designs in terms of power consumption, propagation delay as well as area.

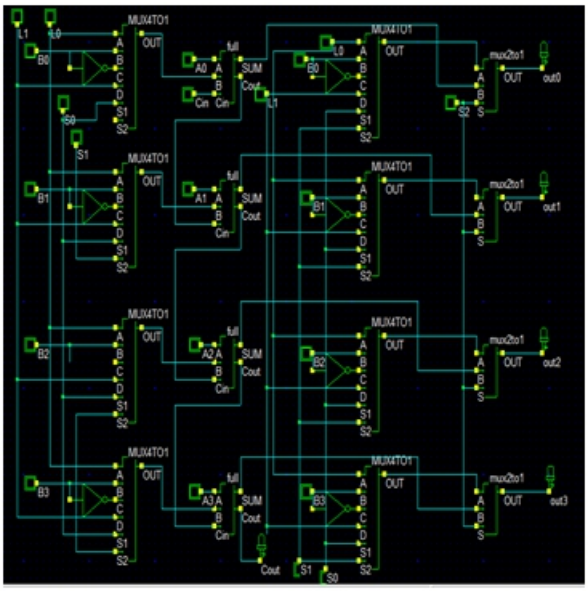

Figure 10. Schematic of 4-bit ALU

V. SIMULATONS RESULTS AND ANALYSIS

This section describes performance of the proposeddesign using Microwind and DSCH 2.0 tool on 120nm technology. Thesimulated output of 2x1 multiplexer, 4x1 multiplexer and fulladder is shown in Figure 11, Figure 12 and Figure 13.Thenumber of transistor required and power consumption for theindividual cells of the ALU is listed in table III and the totalpower consumption and number of transistor of the ALUdesigned in different ways is listed in table IV.

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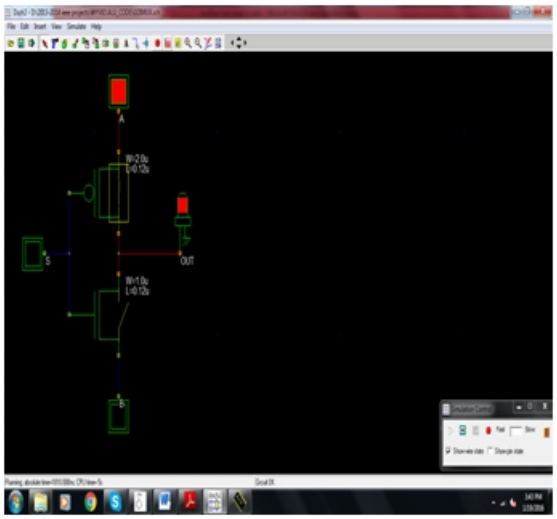

Fig 11. Schematic of 2x1 MUX

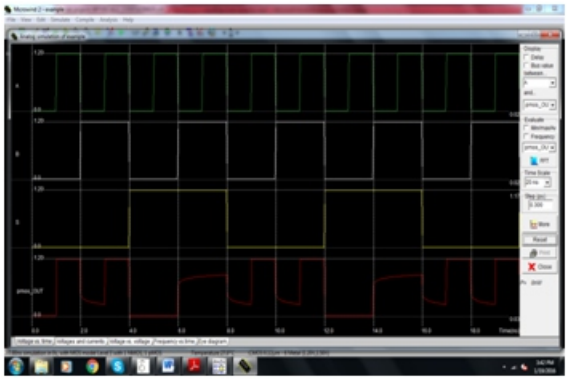

Fig 12. Simulated Output of 2x1 MUX

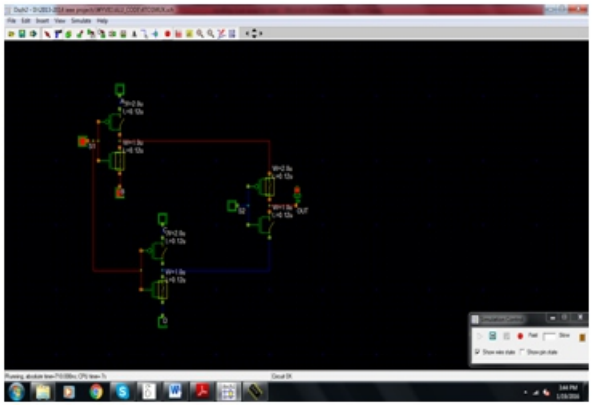

Fig 13.Schematic of 4x1 MUX

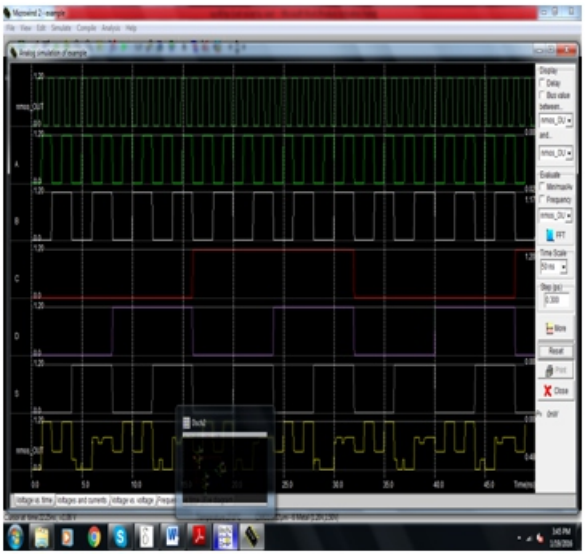

Fig 14. Simulated Output of 4x1 MUX

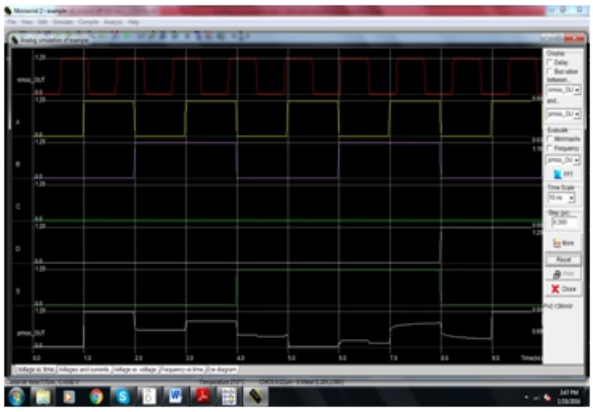

Fig 15. Simulated Output of Full Adder

TABLE III. ANALYSIS RESULT OF DIFFERENT BLOCK OF ALU

S. No.	Design	Cell	Power (μW)	No. of Transistor
1	CMOS	2x1 MUX	4.6073	6
2		4x1MUX	15.123	18
3		Conventional Full adder	16.675	28
4	Pass Transistor Gate	2x1 MUX	1.6079	4
5		4x1MUX	4.225	8
6		Full adder	11.998	24
7	GDI	2x1 MUX	1.394	2
8		4x1MUX	2.987	6
9		Full adder	10.190	10

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TABLE IV. POWER CONSUMPTION OF 4-BIT ALU

S.No.	Design	No. of Transistors	Power(μW)
1	ALU with CMOS Gate	592	4204.5
2	ALU with transmission Gate and 10 Transistor full adder	416	1197.5
3	Proposed ALU with GDI based Full adder	232	1030.5

VI. CONCLUSION:

Power consumption in CMOS circuit is classified in twocategorize: static power dissipation and dynamic powerdissipation. In today's CMOS circuits static powerdissipation is negligible thus not considered as compared todynamic power dissipation. Dynamic Power dissipation in aCMOS circuit is given by P = CLf VDD2. The power supplyis directly related to dynamic power. The numbers of powersupply to ground connections are reduced in GDIimplementation which reduces the dynamic powerconsumption. This work presents a 4-bit ALU designed in250nm technology for low power and minimum area withGDI technique. Various topologies of multiplexer and fulladder implementation is studied and compared. The 2x1multiplexer, 4x1 multiplexer, 1-bit full adder with 10-transistors designed using GDI technique is chosen forlowering power consumption and minimum possible area.Power dissipation, propagation delay and the number oftransistors of ALU were compared using CMOS, nMOSPTL and GDI techniques. GDI technique proved to have bestresult in terms of performance characteristics among all thedesign techniques.

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