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Delay minimization for Carry Select Adder Using Brentkung Adder

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Abstract:

In this brief, the logic operations involved in conventional carry select adder (CSLA) and binary to excess-1 converter (BEC)-based CSLA with bent kung adder are analyzed to study the data dependence and to identify redundant logic operations. We have eliminated all the redundant logic operations present in the conventional CSLA and proposed a new logic formulation for CSLA.In the proposed scheme, we are implemented the brent kung adder in place of ripple carry adder.An efficient CSLA design is obtained using optimized logic units. The proposed CSLA design involves significantly less delay than the recently proposed BEC-based CSLA. Due to the small carry-output delay, the proposed CSLA design is a good candidate for square-root (SQRT) CSLA. The application-specified integrated circuit (ASIC) synthesis result shows that the BEC-based SQRT-CSLA design involve the less delay than the previous design. This work estimates the performance of the proposed designs in terms of delay, area are implemented in Xilinx ISE based on synthesis report and modelsim 6.5e for simulation results.

1. Introduction:

Area and power reduction in data path logic systems are the main area of research in VLSI system design. High-speed addition and multiplication has always been a fundamental requirement of high-performance processors and systems. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the previous bit position has been summed and a carry propagated into the next position. The major speed limitation in any adder is in the production of carries and many authors have considered the addition problem.The CSLA is used in many computational systems to moderate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input and then the final sum and carry are selected by the multiplexers (mux). To overcome above problem, the basic idea of the proposed work is by using n-bit binary to excess-1 code converters (BEC) with brent kung adder to improve the speed of addition. This logic can be implemented with any type of adder to further improve the speed. Using Binary to Excess-1 Converter (BEC) instead of RCA in the regular CSLA to achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the Full Adder (FA) structure. In electronics, a **carry-select adder** is a particular way to implement an adder, which is a logic element that computes the $(n+1)$-bit sum of two n-bit numbers. The carry-select adder is simple but rather fast, having a gate level depth of $O(\sqrt{n})$. The carry-select adder generally consists of two ripple carry adders and a multiplexer. Adding two n-bit numbers with a carry-select adder is done with two adders (therefore two ripple carry adders) in order to perform the calculation twice, one time with the assumption of the carry being zero and the other assuming one. After the two results are calculated, the correct sum, as well as the correct carry, is then selected with the multiplexer once the correct carry is known. The number of bits in each carry select block can be uniform, or variable. In the uniform case, the optimal delay occurs for a block size of $\lfloor\sqrt{n}\rfloor$. When variable, the block size should have a delay, from addition inputs A and B to the carry out, equal to that

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of the multiplexer chain leading into it, so that the carry out is calculated just in time. The $O(\sqrt{n})$ delay is derived from uniform sizing, where the ideal number of full-adder elements per block is equal to the square root of the number of bits being added, since that will yield an equal number of MUX delays.

Basic building block

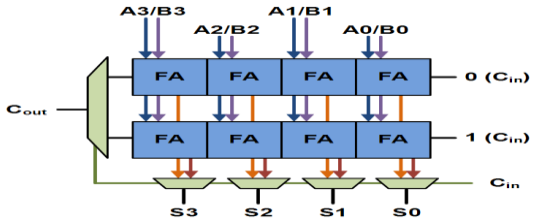

Figure 1: Basic carry Select adder.

Above is the basic building block of a carry-select adder, where the block size is 4. Two 4-bit ripple carry adders are multiplexed together, where the resulting carry and sum bits are selected by the carry-in. Since one ripple carry adder assumes a carry-in of 0, and the other assumes a carry-in of 1, selecting which adder had the correct assumption via the actual carry-in yields the desired result.

Uniform-sized adder:

A 16-bit carry-select adder with a uniform block size of 4 can be created with three of these blocks and a 4-bit ripple carry adder. Since carry-in is known at the beginning of computation, a carry select block is not needed for the first four bits. The delay of this adder will be four full adder delays, plus three MUX delays.

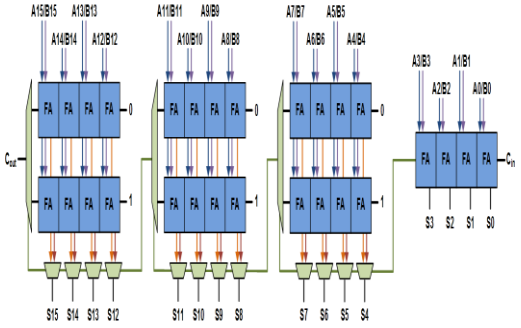

Figure 2: Regular Fixed Size CSLA

Variable-sized adder:

A 16-bit carry-select adder with variable size can be similarly created. Here we show an adder with block sizes of 2-2-3-4-5. This break-up is ideal when the full-adder delay is equal to the MUX delay, which is unlikely. The total delay is two full adder delays, and four mux delays.

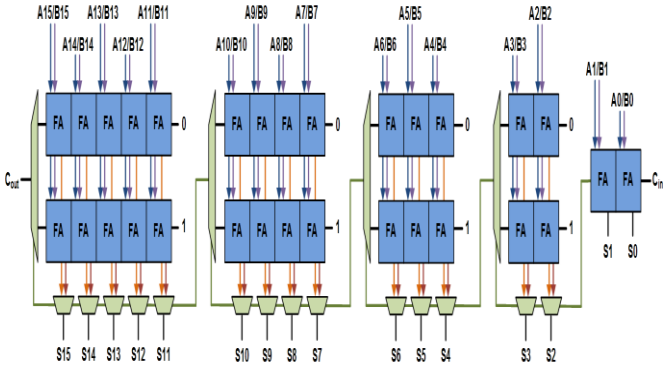

Figure 3: Variable Sized CSLA.

The basic idea of this work is to use Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower area and power consumption [2]–[4]. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure. The details of the BEC logic are discussed in Section III.This brief is structured as follows. Section II deals with the delay and area evaluation methodology of the basic adder blocks. Section III presents the detailed structure and the function of the BEC logic. The SQRT CSLA has been chosen for comparison with the proposed design as it has a more balanced delay, and requires lower power and area [5], [6]. The delay and area evaluation methodology of the regular and modified SQRT CSLA are presented in Sections IV and V, respectively. The ASIC implementation details and results are analyzed in Section VI. Finally, the work is concluded in Section VII.

II. Basic Function And Structure Of BEC Logic:

The delay and area evaluation methodology considers all gates to be made up of AND, OR, and Inverter, each having delay equal to 1 unit and area equal to 1 unit. We then add up the number of gates in the

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longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates required for each logic block. Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder (HA), and FA are evaluated .The basic work is to use Binary to Excess-1 Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower area and power consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit Full Adder (FA) structure As stated above the main idea of this work is to use BEC instead of the RCA with Cin=1 in order to reduce the area and power consumption of the regular CSLA. To replace the n-bit RCA, an n+1-bit BEC is required. A structure and the function table of a 4-bit BEC are shown in Figure.2.

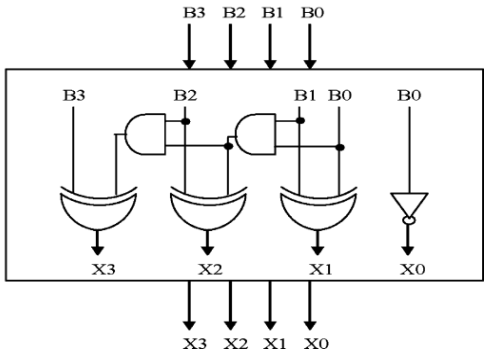

Figure 4: 4 Bit BEC.

The Boolean expressions of the 4-bit BEC is listed as (note the functional symbols ~ NOT, & AND, ^XOR)

X0 = ~B0

X1 = B0^B1

X2 = B2^ (B0 & B1)

X3 = B3^ (B0 & B1 & B2)

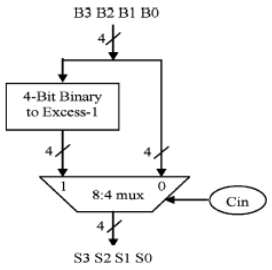

Figure 5: 4-Bit BEC with 8:4 mux.

III. Basic Structure of Regular 16-Bit CSLA:

A 16-bit carry select has two types of block size namely uniform block size and variable block size. A 16-bit carry select adder with a uniform block size has the delay of four full adder delays and three MUX delays. While a 16-bit carry select adder with variable block size has the delay of two full adder delays, and four mux delays. Here we use 16-bit carry select adder with uniform block size. Ripple-carry adders are the simplest and most compact full adders, but their performance is limited by a carry that must ripple from the least-significant to the most-significant bit. A carry-select adder achieves speeds 40% to 90% faster by performing additions in parallel and reducing the maximum carry path.

A carry-select adder is divided into sectors, each of which, except for the least significant performs two additions in parallel, one assuming a carry-in of zero, the other a carry-in of one within the sector, there are two 4-bit ripple- carry adders receiving the same data inputs but different Cin. The upper adder has a carry-in of zero, the lower adder a carry-in of one. The actual Cin from the preceding sector selects one of the two adders. If the carry-in is zero, the sum and carry-out of the upper adder are selected. If the carry-in is one, the sum and carry-out of the lower adder are selected. Logically, the result is not different if a single ripple-carry adder were used.First the coding for full adder and different multiplexer of 10:5was done. Then 4-bit ripple carry adder was done by calling the full adder. The regular 16-bit CSLA was created by calling the ripple carry adders and all multiplexers based on circuit.

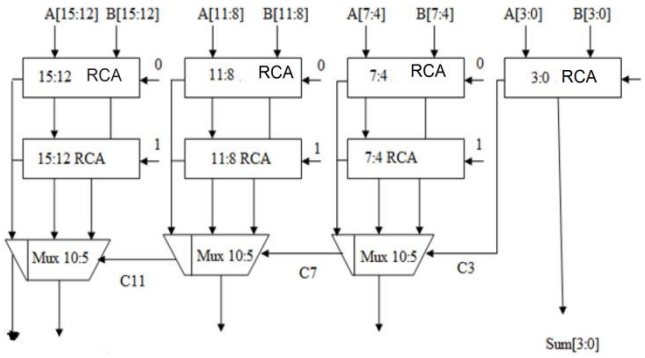

Figure 6: Regular 16-bit SQRT CSLA

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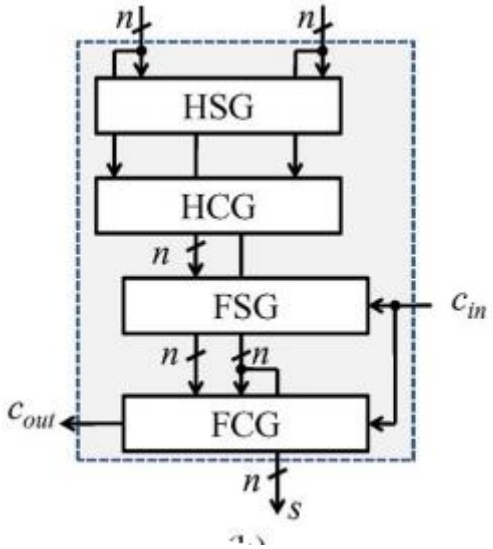
IV.Existing adder design:

The proposed csla is based on logic formulation given in the figure.it consists of one hsg unit and one fsg unitone cg unit and one cs unit.the logic circuit of cg0 and cg1 are optimized to take advantage of the fixed input carry bits.



V.Basic Structure of Modified 16-Bit CSLA:

It is similar to regular 16-bit SQRT CSLA. Change is that in basic blocks having two ripple-carry adders, one ripple carry adder fed with a constant 1 carry-in is replaced by BEC and other one is fed with brent kung adder.

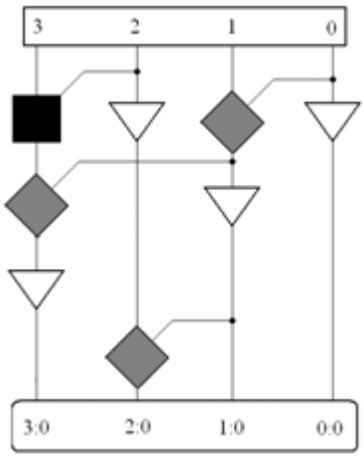


Figure 7. 4-bit brent kung adder

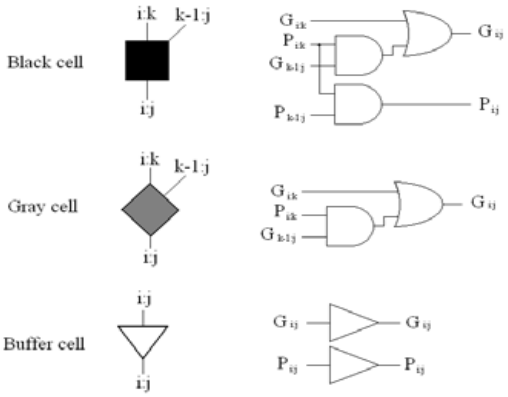


Figure 8. Complex logic cells inside the brent kung adder

The brent kung adder is placed at first stage as shown in fig 9.we are placing a 4-bit brent kung adder in place of 4-bit RCA to get high speed calculations. The brent kung adder we are used in our proposed design is as shown in fig 7.

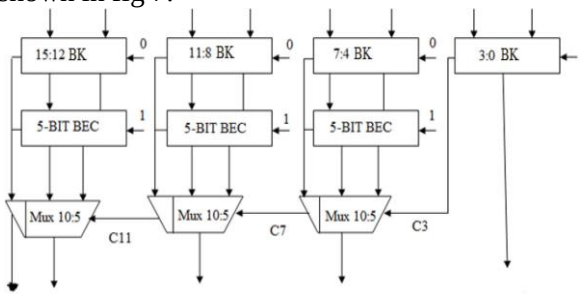


Figure 9. proposed 16-bit SQRT CSLA

VI. IMPLEMENTATION RESULTS:

The design proposed in this paper has been developed using Verilog-HDL and synthesized in Xilinx ISE 9.1i. For each word size of the adder, the same value changed dump (VCD) file is generated for all possible input conditions and imported the same to Xilinx ISE 9.1i Power Analysis to perform the power simulations. The similar design flow is followed for both the regular and modified SQRT CSLA.

Figure. 10. Proposed 16-bit CSLA RTL schematic

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The delay product of the proposed 16-bit is less than that of the regular SQRT CSLA the delay for our proposed design is 15.205ns and the delay for regular design is 17.413ns . However, the power-delay product of the proposed 16-bit SQRT CSLA. input (a sequence of numbers, resulting from sampling and quantizing an analog signal) and produces a digital output.

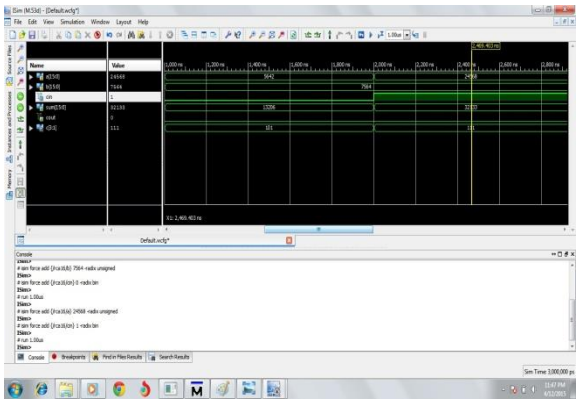

Figure. 11. Proposed 16-bit CSLA simulation results

The simulation and synthesis Results of proposed Modified Carry Select adder shown figure 10 and 11.comapre to regular CSLA modified CSLA architecture is take less amount of delay.

VII. CONCLUSION:

A simple approach is proposed in this paper to reduce the delay and power of SQRT CSLA architecture. This work offers the advantage in the reduction of delay and also the total power. The power-delay product product of the proposed design show a decrease for 16-bit size which indicates the success of the method and proposed design mainly focuses on the delay it has slightly big area than the regular CSLA. The modified CSLA architecture is therefore, low delay, low power, simple and efficient for VLSI hardware implementation.

As the functional verification decides the quality of the silicon, we spend 60% of the design cycle time only for the verification/simulation.we use the latest verification methodologies and technologies and accelerate the verification process. This project helps one to understand the complete functional verification process of complex ASICs an SoC's and it gives opportunity to try the latest verification methodologies, programming concepts like Object Oriented Programming of Hardware Verification Languages and sophisticated EDA tools, for the high quality verification.

Future Work:

This project used System Verilog i.e., the technology used is direct test cases, randomized test cases ,OVM for verification even though the coverage is 100% there may be some errors which cannot be shown so in Oder to overcome this the new technology of System Verilog i.e., OVM and UVM. In the coming future the Router can be done by using OVM and UVM.

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