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EfficientMulti Port Network Router; Withperformance Analysis

K.Venkat Reddy
M.Tech,
Department of ECE,
Brilliant Institute of Engineering and Technology.

M.Ajith Rao
Assistant Professor,
Department of ECE,
Brilliant Institute of Engineering and Technology.

ABSTRACT:

The users which are want to set-up a LAN (Local Area Network) or WLAN (wireless LAN) and connect all computers to the Internet without having to pay a full broadband subscription service to their ISP for each computer on the network.The router consists of one input port and three output ports for the purpose of packet enter at the source terminal and the packet is driven out at the destination terminal respectively. This type of packet travels through a router it is called as NETWORK ROUTER. In the network router specific Packet contains 3 parts. Those are header part, data part and frame check sequence part. Packet width is 8 bits and the length of the packet can be between 1 byte to 63bytes. In the packet the Destination address (DA) of the packet is of 8 bits. The switch drives the packet to the related ports based on this destination address of the packets. In this process every output port has 8-bit unique port address. If the destination address of the packet matches the port address, then switch drives the packet to the output port, Length of the data is of 8 bits. This network router supports three parallel connections at the same time. The router uses store and forward type of flow control and FSM Controller deterministic routing which improves the performance of router.

ROUTER PORT ANALYSIS:

In the functional verification it decides the silicon quality and more than 50% of the design cycle time is for the verification /simulation. Due to the functional bugs as more as possible ASIC fault responses are occurring in the design cycle.For the avoid the delay and meet the TTM, we use the latestVerification methodologies and technologies and accelerate the verification process. This project helps to understand the complete functional verification process of complex ASICs an SOC's and it gives opportunity to learn the trending verification methodologies, programming concepts like Object Oriented Programming of Hardware Verification Languages and sophisticated EDA tools, for the high quality verification

Basic necessity of router:

Broadband or ICS routers will manufacture as quite as different with the value of brand in the quality. Those hardware devices are generally a small box shape with the front and back ports for the purpose of switchable operations in the each computer with the plugging of port in your broadband modem.Depending on the modem and Internet connection formats you have available, and also the user choose a router with phone or fax operating ports. Router operates on the functions of direct trafficking. A packet of data is forwarded in the internetwork operations till it grasps the node of destination.The router applications are so useful in the home to setup a LAN or WLAN for the connection of all computers with a single router network.

Those are the internet services to pay the full broadband subscription to their Internet Service Protocol. In many cases, an ISP will give the permission to use a router and connect multiple computers to a unique Internet connection and pay a normal fee for each additional computer sharing the connection.In the business or organizationthe need of connections of multiple computers to the Internet, but also want to the multiple links between the private networks and it will not be created equal when ever their job will differ slightly between different networks. A router doesn't define its shape, color, size or manufacturer, but its operation of routing data packets between computers.

A modem which routes data between your PC and your ISP can be considered a router. In its most basic form, a router could simply be one of two computers running the Windows 98 (or higher) operating system connected together using ICS (Internet Connection Sharing). In this scenario, the computer that is connected to the Internet is acting as the router for the second computer to obtain its Internet connection. Going a step up from ICS, we have a specific type of hardware routers that are used to perform the same basic task as ICS with more features and functions.

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Ethernet is a computer networking technology which enhances for local area networks (LANs) and metropolitan area networks (MANs). It has been refined to support complex and high mode of bit rates and longer link distances.In Ethernet broadband router the type of wired network will typically have a built-in Ethernet switch to allow for the services of expansion and also those support NAT (network address translation), which gives permission to all of the computers by the access of single IP address on the Internet. Internet connection sharing routers will also provide users with much needed features such as an SPI firewall or serve as a DHCP Server.

DESIGN OF ROUTER:

In the manner of target contest and accomplishment adopted a set of principles about the implementation of particular size of router within the concept of minimal design window for the efficient performance.With Provisional of specifications for theRouteris totally depends on the type of packet based protocol.In the incoming packet the router wires in between the port of input to output port on the basis of address which is consists in the packet.The router implements in the network mode which has a one port of input where the packet enters and three output ports where the packet is driven out. In the format of packet there are three parts. Those are Header, data and frame check sequence. The width of packet is in terms of 8 bits and the length of packet defined in between 1 to 63 bytes. The header of packet consist of three fields DA and lengthDA is nothing but Destination address of the particular packet and each packet consists of 8bits address data.

The packet is driven by the switch with respect to the ports based on the destiny address of particular packets. The size of output port has 8-bit and this address of port is unique. The port address matches to the destination address in the automatic mode the processing of switch wires thepacket to the output port, length of the data is of 8 bits and from 0 to 63. Data must be in the form of bytes and it accepts anything. Actually the binary logic parameter bytes are measured for length in the design of router. The security issues of checking the packet by the frame check sequence of the packet and calculate over the header and data. The router carried out the communication on network on chip for the design of effective NOC and in this case the router operated as well as effective. In this type of NOC's which are used in the operations of router used here is packet switching.

The router works on the store and fetch mode of operations with the controller of FSM and it improves the performance of router by the deterministic routing. The router operates on the size of three ports with the efficient connections.In the transfer of data packets the store, fetch and flow mechanism is the best one because of no requirement for channel reservation and thus does not avoid the effect of idle physical channels. In the operation of ROUTER the role of buffering is to utilize the avoidance of both sides of directions without the effect of congestion. In the project the device implementation levels increases the complexity in the number of ports with the utilization of efficient First In First Out's and router Finite State Machines and synchronous registers. With those sub modules the ROUTER top module implemented with efficient performance and less delay values. With the efficient LUT'S for the output port synchronization we utilize the data packets through the networks depends on the bit size of data chosen by user.

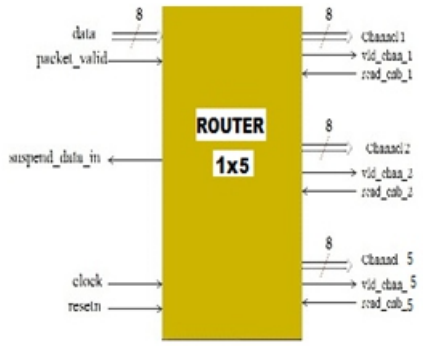

Fig. 1- Block Diagram of five Port Router

FEATURES:

» Full duplex synchronous serial data
» Variable length of transfer word up to 64 bytes.
» HEADER is the first data transfer.
» Rx and Tx on both rising or falling edge of serial clock independently.
» Fully static synchronous design with one clock domain
» Technology independent
» Fully synthesizable
» Multi receivers select lines
» ROUTER is a Synchronous

The clock signal is provided by the master to provide synchronization. The clock signal controls when data can change and when it is valid for reading.Since ROUTER

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is synchronous, it has a clock pulse along with the data. RS-232 and other asynchronous protocols do not use a clock pulse, but the data must be timed very accurately. Since ROUTER has a clock signal, the clock can vary without disrupting the data. The data rate will simply change along with the changes in the clock rate.As compared with its counterpart I2C, ROUTER is more suited for data stream applications. Communication between IP's,

FUNCTIONAL ANALYSIS:

In the operation of basic router we design the blocks with 8-bit register, router controller and output block, the basic router design will enhance with the port allocations. For the support of sequence operating design the FIFO operations are performed in that port router.With the combination of FIFO'S that store packet of data and at the time of requirement the data will read from the FIFO's. the design of router consists of three port router consists of at the size of 8 bit and 8 bit data port and it is using to drive the data into the router module by using the global clock and reset signals and the err signal, suspended data signals are the output's of the router. Those err and suspended data in signals given by the FSM controller.The ROUTER operations consist of a single master device and with one or more slave devices.When the RE pin fixed to the logic low at the single device usage the slave permits it. Some slaves operate on high to low transitions of the slave select to begins an action like the mobile operations, which done the transition o the basis of conversion. With the independent RE signal we operate the single master to multiple slave devices with in each.

SIMULATION RESULT ANALYSIS

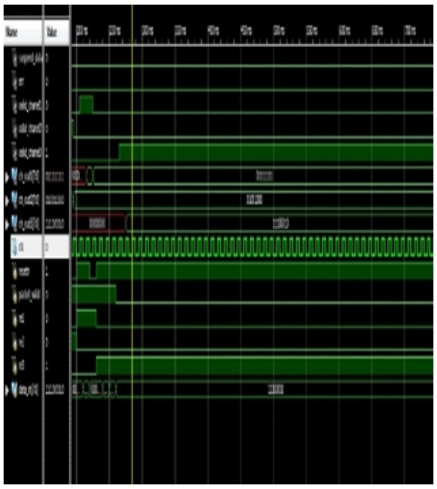

Fig 2:Simulation result of Router

IV APPLICATIONS:

When multiple ports of routers are used in the networks which are connected internally and these routers exchangeinformation by using a dynamic routing protocol about destination addresses in the router operations. Router provides connectivity within enterprises, between enterprises and the internet. Largerouters such as Cisco CRS-1or Juniper T1600 interconnects various ISP's.In the interconnected networks in between two systems they preferred the different routes with the description of table listing in each router.The routers interface with the various physical types of connections in the network applications. Those network connections like as copper cables, fiber optic technologies, wireless transmissions in the real time aspects. It also includes firmware for networking protocol standards in a disparate way.Eachnetwork interface to enable data packets we utilize special softwares and those are directed from one protocol transmissionsystem to othersystems. In the subnets the routers are connected with the two or more logical groups of computing devices by a different sub network address. In the router we do not map the physical interfaces directly and the subnet addresses are also recorded in the routers.

EDA TOOLS AND METHODOLOGIES:
HDL: VERILOG HDL.
Verification Methodology:

Constrained Random Coverage Driven Assertion Based verification.

EDA Tools:

Xilinx 14.5 ISE SIMULATOR AND SYNTHESIZER. By the utilization of XILINX ISE tool we implement the brief architecture through mixed level models through VERILOG HDLlanguage and also we shows the synthesis results on the XILINX ISE with the combination of simulation and synthesis results.

RESULTS
Device Utilization Summary:
Selected Device:
SPARTAN 3E - 3s500efg320-5

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Logic Utilization	Used	Available
Number of Slices	714	14752
Number of Slice Flip Flops	792	29504
Number of 4 input LUTs	632	29504
Number of bonded IOBs	63	250
Number of GCLKs	1	24

TOTAL DELAY FOR FIVE PORT ROUTER 6.937ns(4.907ns logic, 2.030ns route)(70.7% logic, 29.3% route)

CONCLUSION:

In the router functional analysis of ports we define the topologies of multiple ports of the router with the enhanced methodologies of verification. In the project we verify the 3 port router operations and extended to the size offor five ports.This ROUTER improves the performances by the reducing of delay values with the increment of ports and we define the topology in the manner of efficient functional verification.The router ports are verified by the data read ports as output the device to allow the access of multiple computers usage. The router technology will enhance the real time applications MODEM and ETHERNET protocols in the usage of broadband networks and internet wireless networks.

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