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Implementation of Dual Unified Power Quality Conditioner for Power Quality Improvement by Fuzzy Logic Controller

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Abstract:

This paper proposes a novel controlled technique for Dual three phase topology of unified power quality conditioner (d-UPQC) adopted to compensate current and voltage quality problems of Non-linear loads. This paper tends look at the solving the problems by using custom power devices by Dual Unified Power Quality Conditioner (d-UPQC) using Fuzzy Logic Controller. A Fuzzy Logic controller is based on fuzzy sets and fuzzy rules with their membership functions of inputs and outputs. A Control technique of two active filters is to control the sinusoidal references. In dUPQC, series Active Filter (SAF) works as a current source and Parallel Active Filter (PAF) works as a voltage source different from a conventional UPQC and due to these there is a high and low impedances occurs which is indirectly compensates the harmonics and disturbance of the grid voltage and load current and also impedance path is low harmonic at load current.

The i-UPQC is composed of two active filters, a series active filter and a shunt active filter (parallel active filter), used to eliminate harmonics and unbalances. Different from a conventional UPQC, the i-UPQC has the series filter controlled as a sinusoidal current source and the shunt filter controlled as a sinusoidal voltage source. Therefore, the pulse width modulation (PWM) controls of the i-UPQC deal with a well-known frequency spectrum, since it is controlled using voltage and current sinusoidal references, different from the conventional UPQC that is controlled using non sinusoidal references. The dynamic analysis of proposed scheme is evaluated by using Matlab/Simulink platform & results are presented.

IndexTerms:

Active filters, control design, Fuzzy Controller, power line conditioning, unified power quality conditioner (UPQC).

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I. INTRODUCTION:

With the invention of power electronic deviceslike thyristors, GTO's (Gate Turn Off Thyristors) andmany devices, control of electric power is simple andeasy. But the power electronic devices have their nonlinearity characteristics, cause harmonic and drawexcessive currents. The harmonics, excessive currentscause for low system efficiency. In addition to this powersystem is subjected to various disturbances like voltagesags and swells etc. By using Unified power Quality Conditioner(UPQC) [1]-[10] it can supply regulated voltage for theloads, balanced and low harmonic distortion. The UPQC consists of series and shunt active power filters. Shuntactive filters also provides harmonic isolation between supply system and load. The series active filter regulatesthe incoming voltage quality.In the conventional UPQC both series activefilters and shunt active filters are controlled by using nonsinusoidal references. PAF usually acts as non sinusoidal current source used to reduce harmonic currents of theload. SAF acts non sinusoidal voltage source used tomitigate voltage disturbances.

Non sinusoidal referencesmean combination of both fundamental and harmonicreferences. The extraction of harmonic contents requirescomplex calculations. Therefore there are so manymethods to extract harmonics, but it is more complexity of reference generation [10]. In UPQC they are two types of filters SAF and PAF, PAFis a current source and SAF is a voltage source both of themare a nonsinusoidal reference and also compensate theharmonic in grid voltage and load current. It is a complexmethod to solve such problems we are using active filters tocontrol the harmonics and to eliminate harmonics usingfuzzy controller. Its conditioner consists of two single-phasecurrent source inverters where the SAF is controlled by acurrent loop and the PAF is controlled by a voltage loop bothof them are interconnected to fuzzy controller and gridcurrent and load voltage are sinusoidal, and therefore, theirreferences are also sinusoidal.



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This concept is called "dualtopology of unified power quality conditioner" (iUPQC),and the control schemes use the p-q theory, for a real time of positive sequence. The aim of this paper is to propose anovel controlled technique for Dual unified Power QualityConditioner for power quality improvement to eliminate the harmonics from source to load. In ABC reference frame, theproposed control scheme is developed for the classical control theory is without the need for coordinatetransformers and digital control implementation. Thereferences to both SAF and PAF with fuzzy logic controlleris a pure sinusoidal, dispensing the harmonic extraction from the grid current and load voltage. A new methodology for the evaluation and control of losses taking place in a UPQC has been proposed.A new control strategy aimed to compensate reactive power, negative sequence current, current harmonics and also to regulate any voltage imbalance has been proposed. A neural network controlled UPQC without injection transformer has been designed and reported. Another control structure using linear quadratic regulator (LQR) along with hysteresis control is successfully tested for various operating conditions. UPQC implemented uses a control circuit withoutreference calculation. Complicated control structures of UPQChave been replaced by a simple control technique. Voltage interruption can also beeliminated by the use of a unified power qualityconditioner with distributed generation. Recent research shows that AI based controllers are very promising in the field power system and power electronics. The conventional PI controller is replaced by a fuzzy logic controller [FLC] for the determination of the reference current in a shunt active power filter. The successful application of FLC to generate the switching signals required in an active filter realized using current controlled PWM inverter. T-S fuzzy model is used to predict future harmonic compensating current in an APF system.

II.DUAL UPQC:

The conventional UPQC structure is composed of a SAF and a PAF, as shown in Fig.1. In this configuration, the SAF works as a voltage source in order to compensate the grid distortion, unbalances, and disturbances like sags, swells, and flicker. Therefore, the voltage compensated by the SAF is composed of a fundamental content and the harmonics. The PAF works as a current source and it is responsible for compensating the unbalances, displacement, and harmonics of the load current, ensuring a sinusoidal grid current.



The series filter connection to the utility grid is made through a transformer, while the shunt filter is usually connected directly to the load, mainly in low-voltage grid applications. The conventional UPQC has the following drawbacks: complex harmonic extraction of the grid voltage and the load involving complex calculations, voltage and current references with harmonic contents requiring a high bandwidth control, and the leakage inductance of the series connection transformer affecting the voltage compensation generated by the series filter. In order to minimize these drawbacks, the iUPQC is investigated in this project, and its scheme is shown in Fig. 2. The scheme of the iUPQC is very similar to the conventional UPQC, using an association of the SAF and PAF, diverging only from the way the series and shunt filters are controlled. In the iUPQC, the SAF works as a current source, which imposes a sinusoidal input current synchronized with the grid voltage. The PAF works as a voltage source imposing sinusoidal load voltage synchronized with the grid voltage. In this way, the iUPQC control uses sinusoidal references for both active filters. This is a major point to observe related to the classic topology since the only request of sinusoidal reference generation is that it must be synchronized with the grid voltage. The SAF acts as high impedance for the current harmonics and indirectly compensates the harmonics, unbalances, and disturbances of the grid voltage since the connection transformer voltages are equal to the difference between the grid voltage and the load voltage. In the same way, the PAF indirectly compensates the unbalances, displacement, and harmonics of the grid current, providing a low-impedance path for the harmonic load current.



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III. OUTPUT PASSIVE FILTER DESIGN:

The iUPQC circuit can be analyzed by a single-phase wiring diagram, as shown in Fig. 4. The utility grid impedance is represented by

 $Z_{\rm s}=j\,\omega\!L_{\rm s}+R_{\rm s}\,, \ \, {\rm while} \quad {\rm the} \quad {\rm coupling} \quad {\rm transformer}$

leakage impedance is represented by $Z_s = j \omega L_{lg} + R_{lg}$ and the voltage sources and represents the equivalent structures of the series and shunt filters, which generate a waveform composed of the fundamental component and harmonics that originated from the commutation of the switches. These high frequencies must be filtered by the output passive filters of the iUPQC, ensuring sinusoidal grid currents and load voltages. Fig.5 shows the equivalent circuit used for the SAF output impedance analysis, and Fig.6 shows the equivalent circuit used for the PAF output impedance analysis. In order to simplify the analysis of the PAF, the voltage source and the inductance, which are series connected, were considered as a current source. Observing the equivalent circuits, we can claim that the PAF output impedance affects the frequency response of the SAF, while the SAF output impedance does not affect the frequency response of the PAF. Therefore, the output passive filter design of the iUPQC should be started with the PAF design followed by the SAF design. The high-frequency filter transfer function of the PAF is derived by analyzing the circuit of Fig.6 and is shown in

$$\frac{v_L(s)}{v_{pc}(s)} = \frac{1}{L_{pf}C_{pf}} \cdot \frac{1}{s^2 + s \cdot \frac{1}{C_{pf}R_L} + \frac{1}{L_{pf}C_{pf}}}.$$
(1)

The inductor was defined by the power design, so the capacitor will be defined according to the desired cutoff frequency of the filter. In this design, a 2.9-kHz cutoff frequency was used, resulting in a value of 10Mf for the C_pf filter capacitor. Fig.7 shows the PAF frequency response for the nominal load and no load. The high-frequency filter transfer function of the SAF is derived by analyzing the circuit of Fig.5 and is shown in

$$\frac{i_s(s)}{v_{sc}(s)} = \frac{n}{\{sL_{sf} + n^2[sL_{lg} + R_{lg} + \alpha + \beta] \cdot \gamma\}}$$

$$\alpha = \frac{sL_{pf}R_L}{s^2L_{pf}C_{pf}R_L + sL_{sf} + R_L}$$
(2)

(3)

Where

$$\beta = \frac{sL_{rd} + R_{rd}}{s^2 L_s C_{sf} + sC_{sf} R_s + 1}$$

$$\gamma = s^2 C_{sf} L_s + sC_{sf} R_{lg} + 1.$$
(4)

(5)

As the inductor was defined by the power design, the capacitor will be defined according to the desired cutoff frequency of the filter. In this design, a 45-Hz cutoff frequency was used, resulting in a value of 1μ Ffor the load and noload.



Fig 3.Power circuit of the iUPQC.



Fig.4. Single-phase wiring diagram of the dual UPQC.



Fig.5. Equivalent circuit as viewed by SAF.

It can be noted that the filter response has a low cutoff frequency that can reduce the bandwidth of the SAF, decreasing its effectiveness under operation with harmonic contents on the grid voltage. This characteristic of lowfrequency attenuation is undesirable and intrinsic to the structure due to the leakage impedance of the coupling transformers.



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An important contribution of this project and different from what it was stated in some previous articles, which deal with the same iUPQC control strategy, is that, in spite of the SAF operates with sinusoidal reference, the control of this filter needs to deal with high frequency since the current imposed



Fig.6. Equivalent circuit as viewed by PAF.

By the SAF is obtained through the voltage imposition on this filter output inductor. The voltage imposed on these inductors is complementary to the utility grid voltage harmonics so that it guarantees a sinusoidal current through the filter. Different from the conventional UPQC whose narrow-band frequency control may distort the load voltage, in the iUPQC, the narrowband frequency control may distort the current drained from the utility grid. The usage of high-power coupling transformers, with low leakage inductance, and the design of higher voltage dc link, allowing the imposition of higher current rate of change on the filter output inductor, is solutions to change the characteristics of the filter attenuation in low frequencies.



Fig.7. Control block diagram of the SAF controller.

IV. PROPOSED CONTROL SCHEME:

The proposed iUPQC control structure is an ABC reference frame based control, where the SAF and PAF are controlled in an independent way. In the proposed control scheme, the power calculation and harmonic extraction are not needed since the harmonics, unbalances, disturbances, and displacement should be compensated. The SAF has a current loop in order to ensure a sinusoidal grid current synchronized with the grid voltage. The PAF has a voltage loop in order to ensure a balanced regulated load voltage with low harmonic distortion. These control loops are independent from each other since they act independently in each active filter. The dc link voltage control is made in the SAF, where the voltage loop determines the amplitude reference for the current loop, in the same mode of the power factor converter control schemes. The sinusoidal references for both SAF and PAF controls are generated by a digital signal processor (DSP), which ensure the grid voltage synchronism using a phase locked loop.

A.SAF Control :

Fig. 7 shows the control block diagrams for the SAF. The SAF control scheme consists of three identical grid current loops and two voltage loops. The current loops are responsible for tracking the reference to each grid input phase in order to control the grid currents independently. One voltage loop is responsible for regulating the total dc link voltage, and the other is responsible for avoiding the unbalances between the dc link capacitors. The total dc voltage control loop has a low-frequency response and determines the reference amplitude for the current loops. Thus, when the load increases, overcoming the input grid current, the dc link supplies momentarily the active power consumption, resulting in a decrease of its voltage. This voltage controller acts to increase the grid current reference, aiming to restore the dc link voltage. In the same way, when the load decreases, the voltage controller decreases the grid current reference to regulate the dc link voltage. Considering the three phase input current, sinusoidal and balanced, the voltage loop transfer function is obtained through the method of power balance analysis.



Fig.8. Equivalent circuit of the SAF voltage loop.

The three-phase four wire converter with neutral point can be represented by the circuit shown in Fig. 8, composed of a current source which is in parallel with the dc



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link impedance and whose current source represents the average charge current of the dc link. The resistor R_b is absent in the real circuit (R_b $\rightarrow\infty$); it just represents instantaneous active power consumption of the dc link. The term instantaneous is related to the time of the switching period, since active power consumption of the dc link is null for the utility grid voltage frequency. The average charge current of the dc link is given by

$$\overline{I_{eq}} = \frac{3}{2} \cdot \frac{n \cdot V_{gdpk} \cdot I_{sfpk}}{V_b}.$$
(6)

The SAF peak current is considered the same for the three phases due to balanced current. Through (6), the voltage loop transfer function is obtained and is represented by

$$Gv_{sf}(s) = \frac{V_b(s)}{I_{sf}(s)} = \frac{3}{2} \cdot n \cdot \frac{V_{gdpk}}{V_b} \cdot \frac{1}{\frac{1}{R_b} + sC_b}$$
(7)

Where

 V_{gdpk} Vgdpk Peak of the grid voltage;

V_bVbDc link voltage;

 R_b Rb Load equivalent resistance;

 C_b CbTotal dc link equivalent capacitance;

n transformer ratio.

The open-loop transfer function (OLTFv) is given by

$$OLTFv(s) = Gv_{sf}(s) \cdot \frac{Kv_{sf}}{Ki_{sf}} \cdot Km_{sf}$$
(8)

Where

 Km_{sf} = multiplier gain;

Kvsf = voltage sensor gain;

Kisf = current sensor gain.

The gain is obtained by considering the gain of the multiplier integrated circuit and the peak of the synchronized sinusoidal signal generated by the DSP.



Fig.9. Equivalent circuit of the SAF unbalancedvoltage loop.

The unbalanced-voltage control loop also has a low frequency loop and acts on the dc level of the grid current reference in order to keep the voltage equilibrium in dc link capacitors. When a voltage unbalance occurs, this loop adds a dc level to the references of the grid currents, aiming to equalize both and voltages. The unbalanced-voltage loop transfer function is obtained through the analysis of the simplified circuit shown in Fig. 9. The four-wire converter allows the single-phase analysis, where two current sources represent the current on the inverter switches. In Fig. 10, the current i(t) represents the current through the neutral point, and d(t) represents the duty cycle. Through the mesh analysis and by applying Laplace, the unbalancedvoltage loop transfer function is obtained and

$$Gd_{sf}(s) = \frac{V_{b+}(s) - V_{b-}(s)}{I_{sc}(s)} = \frac{3}{2 \cdot s \cdot C_b}.$$
(9)

The open-loop transfer function ($OLTF_d$) is given by



Fig. 10.Single-phase equivalent circuit of SAF.

The current control scheme consists of three identical current loops, except for the 1200 phase displacements from thereferences of each other. The current loops have a fast responseto track the sinusoidal references, allowing the decoupling analysis in relation to the voltage loop. The current loop transfer function is obtained through the analysis of the single-phase equivalent circuit shown in Fig. 10. The voltage source represents the voltage on the coupling transformer. The dynamic model is obtained through the circuit analysis using average values related to the switching period. Under these conditions, the voltage source represents analysis and by using Laplace, the current loop transfer function is given by

$$Gi_{fs}(s) = \frac{I_{sc}(s)}{D(s)} = \frac{V_b}{sA_1 + n^2 \cdot (R_s + R_{lg})}$$
(11)

Where

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$$A_1 = n^2 \cdot (L_s + L_{lg}) + L_{sf}$$
(12)



Fig.11. Control block diagram of the PAF voltage loop.

and

 L_S Series grid inductance;

R_SSeries grid resistance;

 L_{lg} Leakage inductance of the coupling transformer;

 R_{lg} Series resistance of the coupling transformer.

The open-loop transfer function $(OLTF_I)$ is given by

$$OLTFi(s) = Gi_{sf}(s) \cdot Kpwm_{sf} \cdot Ki_{sf}$$
(13)

Where series filter pulse width modulation (PWM) modulator gain. Gain is equal to the inverse peak value of the triangular carrier. Aiming to track the current reference, a PI+pole controller was designed, which ensures a crossover frequency of 5 kHz and a phase margin of 700. The frequency response of the current loop is shown in Fig. 12, including the open-looptransfer function (OLT+), controller transfer function (OLT+),and compensated loop transfer function (OLT+).

B.PAF Control:

Fig. 12 shows the control block diagram of the shunt active filter controller. The PAF control scheme is formed by three identical load voltage feedback loops, except for the 1200 phase displacements from the references of each other. The voltage loops are responsible for tracking the sinusoidal voltage reference for each load output phase in order to control the load voltages independently.



Fig. 12. Single-phase equivalent circuit of PAF.

The voltage loop transfer function is obtained through the analysis of the single-phase equivalent circuit shown in Fig. 12. The dynamic model is obtained through the circuit analysis using average values related to the switching period. Through small signal analysis and by using Laplace, the voltage loop transfer function is given Where

$$Gv_{pf}(s) = V_L(s)/D(s).$$
(14)

The open-loop transfer function (OLTF) is given by

$$OLTFv(s) = Gv_{pf}(s) \cdot Kpwm_{pf} \cdot Kv_{pf}$$
(15)

WhereKpwshunt filter PWM modulator gain. Aiming to track the voltage reference, a proportional integral derivative (PID)+ additional pole controller was designed, which ensures a crossover frequency of 4 kHz and a phase margin of 350.



Fig.13.Powerflow of iUPQC. (a) Vs<VL, (b) Vs>VLv_L. Controller transfer function (HvPF), and compensated loop transfer function (OLTFvpf+Hvpf).

V.FUZZY LOGIC CONTROLLER:

Figure.14.shows the internal structure of the control circuit. The control scheme consists of Fuzzy controller, limiter, and three phase sine wave generator for reference current generation and generation of switching signals. The peak value of reference currents is estimated by regulating the DC link voltage.



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The actual capacitor voltage is compared with a set reference value. The error signal is then processed through a Fuzzy controller, which contributes to zero steady error in tracking the reference current signal. A fuzzy controller converts a linguistic control strategy into an automatic control strategy, and fuzzy rules are constructed by expert experience or knowledge database. Firstly, input voltage Vdcand the input reference voltage Vdc-ref have been placed of the angular velocity to be the input variables of the fuzzy logic controller. Then the output variable of the fuzzy logic controller is presented by the control Current Imax. To convert these numerical variables into linguistic variables, the following seven fuzzy levels or sets are chosen as: NB (negative big), NM (negative medium), NS (negative small), ZE (zero), PS (positive small), PM (positive medium), and PB (positive big) as shown in Figure .15.

The fuzzy controller is characterized as follows:

- 1) Seven fuzzy sets for each input and output;
- 2) Fuzzification using continuous universe of dis-course;
- 3) Implication using Mamdani's 'min' operator;
- 4) De-fuzzification using the 'centroid' method.



Fig.14.Conventional Fuzzy Controller.





Fig.15. (a) Input Vdcnormalized membership function; (b) Input Vdc-ref Normalized Membership Function; (c) Output Imax Normalized Membership Function.

Fuzzification:the process of converting a numerical variable (real number) convert to a linguistic variable (fuzzy number) is called fuzzification.De-fuzzification:the rules of FLC generate required output in a linguistic variable (Fuzzy Number), according to real world requirements, linguistic variables have to be transformed to crisp output (Real number).

Database: the Database stores the definition of the membership Function required by fuzzifier and defuzzifier. Rule Base: the elements of this rule base table are determined based on the theory that in the transient state, large errors need coarse control, which requires coarse in-put/ output variables; in the steady state, small errors need fine control, which requires fine input/output variables. Based on this the elements of the rule table are obtained as shown in Table 1, with 'Vdc' and 'Vdc-ref' as inputs.

Table 1. Rule base.							
Var Var	NB	NM	NS	z	PS	PM	PB
NB	NB	NB	NB	NB	NM	NS	Z
NM	NB	NB	NB	NM	NS	z	PS
NS	NB	NB	NM	NS	z	PS	PM
z	NB	NM	NS	z	PS	PM	PB
PS	NM	NS	z	PS	PM	PB	PB
PM	NS	z	PS	PM	PB	PB	PB
PB	z	PS	PM	PB	PB	PB	PB

VI.MATLABRESULTS:

Here simulation is carried out in several cases, proposed UPQC model is evaluated as voltage sag conditions with respect to sudden load changes and same proposed concept is applied to intelligent based fuzzy systems to validate the optimal results and may increase the robustness of the system.



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Fig.16 shows the Matlab/Simulink Model of Proposed UPQC Model with Simplified Control Scheme.





(b)



(c) Fig.17 Source Voltage & Source Current







(c) Fig.18 Load Voltage & Load Current



Fig.19.PAF Currents



Fig.20.SAF Currents.

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(a)THD Analysis of Load Current.



(b)THD Analysis of Load Current. Fig.21 THD Analysis of Source Current & Load Current, without Compensation Source Current Is Equal To Load Current Then THD Value Is 12.41%, When Compensation Is Performed Getting 2.04%, With In IEEE-519 Standards.



(a)









(e)

Fig.22. (A) Source Voltages And Load During A Voltage Dip In Phase A. (B) Load Voltages And Source Currents (C) Load Voltages And Load Currents During A Load Step From 50% To 100%. (D) Load Voltages and Load Currents during A Load Step From 100% To 50%. (E) DC Link Voltages during a Load Step From 100% To 50%.



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Fig.24 THD Analysis of Source Current, with Fuzzy Compensation then THD value is 0.37%, with in IEEE-519 standards.



VII.CONCLUSION:

Mitigation techniques have been proposed and implemented to maintain the harmonic voltages and currents within recommendedlevels by a custom power device DVR. DVR with PI Controller and Fuzzy Logic Controller has been designed tomitigate the effects of the power quality problems during three phase fault condition. But since there is always scope of improvement in minimizing distortions, so membership function of fuzzy logic are optimized by bacterial foraging optimization (BFO) and it has been successfully recorded that total harmonic distortions are very less as compared toother two techniques.

The investigation of DVR installation on a power distribution system with mainly focus onharmonic reduction and voltage regulation performance has been successfully demonstrated in MATLAB/Simulink. It is found that BFO-Fuzzy Logic Control is more effective than PI Control and fuzzy control technique in operation of DVR as a custom power device. Both the active filters from source to load are dip by the RMS voltage in phase "A" to eliminate the harmonics from grid source voltage to load current using fuzzy controller. Thus the result is validated and its proposed scheme of ABC reference of iUPQC using fuzzy control method is used in synchronized sinusoidal reference.

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