ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Design and Implementation of a Decimal Multi-Operand Adder Using A Fast Binary to Decimal Converter

T.J Sunil Daya Sagar
M.Tech Student,
Department of ECE,
DRK Institute of Science and Technology.

Mrs.Sadguna
Assistant Professor,
Department of ECE,
DRK Institute of Science and Technology.

Abstract:

This paper presents a new architecture for a Binary to BCD (BD) converter which forms the core of our Proposed high speed decimal Multi-operand Adder. Our proposed design contains various improvements over existing architectures. These include an improved BD Converter that helps in reducing the delay of the Multi-operand decimal Adder. Simulation results indicate that with a marginal increase in area, the proposed BD converter exhibits an improvement in delay over earlier designs. Further the decimal Multi-operand Adder achieves faster design when compared to previously published results.

Keywords: Decimal Arithmetic, Binary to BCD Converter, Multi-operand Adder;

The use of decimal arithmetic has been increasing over binary due to increase in the applications of internet banking and there are many others places where precision is very important. Binary digits have a disadvantage of not being able to represent digits like 0.1 or 0.7, requires an infinitely recurring binary number. The availability of multi-operand decimal adders can facilitate financial and commercial applications based on existing huge databases. The simultaneous addition of several decimal numbers is the common operation in multiplication and division algorithms. Multi-operand addition is a vital operation as it is a core component of arithmetic operations, such as division and multiplication. In case of decimal multiplication Multi operand decimal addition comes in handy for swiftly summing large amounts of decimal data.This project introduces a multi-operand decimal addition algorithm by employing high speed binary to BCD converter circuit, which speeds up the process of decimal addition when multiple BCD operands are added together. A Novel design for 7-bit binary to BCD converter circuit is proposed. Further, analysis is done with respect to the existing binary to BCD converter architectures.

The proposed algorithm is fundamentally different from multi-operand BCD addition algorithms [3, 5] since intermediate BCD corrections are not done rather correction is done at the final stage to get proper BCD results. As the decimal corrections are achieved separately from the computation of the binary sum, such that the layout of the binary carry-save adder does not require any further rearrangement, the design can perform as unified Binary/ BCD multi-operand adder.

Existing design:

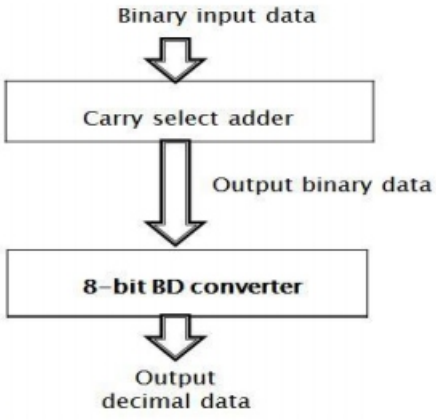

Fig 1. Existed design block diagram

PROPOSED DESIGN:
Multi-operand Decimal Adder:

The binary parallel multi-operand addition is realized using a CSA tree for compressing the input operands. Efficient multi-operand binary adder circuits can be realized using carry-save adders. The absence of carry propagation until the last stage makes the CSA adders very fast [9]. An added advantage is their simple structure. The proposed algorithm is as depicted in the figure 5. It comprises of a binary tree structure formed by 3:2 CSA followed by a high speed Binary to Decimal convertor as depicted in figure 5.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

The proposed multi-operand adder architecture can perform both decimal and binary multi-operand operation. Figure 6 illustrates the multi-operand addition of 8 input operands and a carry in (C in) shown in bold (9+9+9+9+9+9+9+9+7) using the proposed algorithm in figure 5. We have considered the extreme case of each input operand being 9. Further the carry in from the previous multi-operand column can at most be 7.The algorithm computes the binary sum S binary by summing up the input operands in a parallel fashion. Unlike the existing BD converters [7-8] we have removed the contribution blocks resulting in a very fast design at the cost of increase in the complexity of the DH and DL generators as shown in figure. The binary output S binary is fed to the BD converter which produces 2 digit BCD number, S decimal. The design proposed is different from [5] in the sense that the design doesn't do the correction at the intermediate stages, rather it does the decimal conversion after the binary sum has been produced, this improves the performance in terms of speed.

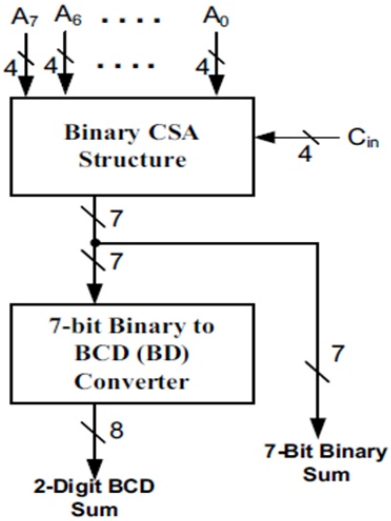

Figure. Proposed Multi-operand Decimal/Binary

$A_0 = 9 = 1001$, $A_1 = 9 = 1001$, $A_2 = 9 = 1001$ → $S_1 = 1001$, $C_1 = 10010$

$A_3 = 9 = 1001$, $A_4 = 9 = 1001$, $A_5 = 9 = 1001$ → $S_2 = 1001$, $C_2 = 10010$

$A_6 = 9 = 1001$, $A_7 = 9 = 1001$, $C_{in} = 7 = 0111$ → $S_3 = 0111$, $C_3 = 10010$

$S_1 = 9 = 1001$, $S_2 = 9 = 1001$, $S_3 = 7 = 0111$ → $S_4 = 0111$, $C_4 = 10010$

$C_1 = 9 = 1001$, $C_2 = 9 = 1001$, $C_3 = 9 = 1001$ → $S_5 = 1001$, $C_5 = 10010$

$C_4 = 9 = 1001$, $C_5 = 9 = 1001$, $S_5 = 9 = 1001$ → $S_6 = 10010$, $C_4 = 1001$

$S_6 = 100100$, $C_6 = 100100$, $S_4 = 0111$ → $S = 0111$, $C = 1001000$

$S_{binary} = 1001111$ → 7-bit BD Converter → $S_{decimal} = 0111\ 1001$ ($D_H\ D_L$)

Figure. Example of proposed eight operand decimal addition.

Proposed 7- bit Binary to BCD Converter:

The proposed BD converter was designed with the intention of speeding up of the multi-operand decimal adder. The 7-bit binary number is converted to the two BCD digits i.e. four LSB bits and four MSB bits of S decimal form DL and DH respectively. In [8] the contribution block adds to the critical path delay of the converter, the proposed design aims at removing these contribution blocks and thereby drastically improving the overall delay of the converter as depicted in figure 1.11.

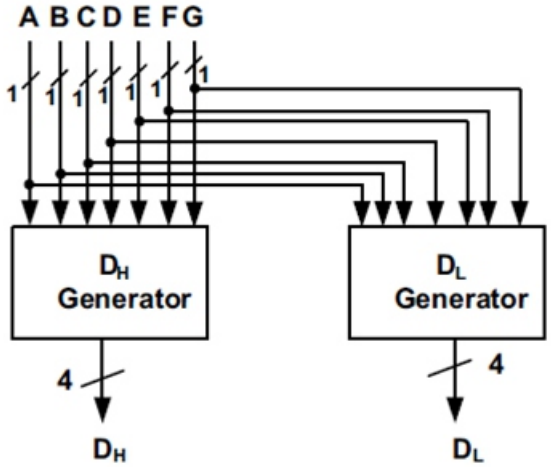

Figure. Proposed 7-bit BD Converter

Instead of splitting and finding the contributions for DH and DL a method is devised to directly find the contribution to each bit of BCD digits by using equations (1) and (2) respectively.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

The maximum BCD number is nine (910 =10012) so eight operand decimal addition will result in a maximum of seventy-two (7210 = 10010002), hence a carry in to higher position can be maximum of seven. So, the proposed BD convertor block has been optimized to convert a maximum of seventy-nine (7910 =10011112), implying in DH the MSBDH3 can never be `1`. Further, it can be observed that the first two MSB bits of S binary cannot be of value `1` simultaneously. Based on this observation the equations (1-2) were devised for the convertor block.

$$D_{Hj} = \sum_{i=0}^{2} P_{ij} \quad (1)$$

TABLE: PROPOSED DH GENERATOR OF 7-BIT BD CONVERTER

j / i	0	1	2	3
	D_{H0}	D_{H1}	D_{H2}	D_{H3}
0	A'B'[DEF+C(D+F)'+C'D(E+F)]	B'C[D+E]	0	0
1	B[C'D'+C[DE'+D'(E+F)]]	B[C'D'+CDE]	B[C+D]	0
2	A[D+EF]	AC'	AC'	0

Where Pij corresponds to (i, j) element in the Table II The four MSB bits DH0, DH1, DH2 and DH3 are formed by replacing j =0, 1, 2, 3 in (1). From the Table I and (1) we can obtain the value of DH as follows.

Case I: j = 0

$$D_{H0} = A'B'[DEF + C(D+F)' + C'D(E+F)] + B[C'D' + C[DE' + D'(E+F)]] + A[D+EF] \quad (2)$$

Similarly we can obtain the values of DH1, DH2, DH3 by replacing the value of j = 1, 2, 3 in (1)

$$D_{Lj} = \sum_{i=0}^{2} Q_{ij} \quad (3)$$

TABLE: PROPOSED DL GENERATOR OF 7-BIT BD CONVERTER

i / j	0	1	2	3
	D_{L0}	D_{L1}	D_{L2}	D_{L3}
0	G	A'B'[C'[D'F+DEF']+C[DE'F+D'[E⊕F]']]	A'B'[CE'[D+F'] + C'E[F+D']]	A'B'[C'DE'F' + C[DEF'+D'E'F]]
1	G	B[D'F'[E+C'] + D[CE'F'+F[E+C']]]	B[C[E'F'D+EFD']+ C'[E⊕ [DF']]]	B[CE'[D⊕ F]'+ C'D'EF]
2	G	A[DF'+C'E'F]	A[E'F+EF'D]	AE[F⊕ D]'

Where Qij corresponds to (i, j) element in the Table 1.4.The four LSB bits DL0, DL1, DL2, DL3 are produced by Substituting j =0, 1, 2, 3 in (3). From the Table II and (4) we can achieve the value of four bits of DL as follows.

Case I: j = 0

$$D_{L0} = G \quad (4)$$

On similar lines we can obtain the values of DL1, DL2 and DL3 By substituting the value of j = 1, 2, 3 in (3).

SIMULATION RESULTS:

All the 7-bit Binary to BCD converters and Multi operand structures were described using Verilog data flow modeling and simulated using Cadence Incisive Unified Simulator (IUS) v6.1. The Binary to BCD converters and Multi-operand designs were mapped on TSMC 180nm Technology Slow-Normal library (operating conditions 0.9V, 125ºC) using Cadence RTL Compiler v7.1. All the inputs were set to have a toggle rate of 50%. Multi-operand structures based on the proposed algorithm were designed and the Binary to BCD converter in the proposed algorithm was replaced with that of architecture [8] for fair comparisons. Table III shows the comparison of Binary to BCD converter with existing design [8]. Synthesis results show that there is a reduction in delay by 55 % with a tradeoff in power by 18 %. This in turn reduces power delay product by 27 %.

TABLE: COMPARISON OF PROPOSED BINARY TO BCD DESIGN WITH FOUR –THREE SPLIT AND THREE– FOUR SPLIT [8] BINARY TO BCD DESIGNS:

Metric	Proposed Design	Four –Three Split [8]	Three –Four Split [8]
Area (µm2)	201.802 (100%)	137.592 (68%)	150.293 (74.5%)
Delay (pS)	590F (100%)	914 (155%)	845 (143%)
Power (nW)	3282.645 (100%)	2703.367 (82.3%)	2693.709 (82%)
Power Delay Product (fJ)	1.936734 (100%)	2.470907 (127.6%)	2.276176 (117%)

Comparison between proposed multi-operand adder and modified multi-operand adder designed using Four –Three Split and Three– Four Split is presented in Table IV. From the Table, it is evident that there is improvement in delay by 15% and in turn reduces power delay product by 13%.From these three designs, the proposed multi-operand adder in conjunction with modified multi-operand adder using Four –Three Split and Three– Four Split gives better performance in terms speed as well as power –delay product.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Further it is evident from Table IV that the proposed design performs better compared to with respect to delay as well as power delay product.

TABLE: COMPARISON OF PROPOSED-MULTI-OPERAND ADDER WITH MODIFIED FOUR-THREE SPLIT AND THREE–FOUR SPLIT [8] ADDERS:

Metric	Area (µm2)	Delay (pS)	Power (nW)	Power Delay Product (fJ)
Proposed Design	749.3 (100%)	2146 (100%)	34937.9 (100%)	74.976 (100%)
Design A [8]	685.1 (91.4%)	2470 (115%)	34358.7 (98.3%)	84.86 (113.2%)
Design B [8]	697.8 (93.1%)	2401 (112%)	34349 (98.3%)	82.472 (110%)
Dadda [4]	655.5 (87.5%)	2429 (113 %)	33382.2 (95.5%)	81.08 (108 %)

Design A: Four –Three split converter
Design B: Three– Four split converter

CONCLUSION:

A Novel Unified BCD/ Binary multi-operand addition algorithm has been proposed. The binary parallel multi operand addition is realized using a CSA tree for compressing the input operands. The proposed BD converter forms the core of the multi-operand decimal adder. Simulation results demonstrate the efficiency of our proposed BD converter as well as multi-operand decimal adder with respect to exiting designs.

REFERENCES:

[1] M. F. Cowlishaw. Decimal floating-point: Algorism forcomputers. In Proc. IEEE 16th Symposium on Computer Arithmetic,pages 104–111, July 2003.

[2] M. D. Ercegovac and T. Lang, Digital Computer Arithmetic.Elsevier/Morgan Kaufmann Publishers,2004.

[3] R. D. Kenney and M. J. Schulte. High-speed multi-operanddecimal adders. IEEE Trans. on Computers, 54(8):953–963,Aug.2005.

[4] Dadda, Luigi. "Multi-operand parallel decimal adder: A mixedbinary and bcd approach." Computers, IEEE Transactions on 56.10(2007): 1320-1328.

[5] Lin, Kuan Jen, et al. "A parallel decimal adder with carrycorrection during binary accumulation."New Circuits and SystemsConference (NEWCAS), 2012 IEEE 10th International.IEEE, 2012.

[6]- Jaberipur, Ghassem, and Amir Kaivani. "Improving the speed ofparallel decimal multiplication." Computers, IEEE Transactions on58.11 (2009): 1539-1552.

[7]- Bhattacharya, Jairaj, Aman Gupta, and Anshul Singh. "A highperformance binary to BCD converter for decimal multiplication."VLSI Design Automation and Test (VLSI-DAT), 2010 InternationalSymposium on. IEEE, 2010.

[8]- Al-Khaleel, Osama, et al. "Fast and compact binary-to-BCDconversion circuits for decimal multiplication." Computer Design(ICCD), 2011 IEEE 29th International Conference on. IEEE, 2011.

[9] S. Knowles, ''A family of adders,'' in: Proceedings of the 14thIEEE Symposium on Computer Arithmetic, pp. 30–34, 1999.