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Simulation of Nine Level Grid Connected Inverter with PWM Technique for Harmonic Reduction

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Abstract:

This paper implements a single phase nine-level inverter for grid connected photovoltaic systems, by using a novel pulse-width modulated (PWM) control technique. This control technique generates pulses by comparing three reference signals with a carrier signal. These three reference signals are identical to each other with an offset equivalent to the amplitude of triangular carrier signal. The implemented nine-level inverter produces nine-levels of output voltages (Vdc , 3Vdc/4 , 2Vdc/4 , Vdc/4 , 0 , -Vdc/4 , -2Vdc/4 , -3Vdc/4 , -Vdc) from the dc supply voltage. This implemented inverter is based on modified H-bridge converter which uses only seven switches instead of sixteen switches as in conventional method. The nine-level inverter is implemented from a seven level inverter by using an additional switch and a capacitor, and both outputs are compared. The behavior of nine level inverter is analysed in detail and verified through simulation.

Keywords:

Photovoltaic(PV)system, Modified H-Bridge Inverter, Pulsewidth modulated (PWM).

I. INTRODUCTION:

Due to the increase in energy consumption, cost of fossil fuels & non renewable energy sources which are depleting the environment created an interest towards renewable energy sources one of which is photovoltaic system. This system directly converts the solar energy into electricity. Phototvoltaic generated energy is delivered to the power system networks by means of grid connected inverters. Multilevel inverters offer: nearly sinusoidal output voltage waveforms, output current with better harmonic profile, less stress of electronic components, less switching losses, small filter size, and low EMI (Electro Magnetic Interference).

Due to these advantages different topologies of multilevel inverters have been proposed over the years. Commonly used multilevel inverters are: diode clamped, flying capacitor, cascaded H-bridge, and modified H-bridge multilevel inverter.This paper uses novel modified H-bridge inverter which consists of three diode embedded bidirectional switches and a conventional H-bridge inverter. The modified H-bridge inverter is advantageous over other topologies. It requires: less power switch, power diodes, and less capacitors for inverters of the same number of levels.

II. INVERTER:

Introduction to Inverters:

D.C.-A.C. inverters are electronic devices used to produce mains voltage A.C. power from low voltage D.C. energy (from a battery or solar panel). This makes them very suitable for when you need to use A.C. power tools or appliances but the usual A.C. mains power is not available. Examples include operating appliances in caravans and mobile homes, and also running audio, video and computing equipment in remote areas. Most inverters do their job by performing two main functions: first they convert the incoming D.C. into A.C., and then they step up the resulting A.C. to mains voltage level using a transformer. And the goal of the designer is to have the inverter perform these functions as efficiently as possible so that as much as possible of the energy drawn from the battery or solar panel is converted into mains voltage A.C., and as little as possible is wasted as heat.

Square-wave or quasi- wave voltages may be acceptable for low and medium power applications, and for high applications low-distorted, sinusoidal waveforms are required. The output frequency of an inverter is determined by the rate at which the semi-conductor devices are switched on and off by the inverter control circuitry and consequently, an adjustable frequency A.C. output is readily provided.

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The harmonic contents of output voltage can be minimized or reduced significantly by switching techniques of available high speed power semiconductor devices.The D.C. power to the inverter may be battery, fuel cell, solar cells or other D.C. source. But in most industrial applications it is fed by rectifier. This configuration of A.C. to D.C. converter and D.C. to A.C. inverter is called a D.C. link. The main objective of static power converters is to produce an ac output waveform from a dc power supply. These are the types of waveforms required in adjustable speed drives (ASDs), uninterruptible power supplies (UPS), static var compensators, active filters, flexible ac transmission systems (FACTS), and voltage compensators, which are only a few applications.

SINGLE PHASE SEVEN LEVEL INVERTER:

Single Phase seven level inverter consists of a single phase conventional H-bridge inverter, two bidirectional switches, and a capacitor voltage divider formed by C1,C2,C3, as shown in fig.1.

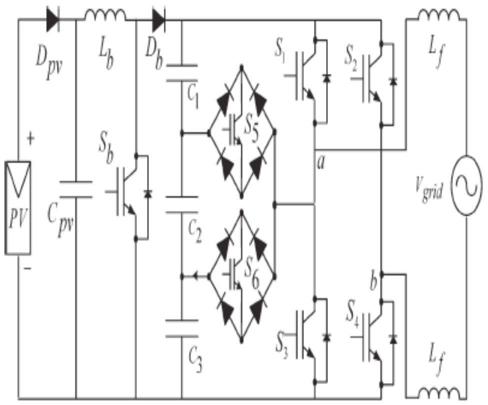

Fig.2.Single Phase Grid Connected Inverter For Photovoltaic System

Photovoltaic (PV) arrays were connected to the inverter by means of a dc-dc boost converter. The dc-dc- boost converter is used to increase the PV array voltage since it is less than the grid voltage. Lf (filter inductance) is used to filter the current injected into the grid. This inverter can be operated in seven switching states depending on the output voltages, as shown in fig. 2(a)-(g). The seven levels of output voltages are:
Vdc, 2Vdc/3, Vdc/3, 0, -Vdc/3, -2Vdc/3, -Vdc.
These seven levels of output voltages were generated as follows:

1) Maximum positive output (Vdc): S1 is ON, connecting the load positive terminal to Vdc, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is Vdc. Fig. 2(a) shows the current paths that are active at this stage.

2) Two-third positive output (2Vdc/3): The bidirectional switch S5 is ON, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is 2Vdc/3. Fig. 2(b) shows the current paths that are active at this stage.

3) One-third positive output (Vdc/3): The bidirectional switch S6 is ON, connecting the load positive terminal, and S4 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is Vdc/3. Fig. 2(c) shows the current paths that are active at this stage.

4) Zero output: This level can be produced by two switching combinations; switches S3 and S4 are ON, or S1 and S2 are ON, and all other controlled switches are OFF; terminal ab is a short circuit, and the voltage applied to the load terminals is zero. Fig. 2(d) shows the current paths that are active at this stage.

5) One-third negative output (−Vdc/3): The bidirectional switch S5 is ON, connecting the load positive terminal, and S2 is ON, connecting the load negative terminal to Vdc. All other controlled switches are OFF; the voltage applied to the load terminals is −Vdc/3. Fig. 2(e) shows the current paths that are active at this stage.

6) Two-third negative output (−2Vdc/3): The bidirectional
switch S6 is ON, connecting the load positive terminal, and S2 is ON, connecting the load negative terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is −2Vdc/3. Fig. 2(f) shows the current paths that are active at this stage.

7) Maximum negative output (−Vdc): S2 is ON, connecting the load negative terminal to Vdc, and S3 is ON, connectin the load positive terminal to ground. All other controlled switches are OFF; the voltage applied to the load terminals is −Vdc. Fig. 2(g) shows the current paths that are active at this stage.

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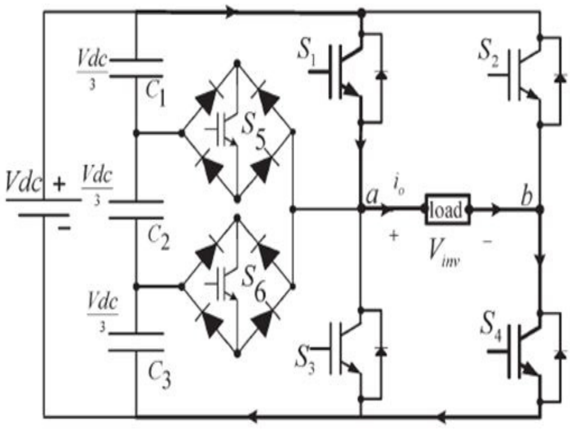

Fig 2(a) Inverter circuit for the output voltage (Vdc)

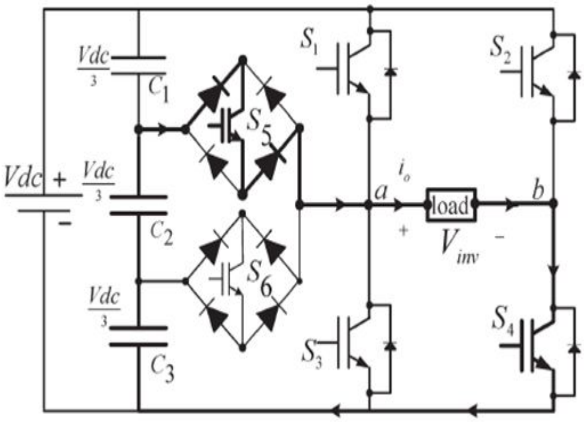

Fig 2(b) Inverter circuit for the output voltage (2Vdc/3)

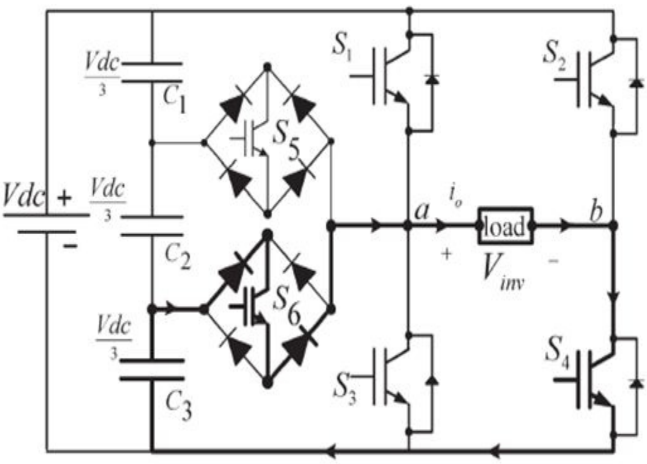

Fig 2(c) Inverter circuit for the output voltage (Vdc/3)

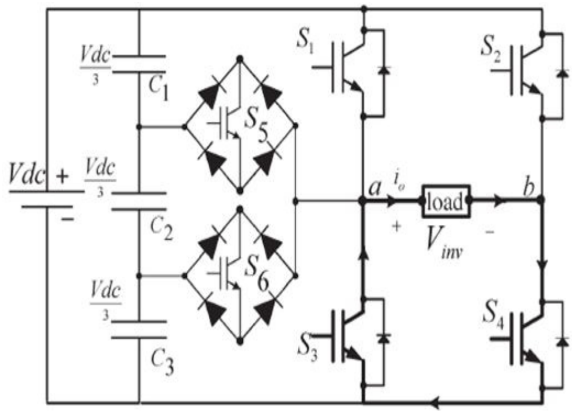

Fig 2(d) Inverter circuit for the output voltage (zero 0)

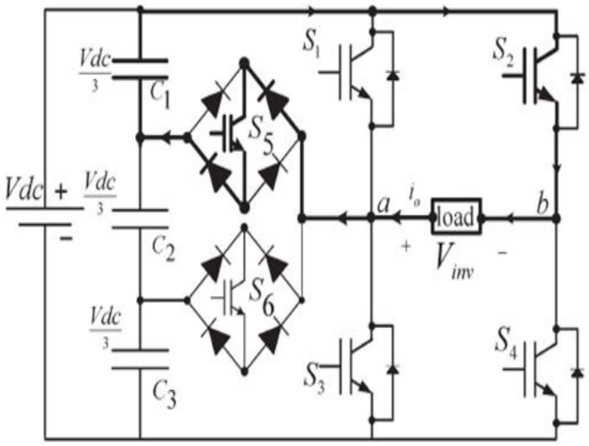

Fig 2(e) Inverter circuit for the output voltage (-Vdc/3)

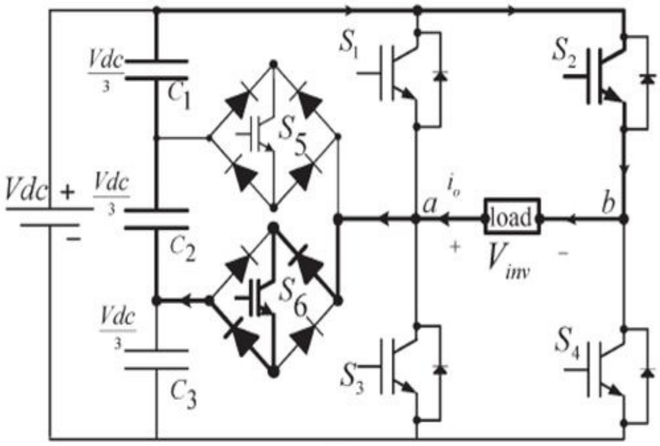

Fig 2(f) Inverter circuit for the output voltage (-2Vdc/3)

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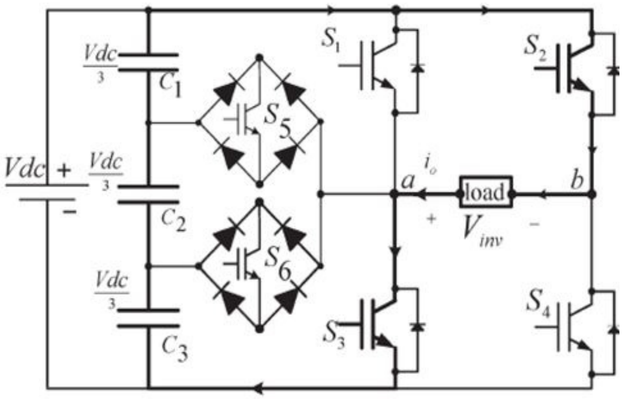

Fig 2(g) Inverter circuit for the output voltage (-Vdc)

TABLE I:UTPUT VOLTAGE ACCORDING TO THE SWITCHES ON–OFF CONDITION

v_0	S_1	S_2	S_3	S_4	S_5	S_6
V_{dc}	on	off	off	on	off	off
$2V_{dc}/3$	off	off	off	on	on	off
$V_{dc}/3$	off	off	off	on	off	on
0	off	off	on	on	off	off
0*	on	on	off	off	off	off
$-V_{dc}/3$	off	on	off	off	on	off
$-2V_{dc}/3$	off	on	off	off	off	on
$-V_{dc}$	off	on	on	off	off	off

III.PWM MODULATION:

The Novel PWM modulation technique generates switching pulses for the switches. Three reference signals (Vref1, Vref2, and Vref3) were compared with a carrier signal (Vcarrier). The reference signals had the same frequency and amplitude and were in phase with an offset value that was equivalent to the amplitude of the carrier signal. The reference signals were each compared with the carrier signal. If Vref1 had exceeded the peak amplitude of Vcarrier, Vref2 was compared with Vcarrier until it had exceeded the peak amplitude of Vcarrier. Then, onward, Vref3 would take charge and would be compared with Vcarrier until it reached zero. Once Vref3 had reached zero, Vref2 would be compared until it reached zero. Then, onward, Vref1 would be compared with Vcarrier. Fig. 3 shows the resulting switching pattern. Switches S1, S3, S5, and S6 would be switching at the rate of the carrier signal frequency, whereas S2 and S4 would operate at a frequency that was equivalent to the fundamental frequency.

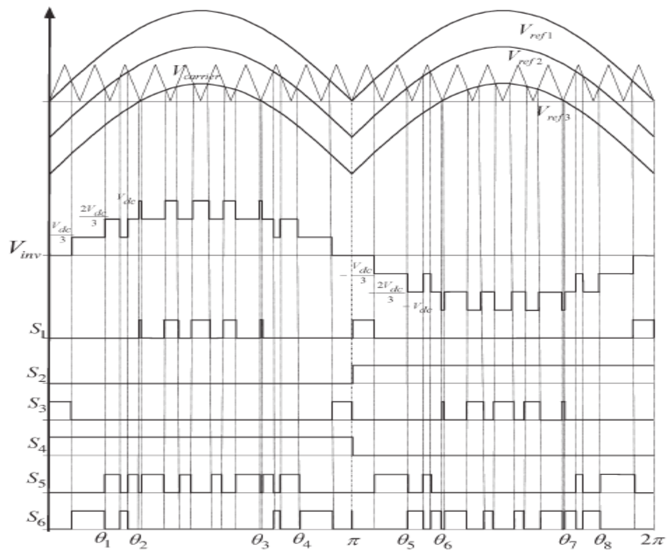

Fig. 3. Switching Pattern For The Single Phase Seven-Level Inverter.

IV.CONTROL SYSTEM:

The control system comprises of MPPT algorithm, a dc-bus voltage controller, reference current generator, and a current controller, as shown in fig. 5. The two main tasks of the control system are maximization of the energy transferred from the PV arrays to the grid, and generation of a sinusoidal current with minimum harmonic distortion, also under the presence of grid voltage harmonics.

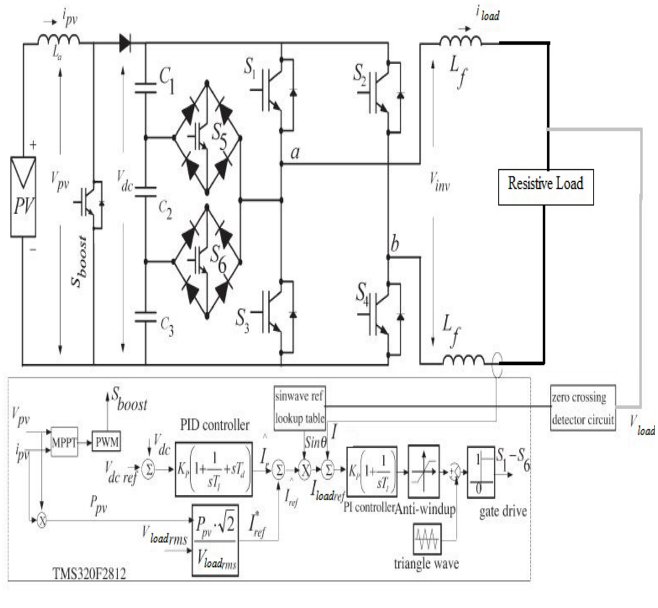

Fig. 4. Seven-level inverter with closed-loop control algorithm

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The proposed inverter utilizes the perturb-and-observe (P&O) algorithm for its wide usage in MPPT owing to its simple structure and requirement of only a few measured parameters. It periodically perturbs (i.e., increment or decrement) the array terminal voltage and compares the PV output power with that of the previous perturbation cycle. If the power was increasing, the perturbation would continue in the same direction in the next cycle; otherwise, the direction would be reversed. This means that the array terminal voltage is perturbed every MPPT cycle; therefore, when the MPP is reached, the P&O algorithm will oscillate around it.

The P&O algorithm was implemented in the dc–dc boost converter. The output of the MPPT is the duty-cycle function. As the dc-link voltage Vdc was controlled in the dc–ac sevenlevel PWM inverter, the change of the duty cycle changes the voltage at the output of the PV panels. A PID controller was implemented to keep the output voltage of the dc–dc boost converter (Vdc) constant by comparing Vdc and Vdc ref and feeding the error into the PID controller, which subsequently tries to reduce the error. In this way, the Vdc can be maintained at a constant value and at more than √2 of Vgrid to inject power into the grid.

To deliver energy to the grid, the frequency and phase of the PV inverter must equal those of the grid; therefore, a grid synchronization method is needed. The sine lookup table that generates reference current must be brought into phase with the grid voltage (Vgrid). For this, the grid period and phase must be detected.The overall response is controlled under this block and the different PID controllers are used for the generation of the sinusoidal signal and the sine lookup table and zero crossing detector are used for the sinusoidal signal. The overall response is controlled under the closed loop conditions to get the accurate output.

V.PROPOSED NINE LEVEL INVERTER TOPOLOGY:

The single phase nine-level inverter is implemented from the seven-level inverter. It comprises of a single-phase conventional H-bridge inverter, three bidirectional switches, and a capacitor voltage didvider formed by C1,C2,C3,C4.This requires an additional bidirectional switch and a capacitor C4.The switching sequence for the nine level inverter is shown below.

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TABLE II: Output Voltage according to the switches' On-Off Condition:

V_0	S_1	S_2	S_3	S_4	S_5	S_6	S_7
Vdc	On	Off	Off	On	Off	Off	Off
3Vdc/4	Off	Off	Off	On	On	Off	Off
2Vdc/4	Off	Off	Off	On	Off	On	Off
Vdc/4	Off	Off	Off	On	Off	Off	On
0	Off	Off	On	On	Off	Off	Off
0*	On	On	Off	Off	Off	Off	Off
-Vdc/4	Off	On	Off	Off	On	Off	Off
-2Vdc/4	Off	On	Off	Off	Off	On	Off
-3Vdc/4	Off	On	Off	Off	Off	Off	On
-Vdc	Off	On	On	Off	Off	Off	Off

VI.SIMULATION RESULTS:

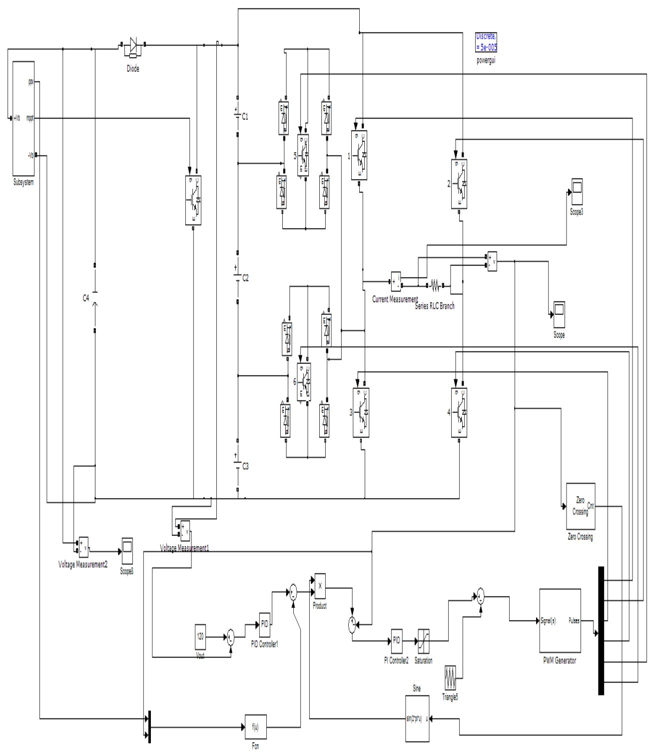

Fig 6.1 Main MATLAB/SimuLink Block diagram for Seven level inverter

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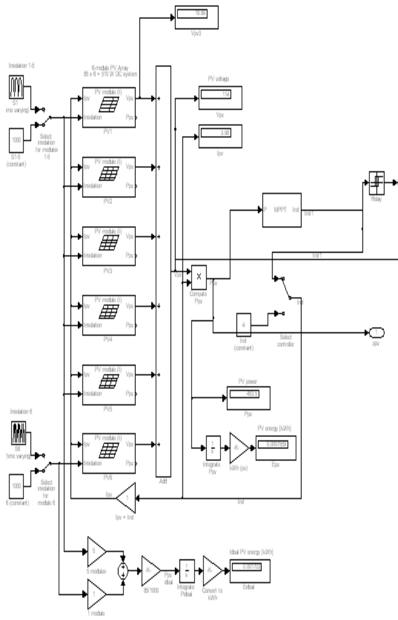

Fig 6.2 Internal PV Block Diagram

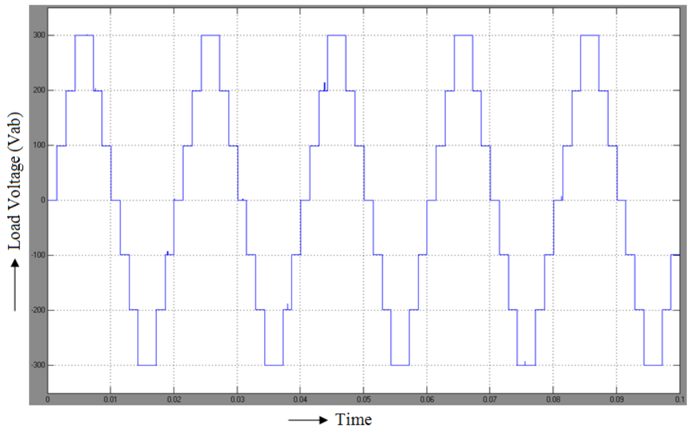

Fig 6.3 Seven levels of Inverter output voltage (Vinv)

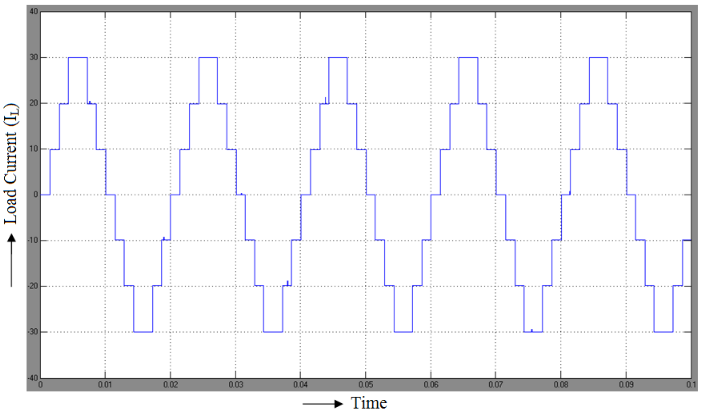

Fig 6.4 Seven levels of Inverter output current (Iinv)

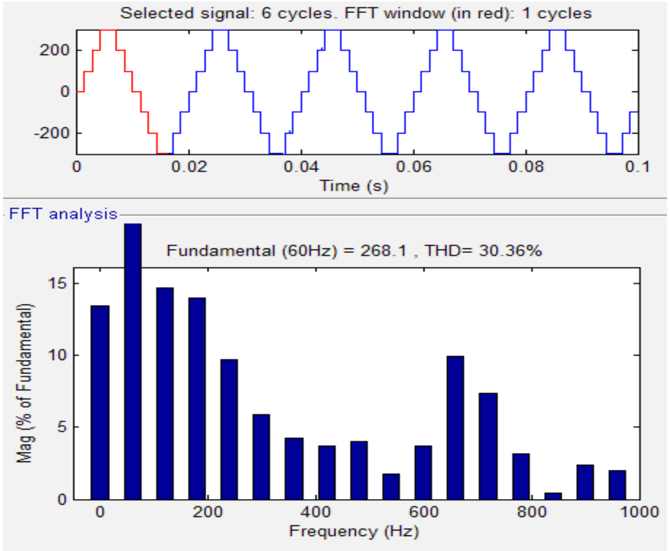

Fig 6.5. THD for seven level inverter

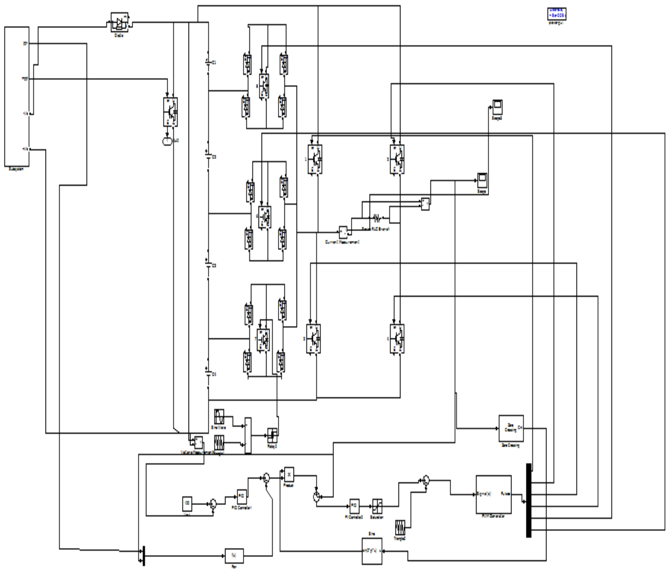

Fig 6.6. Main MATLAB/SimuLink Block diagram for Nine level inverter

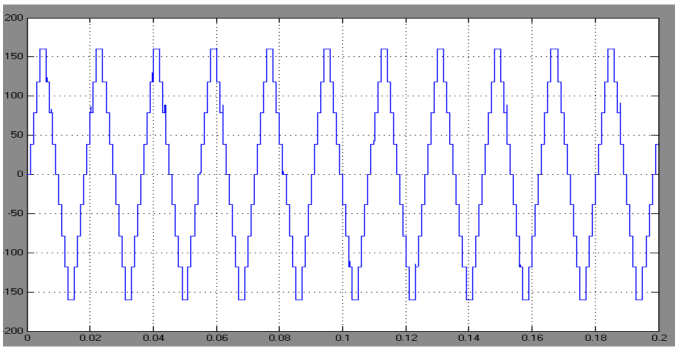

Fig 6.7. Nine levels of Inverter output voltage (Vinv)

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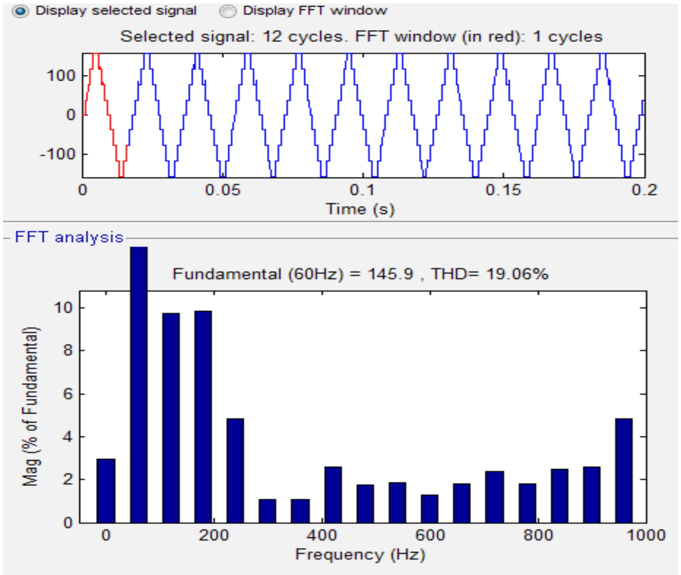

Fig. 6.8. THD for nine level inverter

VII.CONCLUSION:

Multilevel inverters offer improved output waveforms and lower THD. This project has presented a novel PWM switching scheme for the proposed multilevel inverter. It utilizes three reference signals and a triangular carrier signal to generate PWM switching signals. The behavior of the proposed multilevel inverter was analyzed in detail. By controlling the modulation index, the desired number of levels of the inverter's output voltage can be achieved. The less THD in the nine-level inverter is an attractive solution for grid-connected PV inverters. By using this nine level inverter we can improve the overall response of the system with the less number of switching states and the reliable operation. By increasing the number of levels we can decrease the Total Harmonic Distortion (THD) and to get the exact sinusoidal output, and by using the less number of switches we can get the 11-level, and 48-level output distortions less. By this the THD will be minimized. Lower the THD means the output Efficiency is more.By comparing the THD of seven and nine level we can conclude that by increasing the level the harmonics can be reduced.

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