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Energy and Area Efficient Three-Input XOR/XNORs with Gate Diffusion input Methodology

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Abstract
In this brief, we propose three efficient three-input XOR/XNOR circuits as the most significant blocks of digital systems with a new systematic cell design methodology (SCDM) in hybrid-CMOS logic style.

SCDM, which is an extension of CDM, plays the essential role in designing efficient circuits. At first, it is deliberately given priority to general design goals in a base structure of circuits. This structure is generated systematically by employing binary decision diagram. After that, concerning high flexibility in design targets, SCDM aims to specific ones in the remaining three steps, which are wise selections of basic cells and amend mechanisms, as well as transistor sizing.

In the end, the resultant three-input XOR/XNORs enjoy full-swing and fairly balanced outputs. They perform well with supply voltage scaling, and their critical path contains only two transistors. They also outperform their Counter parts exhibiting 27%–77% reduction in average energy-delay product in HSPICE simulation based on TSMC 0.13-μm technology. The symmetric schematic topologies significantly simplify and minimize the layout, as 26%–32% improvement in area is demonstrated.

Index Terms—Binary decision diagram applications, energy efficiency, hybrid-CMOS logic style, systematic design methodology, three-input XOR/XNOR circuits.

1.INTRODUCTION

With the rapid growth of portable electronic devices, it is becoming a critical challenge to design low-power, high-speed (LPHS) circuits that occupy small chip areas. We see many published papers that compete in designing better circuits. Such studies mostly rely on creative design ideas but do not follow a systematic approach. As a consequence, most of them suffer from some different disadvantages

1) They are implemented with logic styles that have an incomplete voltage swing in some internal nodes, which leads to static power dissipation.

2) Most of them suffer from severe output signal degradation and cannot sustain low-voltage operation.

3) They predominantly have dynamic power consumption for non balanced propagation delay inside and outside circuits, which results in glitches at the outputs.

2. SCDM FOR THREE-INPUT XOR/XNOR CIRCUITS

In the first stage, a three-input XOR/XNOR as one of the most complex and all-purpose three-input basic gates in arithmetic circuits has been chosen. If the efficiency of the circuits is confirmed in such a competitive environment, it can show the strength of the methodology. In the second stage, CDM is matured as systematic CDM (SCDM) in designing the three-input XOR/XNORs for the first time. It systematically generates elementary basic cell (EBC) using binary decision diagram (BDD), and wisely chooses circuit components based on a specific target. This takes place when the mentioned features are not considered in the

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CDM. Therefore, after the systematic generation, the SCDM considers circuit optimization based on our target in three steps: 1) wise selection of the basic cell; 2) wise selection of the amend mechanisms; and 3) transistor sizing. It should be noted that BDD can be utilized for EBC generation of other three-input functions. We consider the power-delay product (PDP) as the design target. It stands as a fair performance metric, precisely involving portable electronic system targets. The motivation to use this methodology is the presence of some unique features and the ability to produce some efficient circuits that enjoy all these advantages.

1)The SCDM divides a circuit structure into a main structure and optimization-correction mechanisms. In the main structure, it considers features including the least number of transistors in critical path, fairly balanced outputs, being power ground- free, and symmetry. The mechanisms have the duty of completing the functionality of the circuits, avoiding any degradation on the output voltage, and increasing the driving capability.

2) The least number of transistors in critical path increases the chances of the circuit to have better characteristics, as experimental results have shown an average saving of 10%–50% and 27%–77% in terms of delay and Energy-Delay Product (EDP), respectively.

3) The dynamic consumption optimization comes from the fact of well-balanced propagation delay. This feature is advantageous for applications in which the skew between arriving signals is critical for proper operation, and for cascaded applications to reduce the chance of making glitches.

4) Power-ground-free main structure leads to power reduction.

5)Symmetrical structure, high modularity, and regular arrangement of designs give rise to sharing more wells of connected transistors and in turn reducing the occupied area about 26%–32%.

6)The degradation in all output voltage swing can thus be completely removed, which makes the design sustainable in low *V*DD operations and low static power dissipation.

7) Internal logic structure of designs has the potential to be energy efficient about 17%–53% due to the combined reduction of power consumption and propagation delay.

8) SCDM utilizes the benefits of different logic styles as the hybrid style.

9) The methodology has high flexibility in target and systematically considers it in the three design steps. This can lead to

In this methodology for three-input XOR/XNORs is presented according to the flowchart shown in Fig. 1(a). The design path is started by EBC systematic generation. In this step, general design goals are considered that the most distinctive ones are generating fairly balanced outputs, symmetric and power-ground-free structure, fewer transistors in the critical path, as well as sharing common sub circuit. Systematic generation process of EBC in details is discussed in Section III-A. In the remaining steps, the methodology offers opportunity to strive toward an assigned design target. Two of these steps include wisely selection of mechanisms and basic cells from PDP point of view. An in-depth analysis for the selection.

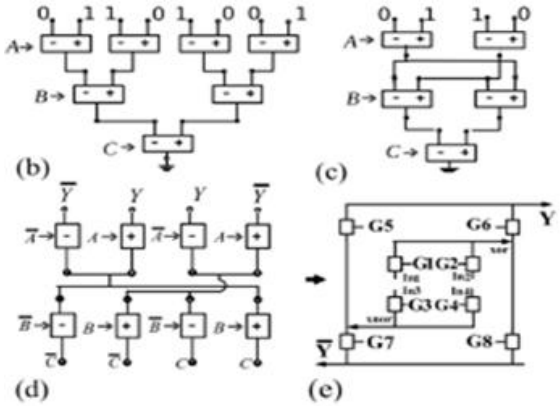

Fig. 1. (a) SCDM process for designing efficient three-input XOR/XNORs. (b) BDT representation of three-input XOR/XNOR function. (c) Applying reduction rules. (d) Substitution and disjointing. (e) EBC

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Elementary Basic Cell Systematic Generation:

In order to generate the EBC of three-input XOR/XNOR circuits, four steps are taken. The process has been shown in Fig. 1(e). Initially, three-input XOR and its complement is represented by one binary decision tree (BDT) in order to share common sub circuits. The BDT is achieved by some cascaded 2 ×1 MUX blocks, which are denoted by simplified symbol controlled with input variables at each correspondent level. This construction simply implements the min terms of the three-input XOR/XNOR function, as shown in Fig. 1(b). The step is followed by applying reduction rules to simplify the BDT representation.

These include elimination, merging, and coupling rules. The major task of the coupling rule, in simple terms, is to obtain all the possible equivalent trees by interchanging the order of the controls. The trees are acquired by impacting the state matrix on the corresponding control matrix where the multiply and add operators operate as follows

$0\_\cdot \chi i = \chi$
$1\_\cdot \chi i = \chi$
$\chi 1$
$+\hat{} \chi 2$
$+\hat{} \cdot \cdot \cdot +\hat{} \chi m = \chi 1 \chi 2 \ldots \chi m = 11 \ldots 1 = I2m-1.$

The result of applying the reduction rules to the tree is shown in Fig. 1(c). Afterward, as the inputs into the first level are 0's and 1's of the function's truth table, the 0 and 1 can be replaced by the Y and $Y\_$, respectively. Finally, the simplified symbol can be divided into two distinct symbols: 1) the plus sign with the x input control and 2) the minus sign with the $x\_$ input control. The result of applying steps 3 and 4 is shown in Fig. 1(d). The EBC, which is extracted from the above procedure, has been presented in Fig. 1(e).

This cell has eight elements, deciding two outputs. We refer to the pins of the central section (IN1–IN4 and G1–G4) as A or C, or their complements. We also assume that pins of the external section $G5$–$G8$ can also be B or its complement.

Wisely Selection of Mechanisms and Cells Based on Design Target:

By replacing the elements with pass transistors or transmission gates and the control inputs with input signals in combination with optimization and correction mechanisms, a huge circuit library is achieved as each circuit can be appropriate for specific applications. The selection is meditated to determine dominant mechanisms and cells, in terms of PDP, power, and delay when the optimization goal is PDP. The results are used to produce circuits for high-performance portable electronic applications.

Mechanisms include optimization mechanisms to resolve non full swing [inverter (I) and feedback (F)], correction mechanisms to resolve high impedance [pull up-down network (P) and feedback (F)], or the combinations of them [bootstrap-pull (BP) up-down, feedback pull (FP) up-down, bootstrap-feedback (BF), inverter-feedback (IF), and inverter-pull (IP) up-down]. The cells are divided into three categories: 1) cells with both nMOS and pMOS in EBC structure ($C1$); 2) only nMOS ($C2$); and 3) only pMOS ($C3$). To reduce complexity, we have also considered the central part of EBC and to achieve real results, the circuits have been simulated in the chain test bench [7]. The circuits have been named with the abbreviation of the mechanism (or cell) being utilized, while the other circumstances, cells, or mechanisms are assumed to be fixed. Using transmission gates in EBC, which is called TG, the complete circuit is achieved as there is no need for any other mechanisms.

Therefore, TG is compared separately with others. Fig. 2(a) shows the order of mechanisms in terms of average power and PDP in voltage range from 0.6 to 2 V. If the concentration is on delay consumption, the right chart can be useful [Fig. 2(b)]. Fig. 2(c) also shows the PDP details for different mechanisms.

INTRODUCTION OF THE STRUCTURE OF THREE-INPUT XOR/XNOR CIRCUITS WITH THE AVERAGE PDP IN FEMTOJOULE

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Circuits	centeral part				external part				avg PDP
	BC	mechanisms F	B	P	BC	mechanisms F	B	P	
XO1	TG				C1	Fnp	-	-	1.27
XO2	C2	Fnp	-	-	C2	Fnp	-	-	0.70
XO3	TG				C2	Fp	-	-	0.62
XO4	TG				TG				0.42
XO5	TG				C1	Fnp	-	✓	0.71
XO6	C2	Fnp	-	-	C2	Fnp	-	✓	0.57
XO7	TG				C2	Fp	-	✓	0.47
XO8	TG				C1	-	p&n	✓	0.86
XO9	C2	Fnp	-	-	C2	-	p	✓	0.65
XO10	TG				C2	-	n	✓	0.50

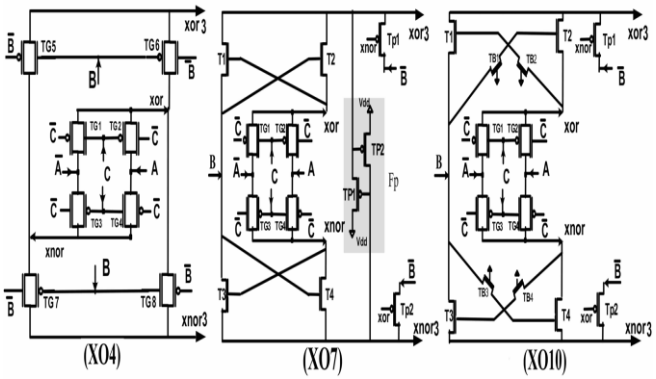

Fig.4. Three-input XOR/XNOR circuits, XO4, XO7, and XO10.

To control the volume of this brief, only the simulation results of the conventional and three of the best proposed circuits in terms of average PDP according to Table I, XO4, XO7, and XO10, are tabulated in Table II. The ascending order of delay, which is the maximum delay between all the possible transitions, as well as PDP are also shown in Fig. 5(a). It is apparent that among the circuits, XO4 and XO7 have the smallest delays. XO7 has slightly less delay than the XO4 at lower supply voltages. However, the trend will reverse at higher supply voltages. Hernandez1 has the second position. The circuits XO10, TF, and 18 T_NEW_FS follow the Hernandez1. In the common circumstances, the circuits utilizing FP, such as XO7 is superior to the circuits utilizing BP like XO10, which is compatible with the delay trend of mechanisms in Fig. 2. The circuits with *C*2 like XO10 and XO7 also perform better than the circuits with *C*1. Since bootstrap technique saves the internal node voltages, the average power dissipation under different supply voltages shows that PB has less power dissipation in common situation. XO10 employing BP outperforms XO7 employing FP with regard to average power. According to the PDP trend in Fig. 2, the ability of TG to provide full-swing leads to the best circuit with optimum performance and drivability as among the circuits, XO4 has the lowest PDP. After that, circuits XO7 and XO10 have the second and third position, respectively. PDP of XO7 is less than that of XO10 for lower voltages but the trend reverses for higher voltages. Hence, from energy point of view, XO7 is a better choice. The circuits, such as XO7 using FP outperform the circuits using F. The circuits with *C*2 like XO7 and XO10 offer less PDP than the circuits with *C*1.

3. GDI-GATE DIFFUSION INPUT 3 INPUT XOR/XNOR GATE

The GDI method which is first proposed by A. Morgenstern, A. Fish, and I. A. Wagner in 2001 [1], is based on the use of a simple cell as shown in figure.4. At first glance, the basic cell reminds the standard CMOS inverter, but there are some important differences: 1. The GDI cell contains three inputs: G (common gate input of nMOS and pMOS), P (input to the source/drain of pMOS), and N (input to the source/drain of nMOS). 2. Bulks of both nMOS and pMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with a CMOS inverter. It must be remarked that not all of the functions are possible in standard p - well CMOS process but can be successfully implemented in twin - well CMOS or silicon on insulator (SOI) technologies.

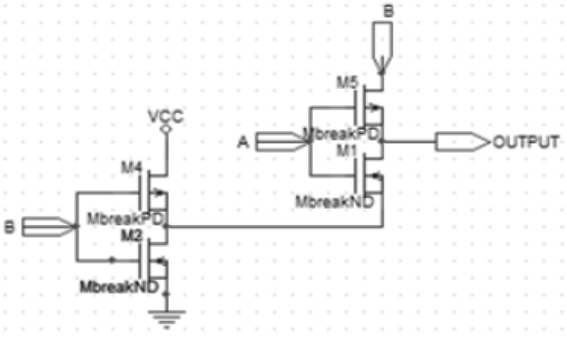

Fig5: Two input XOR/XNOR gate design

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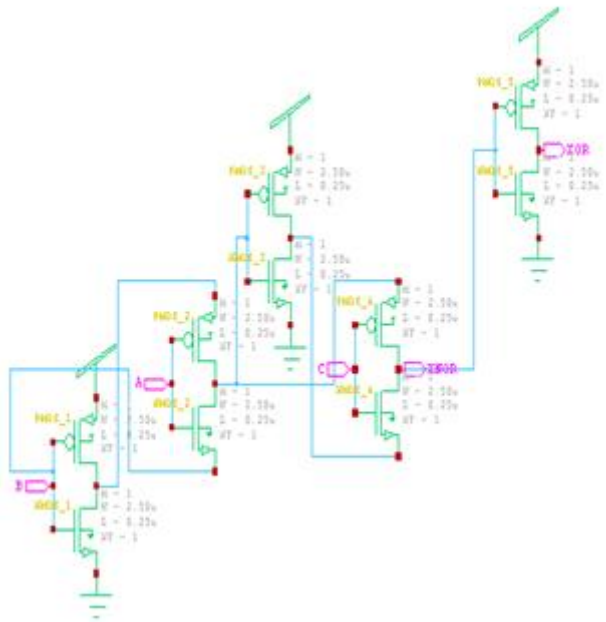

Fig6: Three Input XOR/XNOR gate design.

4. SIMULATION RESULT ANALYSIS

GDI based XOR-XNOR circuit:

The schematic of Second Proposed circuit was implemented in S-Edit of Tanner EDA tool. This circuit is the extension of existing system circuits. This circuit was GDI based Design which gives the output as three input XOR/XNOR output.

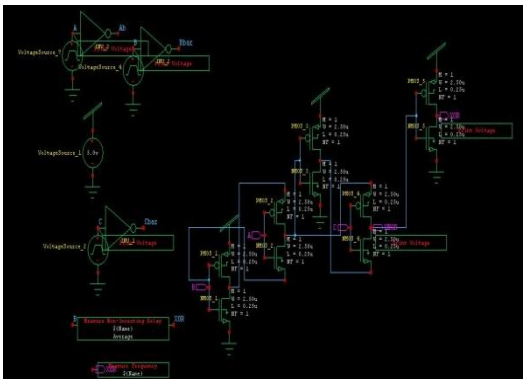

Fig 7: Schematic of GDI based XOR-XNOR Circuit

GDI based XOR-XNOR circuit was designed. It shows some voltage degradation in their output. The below figure shows the GDI based XOR-XNOR circuit simulation waveform with V(A), V(B), V(C) as inputs generates V(XOR) and V(XNOR) as outputs.

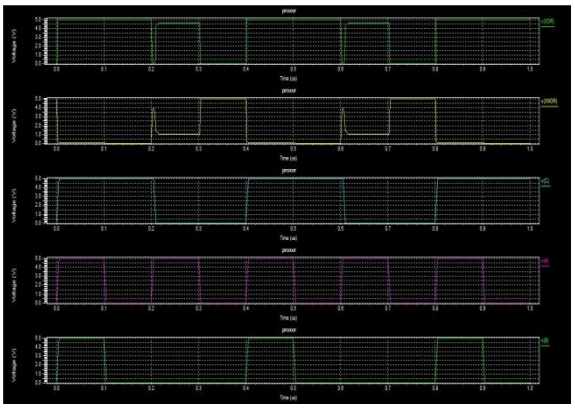

Fig 8: Resultant Waveforms of GDI based XOR-XNOR circuit

Circuits	Average Power	Delay	PDP
XOR4	3.698419e-009w	5.0779e-008	1.8780e-0016
XOR7	9.534406e-003w	1.0022e-007	9.5553e-0010
XOR10	9.601061e-003w	1.0026e-007	9.6259e-0010
Pro XOR	1.167196e-003w	4.8938e-008	5.7115e-0011

5.CONCLUSION

SCDM serves as a design methodology for three-input XOR/XNOR, which is one of the most complex and competitive as well as all-purpose three-input basic gates in arithmetic circuits. The methodology puts emphasis on doing all the steps in a completely systematic way. It also enjoys high flexibility in design target, while it follows the same procedure to obtain the state-of-the-art designs. This brief has favored SCDM with the wise selection of the circuit components for the PDP target. In the end, three new high performance three-input XOR/XNOR circuits with less PDP and occupied area are conceived using SCDM. The new circuits enjoy higher driving capability, transistor density, noise immunity with low-voltage operation, and the least probability to produce glitches. As a unique feature, the critical path of the presented designs consists of only two transistors, which causes low propagation delay.

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