ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Design of a Low Power Area Efficient ALU Using Modified GDI Multiplexer

Chetempally Sridhar Goud
M.Tech, ES& VLSI,
Malla Reddy Collage of Engineering.

Dr.K.Srinivasulu, Ph.D
Professor,
Malla Reddy Collage of Engineering.

M.Shiva Kumar, M.Tech
Assistant Professor,
Malla Reddy Collage of Engineering.

ABSTRACT:
Optimization of area, delay and power dissipation is the major issue in low voltage and low power applications. GDI-Gate Diffusion Technology is low power digital combinational design. This technology requires less number of transistors compared to conventional CMOS technology. As the number of transistors reduced, then optimization of area and power is achieved. One of the disadvantages of GDI is poor logic swing, which is overcome by modifying this technique. This paper mainly presents the optimized area and low power 8-bit ALU using Modified Gate Diffusion Input Multiplexer. This technique allows a reduction in area, delay and low power dissipation with full logic swing. Full adder is a basic cell in ALU which is designed using XOR-MUX to have an operation with high-speed and low power. The entire design is done using CADENCE Tool in GPDK 45nm technology. Power and delay comparison between conventional CMOS, GDI and Modified GDI is also presented.

Keywords:
GDI, Modified GDI, CMOS, full wing, ALU, low power, MUX, ALU.

I. INTRODUCTION:

Gates introduced were of the CMOS variety, and this trend continued till the late1960s. The first practical MOS integrated circuits were implemented in PMOS-only logic and were used in applications such as calculators. The second age of the digital integrated circuit revolution was inaugurated with the introduction of the first Microprocessors by Intel in 1972 (the 4004) and 1974(the 8080).These processors were implemented in NMOS-only logic, which has the advantage of higher speed over the PMOS logic. Simultaneously, MOS technology enabled the realization of the first high density semiconductor memories. In the late 1970s, NMOS-only logic started to suffer from the same plague that made high-density bipolar logic unattractive or infeasible: power consumption. This is where we still are today. Interestingly enough, power consumption concerns are rapidly becoming dominant in CMOS design. CMOS technologyal so playing a vital role in present revolution in information technology.

Motivation:

IC technology has evolved in the 1960s when Gordon Moore, then with Fair-child Corporation and later cofounder of Intel, predicted that the number of transistors that can be integrated on a single die would grow exponentially with time (this prediction, later called Moore's law) from the integration of a few transistors referred to as Small Scale Integration (SSI) the integration of millions of transistors in Very Large scale Integration (VLSI) chips currently in use. Early ICs were simple and only had a couple of gates or a flip-flop. Some ICs were simply a single transistor, along with a resistor network, performing a logic function. Ina period of four decades there have been four generations of ICs with the number of transistors on a single chip growing from a few over million.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

II. EXISTING DESIGN:

While taking account of full adder the sum and carry outputs are represented as the following two combinational Boolean functions of the three input variables A, B and C.

Sum =A xor B xor C -------eqn.1
Carry = AB + AC + BC -------eqn.2

Accordingly the functions can be represented by CMOS logic as follows in fig.1.GDI technique based full adder have advantages over full adder using pass transistor logic or CMOS logic and is categorized by tremendous speed and low power. The technique has been described below.

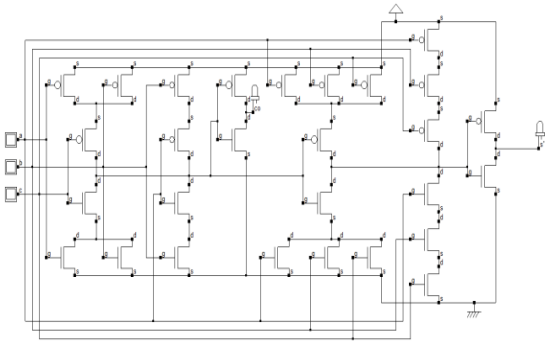

Figure1: Conventional 28-T CMOS 1 bit full adder

III. GATE DIFFUSION INPUT (GDI)

The GDI technique offers realization of extensive variety of logic functions using simple two transistor based circuit arrangement. This scheme is appropriate for fast and lowpower circuit design, which reduces number of MOS transistors as compared to CMOS and other existing low power techniques, while the logic level swing and static power dissipation improves. It also allows easy top- down approach by means of small cell library [5]. The basic cell of GDI is shown in Fig.2.

1) The GDI cell consists of one nMOS and one pMOS. Though in case of GDI both the sources and corresponding substrate terminals of transistors are not connected with supply and it can be randomly biased.

2) It has three input terminals: G (nMOS and pMOS shorted gate input), P (pMOS source input), and N (nMOS source input). The output is taken from D (nMOS and pMOS shorted drain terminal) [11].

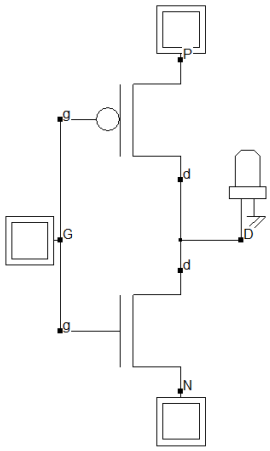

Figure2: GDI basic cell consisting of pMOS and nMOS

GDI logic style approach consumes less silicon area compared to other logic styles as it consists of less transistor count. In view of the fact that, the area is less, the value of node capacitances will be less and for this reason GDI gates have faster operation which presents that GDI logic style is a power efficient method of design. We can realize different Boolean functions with GDI basic cell. Table I shows how different Boolean functions can be realized by using different input arrangements of the GDI cell.

Table I: GDI logic Functions

N	P	G	OUTPUT	FUNCTION	TRANSISTOR COUNT
0	1	A	A'	Inverter	2
0	B	A	A'B	F1	2
B	1	A	A'+B	F2	2
1	B	A	A+B	OR	2
B	0	A	AB	AND	2
C	B	A	A'B+AC	MUX	2
B'	B	A	A'B+B'A	XOR	4
B	B'	A	AB+A'B'	XNOR	4

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

IV. MODIFIED GATE DIFFUSION INPUT (GDI)

In Fig.3 the substrate terminals (P bulk & N bulk) are permanently tied to VDD and GND. Therefore the advantages of Modified GDI are:

1. The variation in threshold drop is overcome.
2. This configuration provides suitability for fabricating the logic cells in CMOS n-well and p-well process.

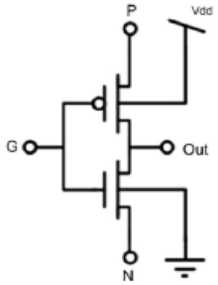

Figure3:Modified GDI

3. Except for inverter, function F1 and F2 remaining logic functions implemented with gate input, which reduces the static power dissipation shown in Table 2.
4. Improves the logic swing adding some more transistors, like NMOS for getting strong logic '0' and PMOS for strong logic '1'.

Table II: Modified GDI logic Functions

Function	G	P	N	Out
OR	A	B	A	A+B
AND	A	A	B	A.B
NAND	A	A'	B	(AB)'
NOR	A	B	A'	(A+B)'
MUX	A	B	C	A'B+AC
XOR	A	B'	B	A'B+AB'
XNOR	A	B	B'	(AB)'+AB

V. ARCHITECTURE OF PROPOSED GDI FULL ADDER:

Multiplexer:

For designing ALU the basic function required is multiplexer to do various logic and arithmetic operations for selected inputs.

In CMOS technology 12 transistors required to implement multiplexer. But using MGDI only six transistors requireddesigning multiplexer as shown Fig.4.

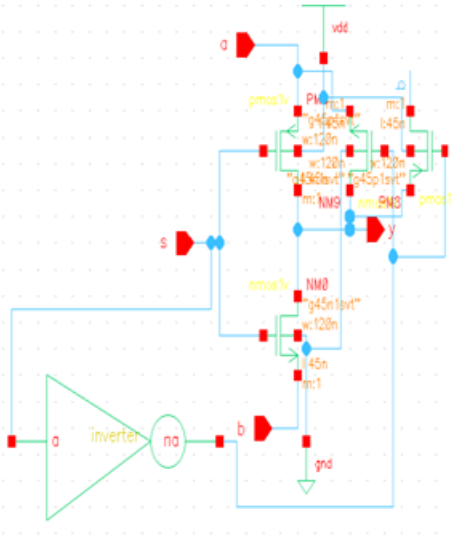

Figure4(a): Schematic of Multiplexer using GDI

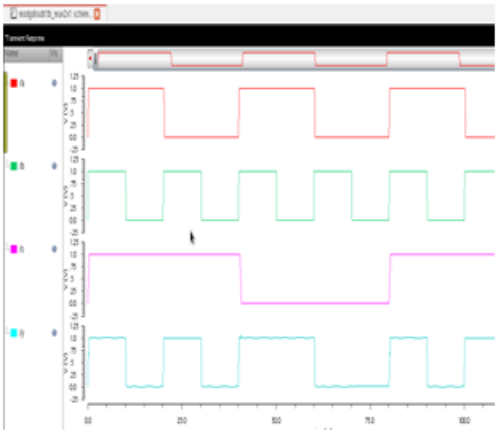

Figure4(b): Simulation of Multiplexer using GDI

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Table III: Average Power of 2x1Multiplexer

Supply voltage	Average Power(n watts)		
	CMOS	GDI	MGDI full swing
0.8	19.9E-9	17.79E-9	13.25E-9
1.0	30.48E-9	17.79E-9	7.677E-9
1.2	50.34E-9	17.79E-9	12.2E-9

Full adder:

Full adder is a combinational circuit that performs arithmetic sum of three bits. It consists of three inputs and two outputs-sum and carry. Fig.5 shows logic diagram of full adder. Boolean expression for sum and carry is given by,

Sum=A xor B xorCin

Carry=AB+BCin+Acin

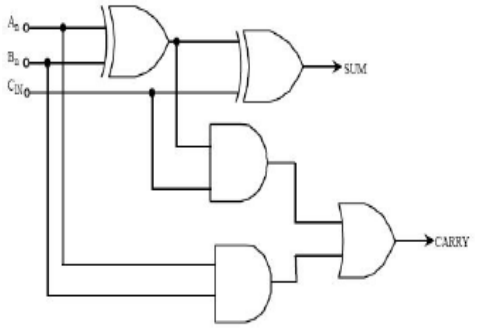

Figure5: Logic level diagram for full adder

In the existing method using 14 transistors full adder full swing in the sum output is achieved but in carry out again there is degraded output due to 2 transistors GDI multiplexer. As carry output of full adder is also plays important role for overflow detection during arithmetic operations, 6 transistors multiplexer is designed such that output should be full logic swing. Full adder using XOR is shown in Fig.5 and itssimulation result using 14 transistors is shown in fig.6. Since Full adder is a basic circuit in ALU for arithmetic operations, it is implemented with a total of 18 transistors using modified GDI multiplexer. Fig.7 shows simulated output of 18 transistor full adder.

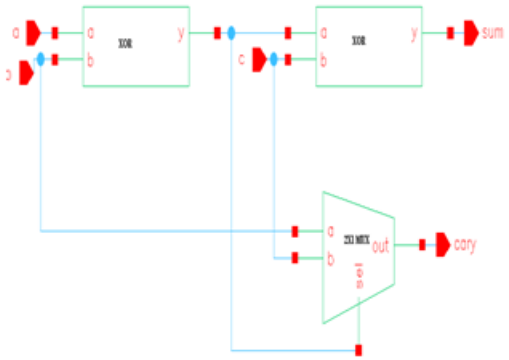

Figure6: XOR-MUX based Full adder

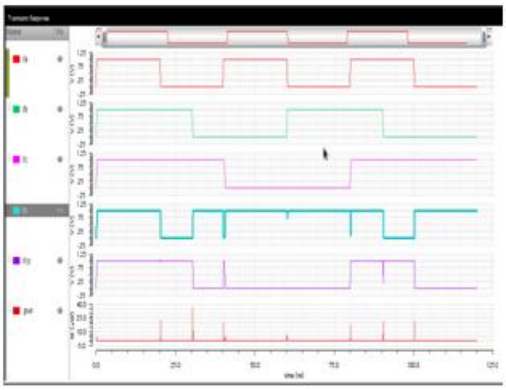

Figure7: Simulation of Modified GDI full adder (18Tr)

The average power of this 18 transistor full adder is less compared to conventional 28 transistor CMOS and GDI full adder as shown in table 1.and table 2 both 45nm technology.

Table IV: Performance of Full Adder in 45nm Technology

45nm	CMOS [28Tr]	GDI[10Tr]	Modified GDI [18Tr]
Avg pwr (watts)	70.23E-9	1.849E-6	49.52E-9
Delay (sec)	85.5E-12	13.22E-12	36.05E-12

Average power dissipation with respect to 45 nm technology for various supply voltages is shown in Table.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Table V: Average power dissipation for various supply voltages

Supply Voltage (V)	Power (Watts)
	45nm
0.8	668.2E-9
1	942.9E-9
1.2	1.093E-6

Schematic Design of 4–bit ALU:

The schematic of arithmetic and logic unit is drawn using a schematic editor i.e., **Virtuoso Composer Schematic**. It describes the transistor level or higher abstraction levels of the circuit. It also can be drawn connectivity between the components and describes aspect ratios of the transistor can be modified along with the design. The fig.8 represent the complete schematics view of ALU. This consists of all the building blocks of ALU.

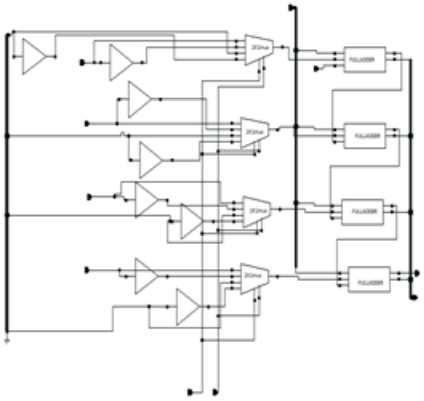

Figure8:Schematic of 4-bit ALU

Simulation Results of 4–Bit ALU:

It consists of four outputs and one carryout(out0, out1, out2, out3,cout) and two –bit inputs(a0,a1,a2,a3,b0,b1,b2,b3) and three selection lines (s0,s1,s2) depend son selection line (s2) either arithmetic or logical will be performed.

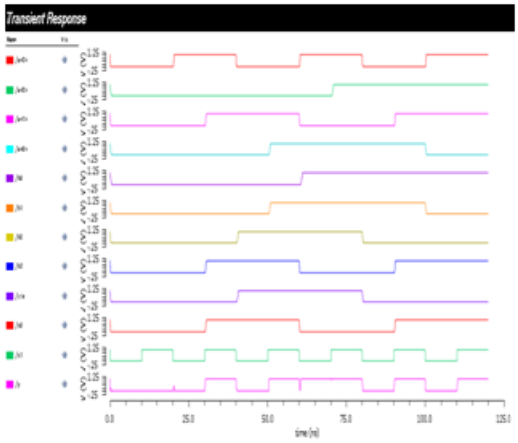

Figure9: Simulation results of 4–bit ALU

Table VI: Function Table of 4– Bit Arithmetic Circuit

Select Lines			Input	Output	Micro Operation
S_0	S_1	C_{in}	Y	D = A + Y + Cin	
0	0	0	B	D = A+ B	Add
0	0	1	B	D = A+ B +1	Add with carry
0	1	0	B'	D = A + B'	Subtract with borrow
0	1	1	B'	D = A + B' + 1	Subtract
1	0	0	0	D = A	Transfer A
1	0	1	0	D = A + 1	Increment A
1	1	0	1	D = A – 1	Decrement A
1	1	1	1	D =A	Transfer A

Design of 8 – Bit Arithmetic Circuit:

The design of low power and high speed embedded systems requires that its sub components like microprocessors, microcontrollers etc. should consumes less power. Arithmetic and logic unit is one of most power consuming device in processor design.The existing methods used different blocks for different operations like arithmetic block, logic block and finally outputs given to multiplexer, which requires more area and more number of transistors, more connections, power and delay. ALU using GDI with multiplexers decreases the power, area, but output is not a full logic swing and also doesn't include shift operations.The above said drawbacks are eliminated with the proposed technique. The proposed ALU is designed using Low power and high speed 4x1 multiplexers and Full adder using Modified GDI Multiplexer.ALU consists of four select signals S3,S2,S1,S0 and one Cin input for different arithmetic operations. Final multiplexer has S2, S3 selection lines to select four different operations of ALU. Fig.10 shows schematic of 8-bit ALU.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Table VI shows functional table of operations performed by ALU. Compared to CMOS and GDI, Modified GDI technique is low power and high speed. Simulation results are shown in Figure 10. The power calculations of GDI ALU and Modified GDI ALU in 90nm and 45nm are shown in Table IV. CMOS power will be more compared to GDI and Modified GDI as number of transistors is more.

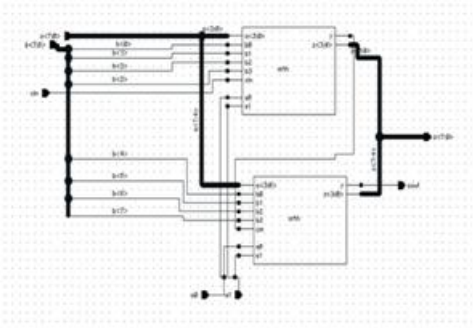

Figure10: 8- bit arithmetic circuit

Implementation of Logic Circuit:

The hardware implementation of logic micro operations requires that logic gates be inserted for each bit or pair of bits in the registers to perform the required logic function.Most computers use only 4 gates – AND, OR, XOR and NOT.

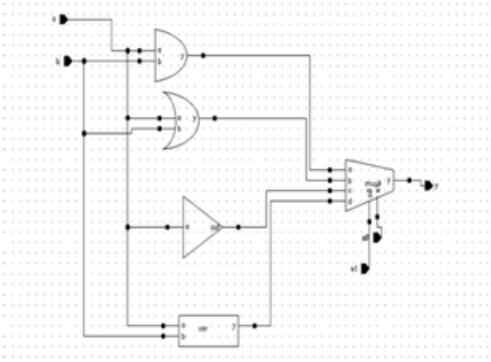

Figure11: Logic Circuit

Design of Shifter:

Shift operations are used for serial transfer of data. They are also used in conjunction with arithmetic, logic and other data-processing operations. In a processor with many registers it is more efficient to implement the shift unit with a combinational circuit rather than sequential.

A combinational circuit shifter can be constructed with multiplexers as shown in Fig.12. The 4-bit logical shifter has four data inputs,A_0 through A_3,and four data outputs Z[0] through Z[3].there are two serial inputs, one for shift left (sl) and other for shift right (sr). The function table for shift operations shown in Table VII. Similarly circular shift operation is implemented. The 4-bit circular shift is shown in Fig.13.

Table VII: Function Table of Shifter:

select	output							
S	Z[7]	Z[6]	Z[5]	Z[4]	Z[3]	Z[2]	Z[1]	Z[0]
Shift left 0	A6	A5	A4	A3	A2	A1	A0	SL
Shift right 1	SR	A7	A6	A5	A4	A3	A2	A1
Rotate left 0	A6	A5	A4	A3	A2	A1	A0	A7
Rotate right 1	A0	A7	A6	A5	A4	A3	A2	A1

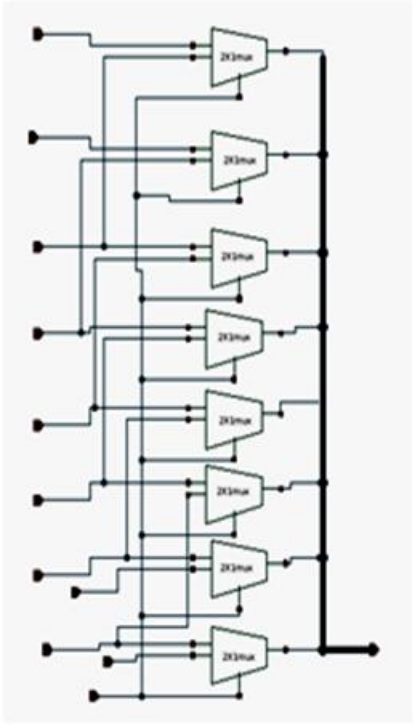

Figure12: 8-Bit Combinational Circuit Logical Shifter

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

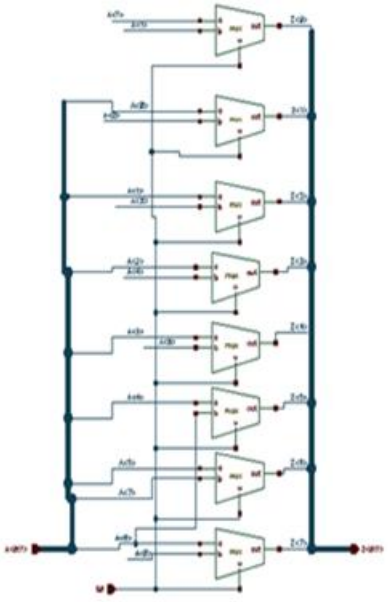

Figure13: 8-Bit Combinational Circular Shift

Schematic of 8-Bit ALU:

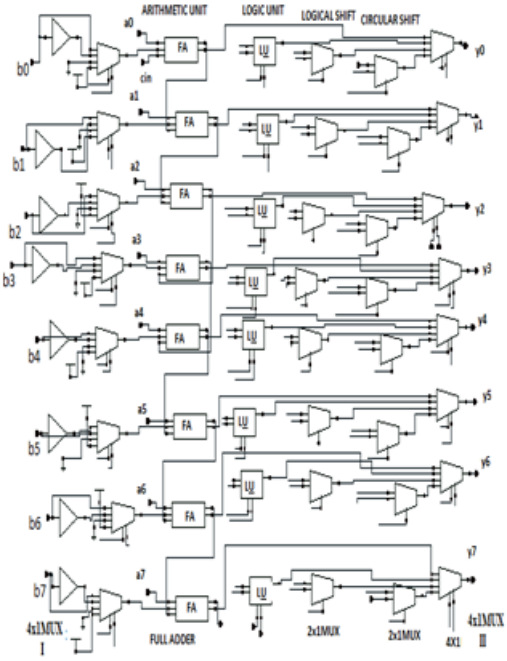

Figure14:Schematic of 8-bit ALU

Test Bench for ALU Using MGDI

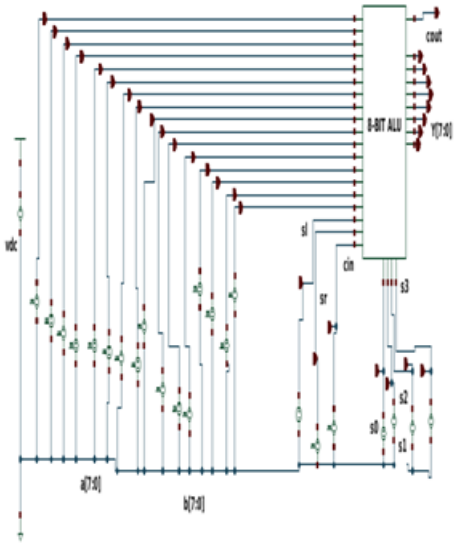

Figure15: Test Bench for ALU

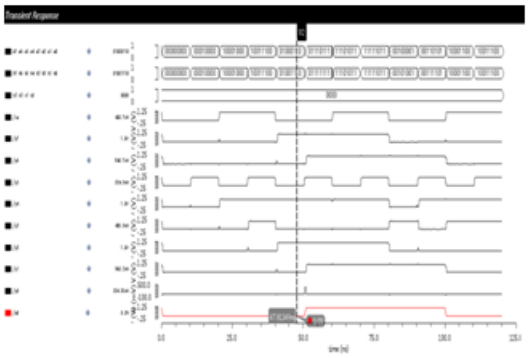

Figure16: Simulation of ALU 8- Bit Addition Operation

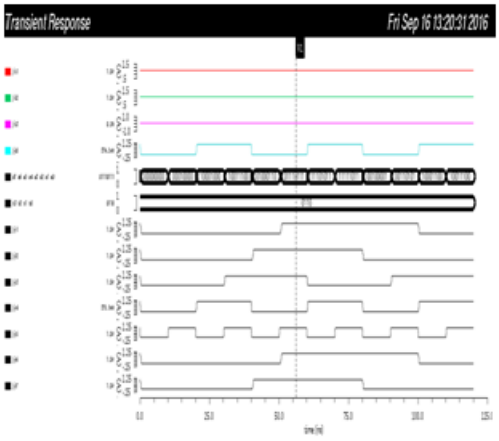

Figure17: Simulation of ALU 8- Bit Shift Rotate

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

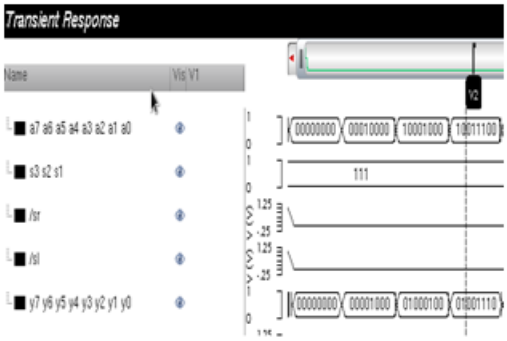

Figure18: Transient Response of 8-Bit ALU for Shift right Operation.

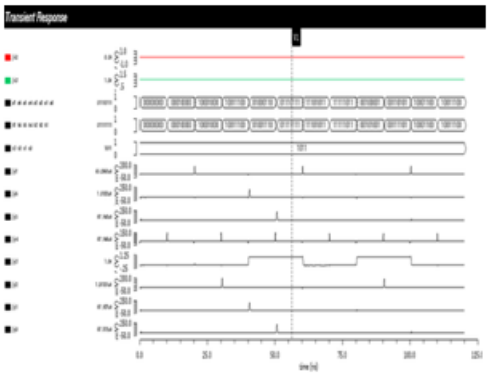

Figure19: Simulation of ALU 8- Bit XOR Operation

Conclusion:

The primary goal of this thesis work is not only to provide an efficient result in low power VLSI design but also shows a successful try in terms of reduction of power dissipation . The basic low power CMOS cell structures as like a two-input AND gate, a two-input OR gate, a two-input XOR gate etc are designed using complementary CMOS logic style and an another effective approach Gate Diffusion Input technique. The high speed, low power and area optimized 8-bit ALU is designed using Modified Gate Diffusion Input Technique. Compared to CMOS technology the number of transistors was reduced. By this Power consumption, delay and area is reduced. When compared with GDI ALU, the Modified GDI ALU‘s output is full logic swing with reduced power and delay.

Future Scope of Work:

Hence GDI technique can be used to design low power circuits such as digital wrist watches, radio frequency identification (RFID), sensor nodes, Laptops, pacemakers and battery operated devices such as, cellular phones etc. This thesis work is based on combinational circuit design so there is a highly fill place for the sequential circuit design for providing a better design. In low power VLSI design GDI technique has very good scope for future.

REFERENCES:

[1]Deepali Koppad, Sujatha Hiremath Low Power 1-Bit Full Adder Circuit Using Modified Gate Diffusion Input (GDI) conference on First International micro and nano technologies.

[2] R.uma and P.Davachelvan low power and High Speed Adders in Modified gate Diffusion Input Technique Computer Networks & Communications (NetCom).

[3]T. Esther Rani, M. Asha Rani, Dr.Rameshwarrao, Area Optimized Low Power Arithmetic And Logic Unit”978-1- 4244-8679-3/11/$26.00 ©2011 IEEE.

[4]D.Anitha,K.Manjunatha Chari,(2014,October) Low Power ALU Design Considering PVT variations. International Journal for Computer Applications-Volume-104-No 17.

[5]M.Kamaraju K.Lal Kishore A.V.N.Tilak (2010 Dec) Power Optimized ALU for Efficient Datapath International Journals for Computer Applications-Volume-11-No 11.

[6]S.Swetha (2016,july) Design of Low Power and Area Efficient Full Adder using Modified Gate Diffusion Input. International Journal for Computer Applications-Volume-145-No 8.

[7]Morris Mano” Register Transfer and Micro operations” Computer System Architecture. Pearson Education.