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The Voltage Injected By DVR Control with SRF Theory for Unsymmetrical Loads

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Abstract:
At present, a wide range of very flexible controllers, which capitalize on newly available power electronics components, are emerging for custom power applications. Among these, the distribution static compensator (D-STATCOM) and the dynamic voltage restorer (DVR) are most effective devices, both of them based on the VSC principle. MATLAB SIMULINK has been used in this project to perform the modeling and analysis of such controllers. A DVR injects a voltage in series with the system voltage to correct the voltage sag. The steady state performance of DVR is obtained for various voltage sags/swell levels. Comprehensive results are presented to assess the performance of each device as a potential custom power solution.

Key Words: ***Power Quality, DSTATCOM, DVR, Voltage Sag, Voltage Swell.***

INTRODUCTION

A DVR is used to compensate the supply voltage disturbances such as sag and swell. The DVR is connected between the supply and sensitive loads, so that it can inject a voltage of required magnitude and frequency in the distribution feeder. The DVR is operated such that the load voltage magnitude is regulated to a constant magnitude, while the average real power absorbed/ supplied by it is zero in the steady state. The capacitor supported DVR is widely addressed in the literature. The instantaneous reactive power theory (IRPT), sliding mode controller, instantaneous symmetrical components etc., are discussed in the literature for the control of DVR. In this project a new control algorithm is proposed based on the current mode control and proportional-integral (PI) controllers for the control of DVR. The extensive simulation is performed to demonstrate its capability, using the MATLAB with its Simulink and Power System Blockset (PSB) toolboxes.

A DVR is a voltage-source converter (VSC)-based powerelectronics device connected in series between the supply andthe critical loads, which are to be protected from the supplysidevoltage quality problems, other than outages, by injectingthe required compensating voltage through DVR into the distributionline. A DVR can restore a balanced sinusoidal loadvoltage of desired amplitude even when the source voltageis unbalanced and/or distorted. The voltage injected by self-supportedDVR is in quadrature with the feeder current; hence,it does not need any active power during steady state. However,its disadvantage is that, in case of the voltage sag/swell, therestored voltage may not be in phase with the presag/preswellvoltage. The self-supported DVR is used when the phase jump, caused by the quadrature voltage injection, is affordable.

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TheDVR supported by a capacitor has become popular as a costeffectivesolution for the protection of sensitive loads from thesupply-side voltage quality problems. Currently, most of theresearch is on DVR dealing with the protection of balancedlinear load; however, there are a few which are related to theprotection of unbalanced and nonlinear loads. The approach discussed here is comparatively simple as it needsonly the extraction of the fundamental positive-sequence phaseterminal voltages, thus making it computationally simpler withthe least memory requirement. The proposed fundamentalpositive-sequence extractor requires the sensing of only twoline voltages of supply. This reduces the analog-to-digital converter(ADC) requirements of a digital controller and correspondingsensing element. Moreover, it is able to extract threefundamental positive-sequence phase voltages irrespective ofthe distribution system configuration such as three-phase, four-wireor three-phase, three-wire system where the neutral is notavailable for sensing phase voltages.

STRUCTURE OF PROPOSED DVR

The power circuit of DVR is discussed. Practically, theDVR is realized by three single-phase H-bridge VSCs alongwith a common dc capacitor (Cdc) as shown in Fig. 1.The three H-bridge VSCs are connected to each phase ofthe distribution feeder through the improved structure ripplefilter (Lr, Cr,Rr) and an injection transformer. The injectiontransformer not only reduces the voltage requirement of theconverter but also provides isolation between the converter andthe distribution feeder. The shunt capacitor filter Cf is used toprovide a low impedance path to higher order harmonics of loadcurrents when the load current is nonlinear. The operation ofpractical DVR with nonlinear load current is discussed in thenext section.

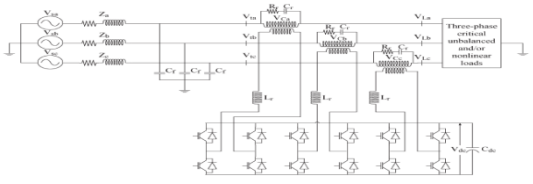

Fig 1: DVR structure

To track the reference compensating voltages, an improvedfilter structure constant switching frequency hysteresis band controller is used in this work. The main advantages ofthe band controller are unconditional stability, faster responseand easy implementation compared to other controllers likecarrier-based controllers, dead-beat control, state feedback control, combined feedforward and feedback control,etc., which are based on complex mathematical computationsand need much information about system parameters. Despitethese advantages, the main disadvantage of the band controllercompared to carrier-based controllers is variable switchingfrequency which may cause stress in the switches of the VSC,resulting in the deterioration of its life. The band controllerhas other drawbacks also like poor controllability, heavy filtercurrents, parabolic band voltage response, and frequent bandviolations due to the use of a conventional LC filter which hasa second-order characteristic equation.

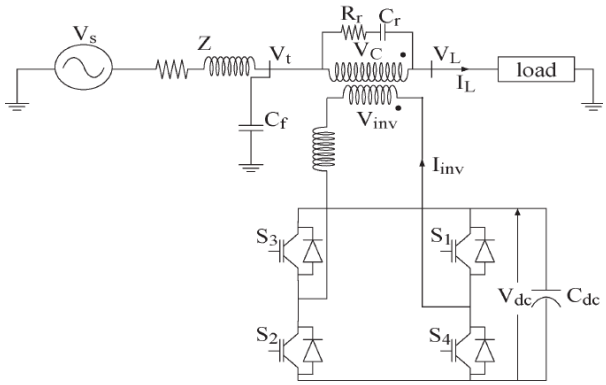

Fig 2: Single-phase circuit of DVR

The single-phase equivalent circuit of the DVR-connected system in Fig. 1 is shown in Fig. 6 to explain the basic principleof the hysteresis band controller. The reference compensatingvoltage for the DVR is calculated using the proposed algorithm.To inject this voltage in series with the distribution feeder,appropriate switching pulses for VSC are generated using thehysteresis band controller with hysteresis band h. When the DVR voltage VC goes below the lower boundary, thepositive dc voltage is applied across the ac filter combination(Cr,Rr) by

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turning switches S1 and S2 on. If DVR voltageVC goes above the upper boundary, the negative dc voltage isapplied by turning switches S3 and S4 on.

In order to improve the performance of the controller, anextra resistance Rr is connected in series with ac filter capacitor Cr as shown in Fig. 2. This resistance dominates the capacitivereactance at switching frequency. At switching frequency, theresistance Rr and combined inductive reactance of the Lr andtransformer are very large compared to the capacitive reactanceof Cr. Thus, at switching frequency, this improved structurefilter circuit behaves as an R−L circuit and gives a linear voltagevariation within the band compared to the parabolic voltagevariation given by the conventional L−C filter circuit. Becauseof the linear response, this filter has less band violations and,hence, better controllability compared to the conventional filter.

CONTROL SYSTEM

The schematicdiagram of DVR (ideal voltage sources) connected distributionfeeder is shown in Fig. 1. A three-phase supply is representedby the star-connected three single-phase voltage sources(Vsa, Vsb, Vsc) along with their series source impedances(Za, Zb, Zc). To regulate the load voltages (VLa, VLb, VLc) tobe balanced and sinusoidal against various PQ problems inthe terminal voltages (Vta, Vtb, Vtc), DVR injects the requiredcompensating voltages (VCa, VCb, VCc) in each phase.The practical implementation of a DVR using three singlephaseH-bridge VSCs along with a common dc capacitor isdiscussed later.

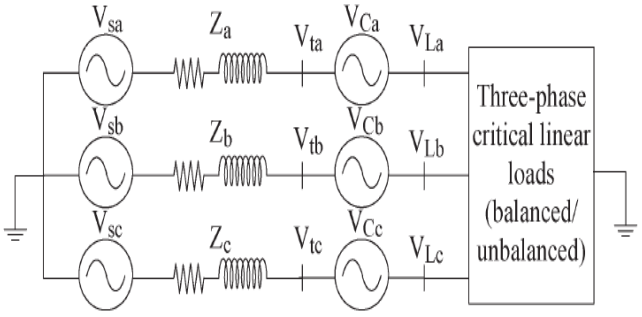

Fig 3: Schematic diagram of DVR (ideal voltage sources) connected powersystem.

The energy storage device is a capacitor, so thefollowing condition is stipulated on the DVR.

- The DVR should not supply any real power in steady state.This implies that, in steady state, the phase differencebetween instantaneous DVR voltages and instantaneousline currents must be 90◦.

Under Balanced Linear Load

The algorithm is developed to compute instantaneousDVR voltages from the samples of instantaneous terminalvoltages and line currents assuming balanced sinusoidalsupply and balanced load.

Taking the line current as the reference frame, the aboveequation can be converted to SRF as

$$v_{td} + jv_{tq} + jv_{cq} = v^*_{Ld} + jv^*_{Lq}$$

Note that, for zero DVR active power in steady state, VCshould be at 90◦ to the line current vtd can be computed from the instantaneous samplesof terminal voltages as

$$v_{td} = v_{ta}\sin\theta + v_{tb}\sin\left(\theta - \frac{2\pi}{3}\right) + v_{tc}\sin\left(\theta + \frac{2\pi}{3}\right)$$

As terminal voltages are balance and sinusoidal, vtd containsonly the constant dc component

$$v^*_{Ld} = v_{td}$$

Moreover, to regulate the peak of the load voltage (ph-n) tovLp, v*Lq can be directly calculated as

$$v^*_{Lq} = \sqrt{v^2_{Lp} - v^{*2}_{Ld}}$$

$$= \sqrt{v^2_{Lp} - v^2_{td}}.$$

After computing v*Ld and v*Lq, the instantaneous referenceload voltages can be computed as follows

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$$\begin{bmatrix} v_{La}^* \\ v_{Lb}^* \\ v_{Lc}^* \end{bmatrix} = \begin{bmatrix} \sin\theta & \cos\theta \\ \sin\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta - \frac{2\pi}{3}\right) \\ \sin\left(\theta + \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \begin{bmatrix} v_{Ld}^* \\ v_{Lq}^* \end{bmatrix}$$

Under Unbalanced Linear Load

The algorithm discussed in the previous section will fail tocompute the desired reference load voltages under the situation,where the unbalanced and/or distorted supply voltages feedthe unbalanced load.

The unbalanced and/or distorted terminal voltages can bewritten as

$$v_{tk} = v_{tk1\_f} + v_{tk\_rest}; \quad k = a, b, c$$

Where vtk1_f is the positive-sequence component of vtk andvtk_rest is the remaining portion containing the influence of unbalanceand harmonics. The modification is thus to replace vta,vtb, and vtc in (3) by vta1_f , vtb1_f , and vtc1_f , respectively

$$v_{td} = v_{ta1\_f}\sin\theta + v_{tb1\_f}\sin\left(\theta - \frac{2\pi}{3}\right) + v_{tc1\_f}\sin\left(\theta + \frac{2\pi}{3}\right)$$

To extract the fundamental positive-sequence terminal phasevoltages, a novel fundamental positive-sequence extractor isproposed which requires the sensing of only two distortedand/or unbalanced terminal line voltages.

Fundamental Positive-Sequence Extractor

As the line voltages are the difference of different phasevoltages (va−vb, vb−vc, and vc−va), the summation of threeline voltages is always zero irrespective of whether three phasevoltages are balanced and sinusoidal or unbalanced. Therefore,by sensing only two line voltages vab and vbc, the third linevoltage vca can be calculated asvca = −(vab + vbc).

If Park's transformation is applied to three balanced sinusoidalline voltages vab, vbc, and vca using a PLL over the sameline voltages, then it gives constant direct-axis component vdequal to the amplitude of line voltage, quadrature-axis componentvq equal to zero, and zero-sequence component v0 equal tozero because line voltages are a positive sequence only without any harmonics.

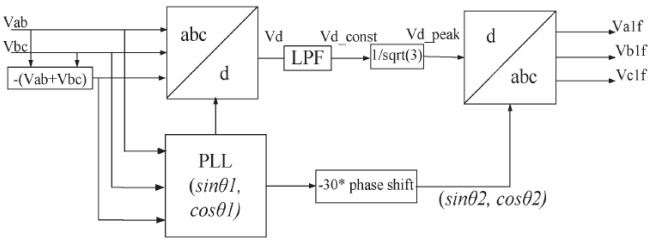

Fig 4: Block diagram of fundamental positive-sequence extractor

When line voltages are unbalanced and/or distorted,then, vd is composed of two parts: a constant componentequal to the amplitude of positive-sequence line voltage and avarying component influenced by negative-sequence line voltageand harmonics.While vq and v0 are not of interest because,here, the aim is to extract fundamental positive-sequence linevoltages and both vq and v0 do not contain any informationabout positive-sequence line voltages, note that v0 is alwayszero when Park's transformation is applied to the line voltages.

SIMULATION RESULTS

Voltage Sag

The proposed control scheme of DVR is verified through simulation using MATLAB software along with its Simulink and Power System Blockset (PSB) toolboxes. The DVR is tested under different operating conditions like sag (Fig 5) and swell (Fig. 6) at the terminal voltages (Vta, Vtb, Vtc). In Fig. 5, the terminal voltage has a sag of 30% with a magnitude at 70% of rated value at 0.22 sec and occurs up to 0.32 sec.

The DVR injects fundamental voltage (Vc) in series with the terminal voltages (Vla, Vlb, Vlc). The load voltage is maintained at the rated value. The terminal voltage (Vt), supply current (is), amplitude of terminal voltage (Vt) the amplitude of load voltage (VL) and the dc bus voltage (Vdc) of DVR are also shown in the Fig.5. It is observed that the dc bus voltage of DVR is maintained at reference value.

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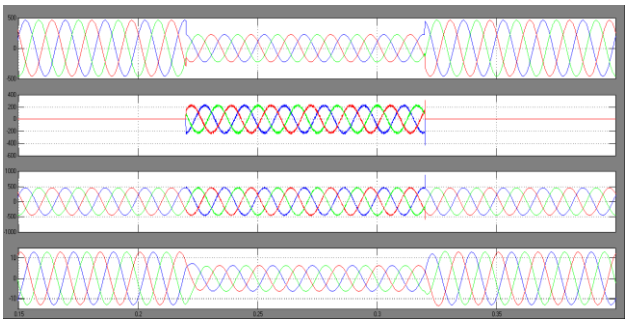

Fig 5: Dynamic behavior of DVR for voltage sag compensation

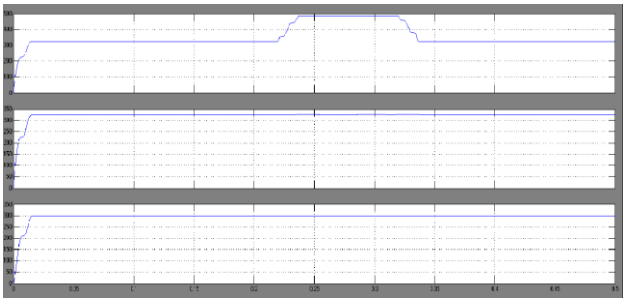

Fig 6: RMS Values of Voltage Sag Compensation

Voltage Swell

Similarly, in Fig.7, a swell in terminal voltage (Vt) has occurred at 0.22 sec up to 0.32 sec and the load voltage (VL) is observed to be satisfactory due to the proper voltage injection by the DVR. The load voltage (VL) is maintained at the rated value. The terminal voltage (Vt) supply current (Is), the amplitude of terminal voltage (Vt), the amplitude of the load voltage (VL) and the dc bus voltage (Vdc) of DVR are also shown in the Fig.6.2. It is observed that the dc bus voltage of DVR is maintained at reference value, though perturbation is occurring during transients.

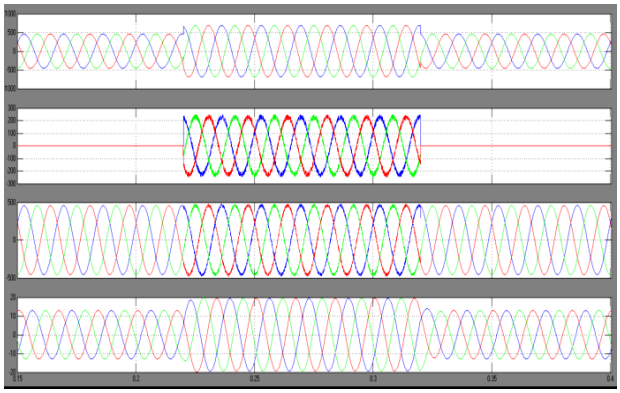

Fig 7: Dynamic behavior of DVR for voltage swells compensation

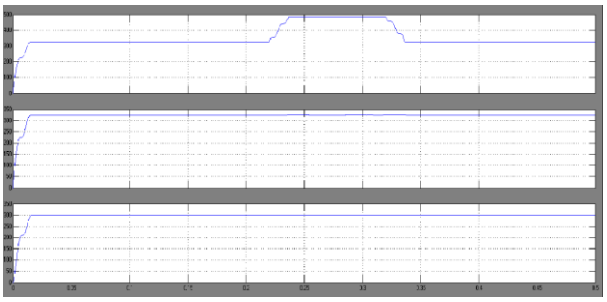

Fig 8: RMS Values of Voltage Swell Compensation

CONCLUSION

A new control strategy based on current mode control for Dynamic Voltage Restorer (DVR) has been proposed to mitigate the power quality problems in the terminal voltages. The DVR is controlled indirectly by controlling the supply current. The reference supply currents are estimated using the sensed load terminal voltages and the dc bus voltage of DVR. The control scheme is based on synchronous reference frame theory (SRFT) for the operation of a capacitor supported DVR. The proposed control scheme of DVR has been validated the compensation of sag and swell in terminal voltages. The performance of the DVR has been found very good to mitigate the voltage power quality problems. Moreover, it has been found capable to provide self-supported dc bus of the DVR through power transfer from ac line at fundamental frequency.

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