A 32 BIT MAC Unit Design Using Vedic Multiplier and Reversible Logic Gate

K.Kotiratnam
M.Tech Student
Ellenki Institute of Engineering and Technology.

B.Ramu, M.Tech
Assistant Professor
Ellenki Institute of Engineering and Technology.

ABSTRACT:

The Vedic Multiplier and the Reversible Logic Gates has Designed and implemented in the multiply and Accumulate Unit (MAC) and that is shown in this paper. A Vedic multiplier is designed by using Urdhava Triyagbhayam sutra and the adder design is done by using reversible logic gate. Reversible logics are also the fundamental requirement for the emerging field of Quantum computing. The Vedic multiplier is used for the multiplication unit so as to reduce partial products and to get high performance and lesser area .The reversible logic is used to get less power. The MAC is designed in Verilog HDL and the simulation is done in Xilinx 14.2 and synthesis is done using Xilinx. The chip design for the proposed MAC is also carried out.

Keywords: Reversible Logic, Urdhava Triyagbhayam, Quantum Computing, Kogge Stone Adder

I.INTRODUCTION:

In the accumulate adder the previous MAC output and the present output will added and it consists of Multiplier unit, one adder unit and both will get be combined by an accumulate unit. The major applications of Multiply-Accumulate (MAC) unit are microprocessors, logic units and digital signal processors, since it determines the speed of the overall system [13]. The efficient designs by MAC unit are Nonlinear Computation like Discrete Cosine or wavelet Transform (DCT), FFT/IFFT. Since, they are

basically executed by insistent application of multiplication and addition, the entire speed and performance can be compute by the speed of the addition and multiplication taking place in the system.

Generally the delay, mainly critical delay, happens due to the long multiplication process and the propagation delay is observed because of parallel adders in the addition stage. The main idea of this paper is comparison of area, speed and other parameters of Conventional MAC unit with the Vedic MAC design.

II.LITERATURE SURVEY
MAC Unit

A multiplying function can be carried out in three ways: partial product Generation (PPG), partial product addition (PPA), and final conventional addition. The two bottle necks that should be considered are increasing the speed of MAC are partial product reduction and accumulator block. The 32 bit Mac design by using Vedic multiplier and reversible logic gate can be done in two parts. First, multiplier unit, where a conventional multiplier is replaced by Vedic multiplier using Urdhava Triyagbhayam sutra. Multiplication is the fundamental operation of MAC unit [1].

Power consumption, dissipation, area, speed and latency are the major issues in the multiplier unit. So, to avoid them, we go for fast multipliers in various applications of DSP, networking, etc. There are two

major criterion that improve the speed of the MAC units are reducing the partial products and because of that accumulator burden is getting reduced. The basic operational blocks in digital system in which the multiplier determines the critical path and the delay. The (log2N + 1) partial products are produced by 2N-1 cross products of different widths for N*N. The partial products are generated by Urdhava sutra is by Criss Cross Method. The maximum number of bits in partial products will lead to Critical path.

The second part of MAC is Reversible logic gate. In modern VLSI, fast switching of signals leads to more power dissipation. Loss of every bit of information in the computations that are not reversible is kT*log2 joules of heat energy are generated, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. In recent years, reversible logic functions has emerged and played a vital role in several fields such as Optical, Nano, Cryptography, etc.

III.DESIGN OF MAC ARCHITECTURE:

The design of MAC architecture consists of 3 sub designs.

➢ Design of 32×32 bit Vedic multiplier.
➢ Design of adder using DKG gate reversible logic.
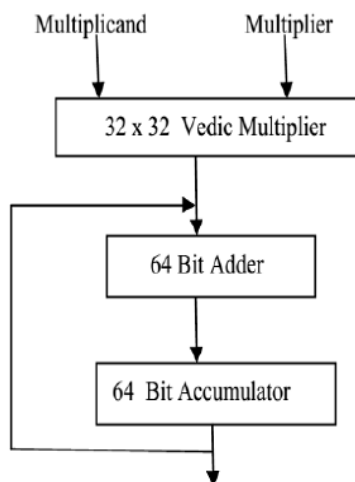➢ Design of accumulator which integrates both multiplier and adder stages.


Fig: Modified MAC Architecture.

A.32 x 32 bit Vedic Multiplier:

Vedic mathematics is an ancient system of mathematics, which was formulated by Sri Jagadguru Swami Bharati Krishna Tirthaji (1884 - 1960). After a research of eight years, he developed sixteen mathematical formulae from AtharvanaVeda[11].

The sutras (aphorisms) covered each and every topic of Mathematics such as Arithmetic, Algebra, Geometry, Trigonometry, differential, integral, etc., The word "Vedic" is derived from the word "Veda" which means the power house of all knowledge and divine [2, 3]. The proposed Vedic multiplier is based on the "Urdhava Triyagbhayam" sutra (algorithm). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we will utilize similar techniques to solve the binary number system to make the new aphorism, which will be more compatible for the digital systems. It is a general multiplication formula applicable to all cases of multiplication.

Urdhava Triyagbhayam Sutra:

It literally means "Vertically and Crosswise". Shift operation is not necessary because the partial product calculation will perform it in a single step, which in turn saves time and Power. This is the main advantage of the Vedic multiplier. An example for the Urdhva Triyagbhayam sutra is as follows:9284 * 5137
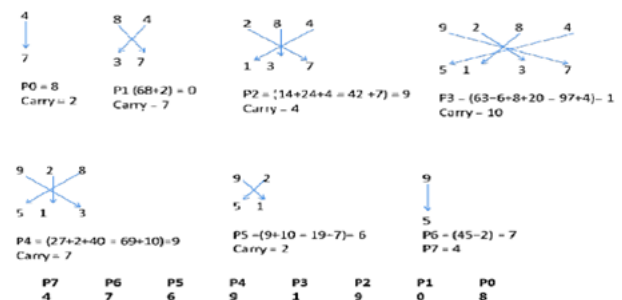

IV.IMPLEMENTATION OF VEDIC MULTIPLIER USING MODEL ARCHITECTURE IN DESIGN:

The following fig. 2 shows the design of a 16×16 Vedic multiplier using an 8×8 Vedic multiplier and the

design can be implemented using Verilog HDL. Using a 16×16 Vedicmultiplier we can design 32 ×32 Vedic multiplier with carry save adder as shown in fig. We have modified the final adder stage with the Kogge stone adder which is more efficient than the Carry save adder which is shown in the fig.

By using the Vedic multiplier we can achieve lesser partial products as the table shows that the multiplier and adder stages for Vedic multiplier for higher bit are lesser as compared to the conventional multiplier.The multiplier design has been simulated and synthesizedusing Xilinx.
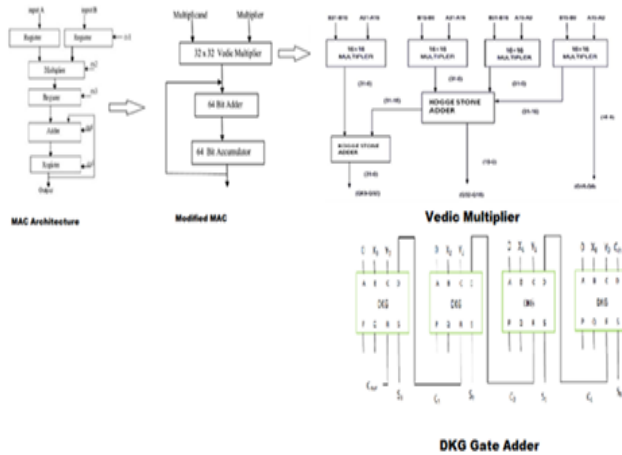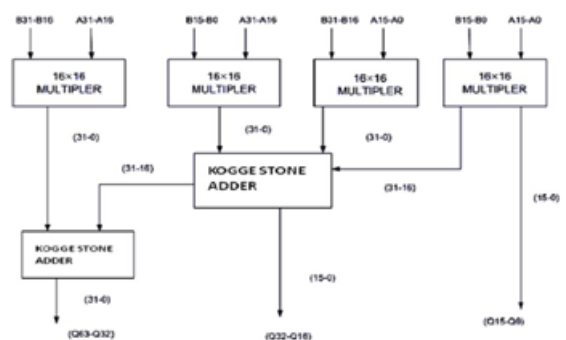

Fig. Block diagram of 32 bit MAC using vedic multiplier and reversible logic gate
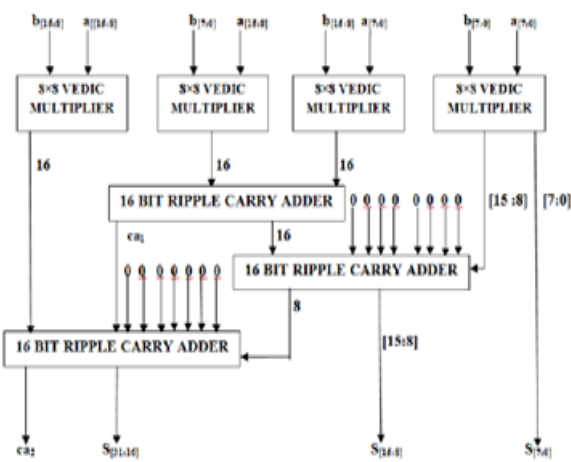
**Fig : 16×16 Vedic multiplier using 8×8 Vedic multiplier**
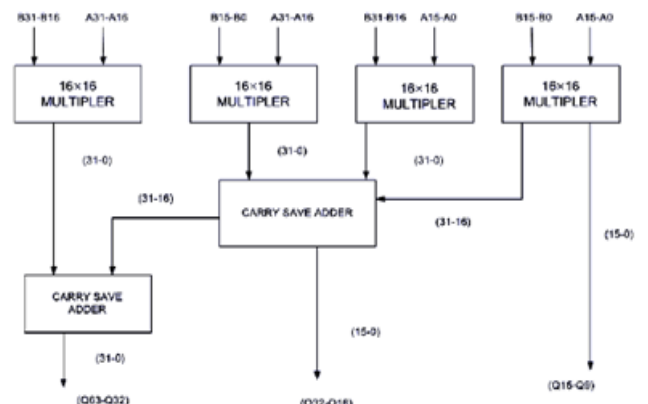
Fig : 32 × 32 Vedic Multiplier with Carry save Adder

Fig: 32 × 32 Vedic Multiplier with Kogge Stone Adder

IV.KOGGE STONE ADDER:

It's a parallel prefix adder, which is the one of the fastest adder. Carry stages: $\log 2\ n$; The number of cells: $n(\log 2\ n-1)+1$; Maximum fan-out: 2 (extra wiring). So, it will reduce thepower consumption as well as the power dissipation.
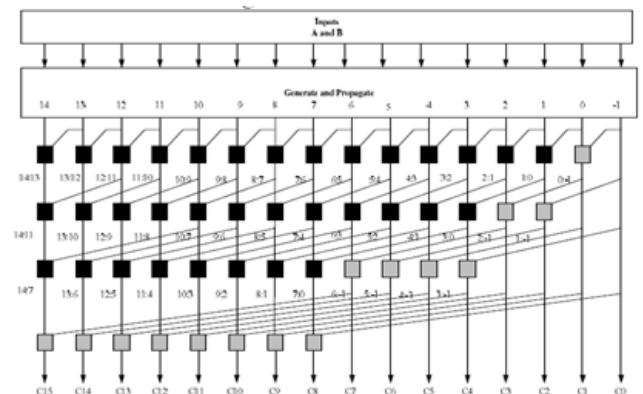
Fig: 16-bit Kogge Stone Adder

VI. DESIGN OF ADDER USING REVERSIBLE LOGIC DKG GATE

Reversible logic

Reversible logic is a unique technique (different from other logic). Loss of information is not possible in here. In this, the numbers of outputs are equal to the number of inputs.

General consideration for reversible logic gate

A Boolean function is reversible if each value in the input set can be mapped with a unique value in the output set. Landauer [18] proved that the usage of traditional irreversible circuits leads to power dissipation and Bennet [17] showed that a circuit consisting of only reversible gates does not dissipate power. In the design of reversible logic circuits, the following points must be kept in mind to achieve an optimized circuit:

Fan-out is not permitted
Loops or feedbacks are not permitted
Garbage outputs must be Minimum
Minimum delay
Minimum quantum cost
Zero energy dissipation [17]

DKG Gate

A 4* 4 reversible DKG gate [6] that can work singly as a reversible full adder and a reversible full subtractor is shown below. If input A=0, the DKG gate works as a reversible Full adder, and if input A=1 then it works as a reversible Full subtractor. It has been verified that a reversible full-adder circuit requires at least two or three garbage outputs to make the output combinations unique [5], [6].
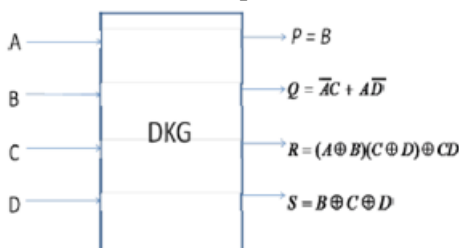
$$P = B$$
$$Q = \overline{A}C + A\overline{D}$$
$$R = (A \oplus B)(C \oplus D) \oplus CD$$
$$S = B \oplus C \oplus D$$

Fig. 6a [6] DKG gate

$$P = A = g1$$
$$Q = B = g2$$
$$R = A(B \oplus C) \oplus BC = carry$$
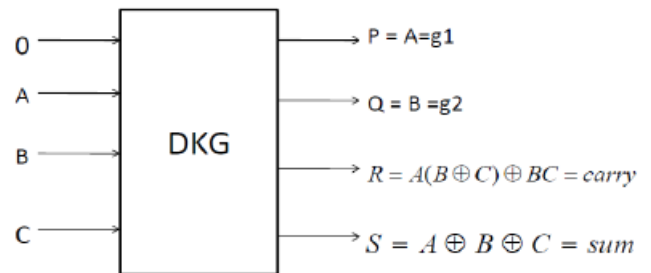$$S = A \oplus B \oplus C = sum$$
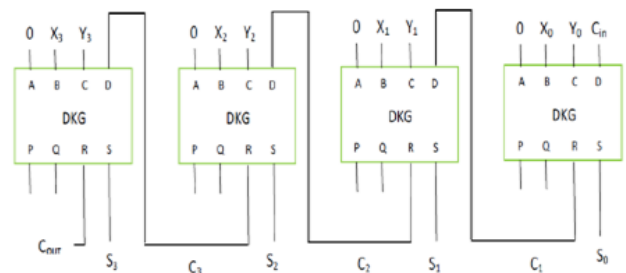
Fig. 6b DKG gate as a Full adder

Fig. 6c Parallel adder using DKG gate

VII. ACCUMULATOR STAGE:

Accumulator has an important role in the DSP applications in various ranges and is a very basic and common method. The register designed in the accumulator is used to add the multiplied numbers. Multiplier, adder and an accumulator are forming the essential foundation for the MAC unit. The conventional MAC unit has a multiplier and multiplicand to do the basic multiplication and some parallel adders to add the partial products generated in the previous step. To get the final multiplication output we add the partial product to these results. Vedic Multiplier has put forward to intensify the action of the MAC Unit. The suggested MAC is compared with the conventional MAC and the results are analyzed. The results obtained using our design had better performance when compared to the pervious MAC designs.

VIII. RESULT AND DISCUSSION:

The modified multiplier using the Kogge Stone Adder is fast and the design of 32 bit MAC is done in Xilinx. All the synthesis and simulation results are performed using Verilog HDL. The synthesis and simulation are

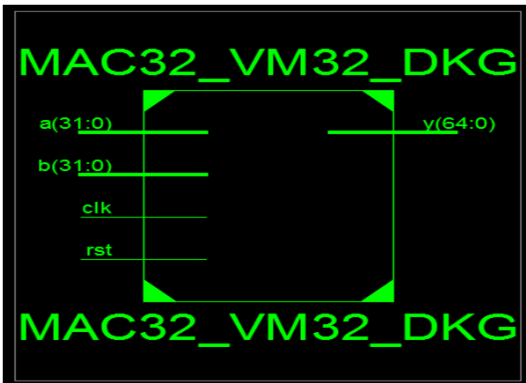performed on Xilinx ISE 14.4. The simulation results are shown below figures.

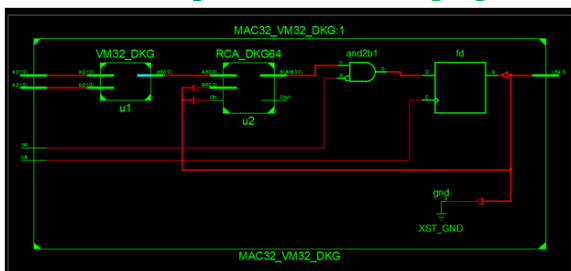**Fig.15: RTL schematic of 32bit-MAC using 32x32 vedic multiplier with DKG Logic gate**

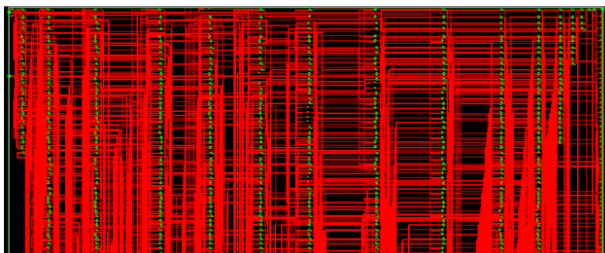**Fig.16: RTL sub schematic of 32bit-MAC using 32x32 vedic multiplier with DKG Logic gate**

Fig.17: Technology schematic of 32bit-MAC using 32x32 vedic multiplier with DKG Logic gate

Fig.18: Design summary of 32bit-MAC using 32x32 vedic multiplier with DKG Logic gate

Fig.19: Simulation of 32bit-MAC using 32x32 vedic multiplier with DKG Logic gate

CONCLUSION AND FUTURE WORK:

The results obtained by the design of Vedic multiplier with 32 bits and reversible logic are quite good. The work presented is based on 32 – bit MAC unit with Vedic Multipliers. We have designed MAC unit basic building blocks and its performance has been analyzed for all the blocks. Therefore, we can say that the Urdhava Triyagbhayam sutra with 32-bit Multiplier and reversible logic is the best in all aspects like speed, delay, area and complexity as compared to other architectures which are shown in table. Many researchers are reconfiguring the structure of MAC unit, which is the basic block in different designs and aspects especially using reversible logic which evolves recent days. Spectrum Analysis and Correlation linear filtering which are the applications of transform algorithm further add to the field of communication, signal and image processing and instrumentation, and some other.

Combining the Vedic and reversible logic will lead to new and efficient achievements in developing various fields of Mathematics, science as well engineering.

References:

[1]Vaijyanath Kunchigi ,Linganagouda Kulkarni, Subhash Kulkarni 32-bit MAC unit design using Vedic multiplier International Journal of Scientific and Research Publications, Volume3, Issue 2, February 2013.

[2]Ramalatha, M.Dayalan, K D Dharani, P Priya, and S Deoborah, High Speed Energy Efficient ALU design

using Vedic multiplication techniques, International Conference on Advances in Computational Tools for Engineering Applications, 2009. ACTEA '09.pp. 600 - 3, Jul 15-17, 2009.

[3]SreeNivas A and Kayalvizhi N. Article: Implementation of Power Efficient Vedic Multiplier. International Journal of Computer Applications 43(16):21-24, April 2012. Published by Foundation of Computer Science, New York, USA.

[4]Vaijyanath Kunchigi, Linganagouda Kulkarni, Subhash Kulkarni, High Speed and Area Efficient Vedic Multiplier, International Conference on Devices, Circuitsand Systems (ICDCS), 2012.

[5]D.P.Vasudevan, P.K.Lala, J.Di and J.P.Parkerson, "Reversiblelogic design with online testability", IEEE Trans. On Instrumentation and Measurement, vol.55., no.2, pp.406-414, April 2006.

[6]Raghava Garipelly ,P.Madhu Kiran , A.Santhosh Kumar A Review on Reversible Logic Gates and their Implementation International Journal of Emerging Technology and Advanced Engineering Website: www.ijetae.com (ISSN 2250-2459, ISO 9001:2008 Certified Journal, Volume 3, Issue 3, March 2013.

[7] Wikipedia.org/ mac design.

[8]Prabir Saha, Arindam Banerjee, Partha Bhattacharyya, Anup Dandapat, High Speed ASIC Design of Complex Multiplier Using Vedic Mathematics, Proceeding of the 2011 IEEE Students' Technology Symposium 14-16 January, 2011, IIT Kharagpur.

[9]Asmita Haveliya, A Novel Design for High Speed Multiplier for Digital Signal Processing Applications (Ancient Indian Vedic mathematics approach), International Journal of Technology and Engineering System (IJTES), Vol.2, No.1, Jan -March, 2011.

[10]Aniruddha Kanhe, Shishir Kumar Das and Ankit Kumar Singh, Design and Implementation of Low Power Multiplier Using Vedic Multiplication Technique, (IJCSC) International Journal of Computer Science and Communication Vol. 3, No. 1, January-June 2012, pp. 131-132 International Journal of Scientific and Research Publications, Volume 3, Issue 2, February 2013 ISSN 2250-315.

[11]www.hinduism.co.za/vedic.htm#Vedic athematics.

[12] www.vedicmaths.org/

[13] A. Abdelgawad, MagdyBayoumi ," High Speed and Area- Efficient Multiply Accumulate (MAC) Unit for Digital Signal Processing Applications", IEEE Int. Symp. Circuits Syst. (2007)3199–3202.

[14] R.Bhaskar, GanapathiHegde, P.R.Vaya," An efficient hardware model for RSA Encryption system using Vedic mathematics", International Conference on Communication Technology and System Design 2011 Procedia Engineering 30 (2012) 124 – 128.

[15] FatemehKashfi, S. Mehdi Fakhraie, Saeed Safari," Designing an ultra-high-speed multiply-accumulate structure", Microelectronics Journal 39 (2008) 1476–1484.

[16]Jagadguru Swami Sri BharatiKrisnaTirthaji Maharaja, "Vedic mathematics", MotilalBanarsidass Publishers Pvt. Ltd, Delhi, 2009.

[17]C.H. Bennett," Logical reversibility of computation", IBM J. Res. Dev. 17 (1973) 525–532.

[18]R. Landauer, Irreversibility and heat generation in the computational process's, IBM J. Res. Dev. 5 (1961) 183–191.

[19]Ashis Kumer Biswas, Md. Mahmudul Hasan, Ahsan Raja Chowdhury, Hafiz Md. HasanBabu, "Efficient approaches for designing reversible Binary Coded Decimal adders".