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Design of Full Adder Circuit using Double Gate MOSFET

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Abstract:
This paper presents a design of a one bit full adder cell based on degenerate pass transistor logic (PTL) using Double Gate MOSFET. The design cell is degenerate 5-T XOR-XNOR module. This design has been compared with existing one-bit full adder cell based on degenerate pass transistor logic (PTL)designed using Single Gate MOSFET. The simulations of the proposed Full Adder have been performed using DSCH3.5 and Microwind3.5. All the proposed design simulations are carried out at 65nm technology. The results show a validity of double gate MOSFETs for designing for low power full adder circuit.

Index Terms:
Full Adder; Pass Transistor Logic; Double Gate; Low Power;

I.INTRODUCTION:

The need of designing low power VLSI circuits has been increased immensely due to increased demand of portable devices like palmtops, cellular and mobiles. Further to integrate more number of devices on chip, scaling of device size is required. But there are number of problems in scaling of bulk MOSFETs. The problems like leakage current, drain induced barrier lowering (DIBL) effect, and other short channel affects (SCE's) degrade the performance of circuits. New device structure is needed which can work with improved performance in nanometer range of operation.

A double gate MOSFET is capable device because it shows better scalability in nano circuits [1]. Double Gate MOSFET (DG MOSFET) is widely used in ultra-low power design. DGMOSFET's has drain, source and two gates. The two gates (front and back) are electrically coupled together in double gate devices. The two gates ensure that no part of the channel is far away from a gate and it has better control over channel conductance and immunity to SCE's and reduces sub threshold leakage. DG-MOSFET can also operate in two modes such as symmetrical driven (SDDG) and independent driven (IDDG) double gate MOSFET [2-3] to design digital and analog circuits. In SDDG mode, the front and back gates are connected together and in IDDG mode, separate biasing are provided to the front and back gates. The Fig. 1(a) shows symbol of double gate MOSFET and Fig. 1(b) shows asymmetrical and asymmetrical mode of operation of double gate MOSFETs.

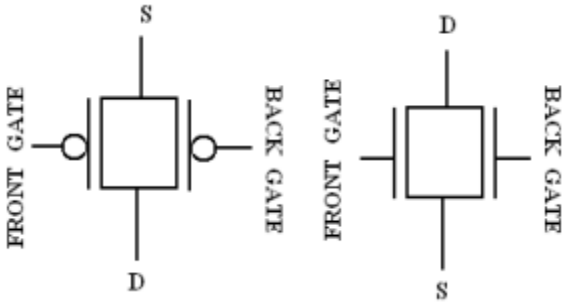

Figure 1(a). Circuit symbols for p-type and n-type DG- MOSFET transistors

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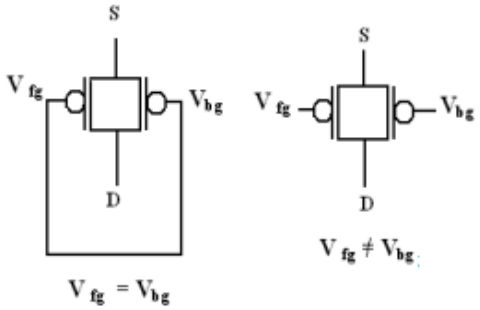

Figure 1(b). Symmetrical and independent driven double gate MOSFETs

The paper is organized into five sections. Section I give the general information for l low power designing and introduce DG-MOSFET device. Section II illustrates the existing single gate based full adder cell as reported in the literature. In, section III full adder cell using DG MOSFET has been proposed. Simulations, results are given in Section IV and finally Section V concludes the paper.

II.DESIGN OF FULL ADDER USING SINGLE GATE MOSFET:

The full adder is basic unit of arithmetic circuits and it is the most necessary building blocks in microprocessors, microcontrollers, ALU's and digital signal processor [4-5]. 1- bit full adder circuit has three inputs and one carry in (Cin). Various full adder circuits has been designed which emphasison low power, less complexity and high speed but there are several problem like degraded outputs and cannot work in ultra low power range. In this paper, high speed and low power DG- MOSFET based full adder is designed using 5-T XOR-XNOR module. Though 5T XOR-XNOR module does not satisfy all inputs, but it is sufficient to function properly in full adder applications. 5-T XOR-XNOR module [6] as given in Fig. 2(a) is designed by removing the weak pull-up transistor at the XNOR output from the 6-T design.

The complementary signal will be used to generate sum and carry outputs. It is supply voltage free, so suitable for low power operations. It also avoids a latch breaking problems of XORXNOR module.

The truth table of XOR-XNOR design is given in Fig. 2(b), in which "0+ " and "1- " indicate degraded signals, i.e. |Vtp| and (Vdd-Vtn), due to threshold voltage loss. In the case of both inputs equal to "0", the XNOR output becomes floating. So this module is considered logically degenerate.

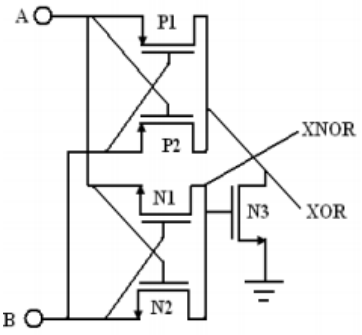

Figure 2(a). XOR-XNOR design using 5 transistors

TABLE.I TRUTH TABLE OF XOR XNOR MODULE

A	B	XOR	XNOR
0	0	0+	X
0	1	1	0
1	0	1	0
1	1	0	1-

TABLE.I illustrates a single gate MOSFET based full adder. The 5T XOR XNOR module is used to design full adder the logical equation of Sum and Cout are given as:

$$Sum = \overline{(A \oplus B)}C + (A \oplus B)\overline{C} \quad (1)$$

$$Cout = (A \oplus B)C + \overline{(A \oplus B)}A \quad (2)$$

The complimentary signal P is used as control signal to realize Sum and Cout outputs with less threshold loss. The sum is observed assum=p⊕c. Logically XOR-XNORmodules, pass transistors P1, P2 and N1, N2 are sufficient to realize the XOR function in the sum module. Because the P (XNOR input) signal could become floating, additional pass transistor P3 is added to tackle the problem. When C is equals "1" and A, B is (0, 0), C is propagated through P3, N4. When C is equal to "0" and A, B is (1, 1) the previous value of XNOR signal is retained which either "1- " or "0". This does not affect the functionality of carry module.

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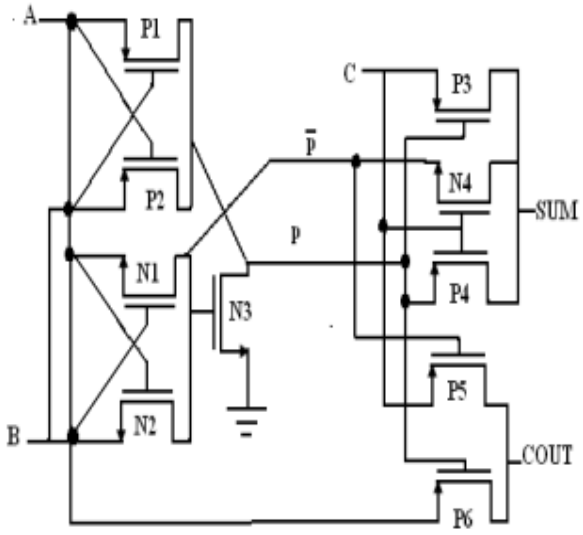

Figure 2(c). Single gate MOSFET based full adder circuit

The carry module uses a 2-to-1 multiplexer (P5, P6) which implements the Boolean expression:

$$Cout = P \oplus C + \overline{P} \oplus A \qquad (3)$$

The multiplexer is realized by two pMOS (P5, P6). Transistor P3 is responsible for the term .AP while transistor P4 implements the term .CP . P3 and P4 now work in parallel to enhance the propagation of signal "0". Although our carry module design has degraded signal "0+ ", but still gives proper logical function of full adder.

III.FULL ADDER CIRCUIT USING DOUBLE GATE MOSFET

DG- MOSFET full adder circuit has been designed using the equivalent style. The full adder circuit using Double gate MOSFET has been shown in Fig. 3(a) DG- MOSFET will be constructed by connecting two single gate MOSFET transistors in parallel in such a way that their source and drain are connected together. The two gates in DG-MOSFETs lead to increased current driving property of transistor. The DGMOSFET structure provides electrostatic coupling for conduction channel and two gates allows additional gate length scaling by factor of 2 as compare to the single gate MOSFET [7-8].

The schematic of single gate MOSFET based full adder is implemented using double gate MOSFET in symmetrical driven mode. There are number of adder circuits have been designed using DG-MOSFETs [9]. The proposed circuit shows better output waveforms at lower input voltages. According to the DG-MOSFET, the chip area of a p-type DG MOSFET and n-type DG MOSFET are same, and the amounts of current related to them can also be the same. The W/L ratios of transistors are taken as 1/1.

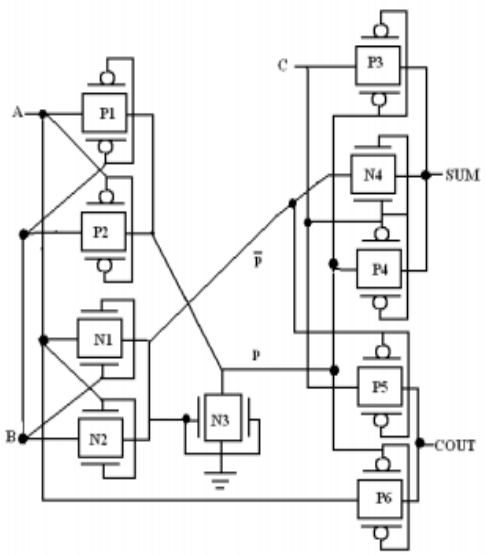

Figure 3(a). Double gate MOSFET based full adder circuit

IV.SIMULATION AND RESULTS:

All the simulations are performed on Microwind3.5 and DSCH3.5. The main focus of this work is to meet all challenges faces in designing of full adder circuit with Double Gate MOSFET in 65nm technology.

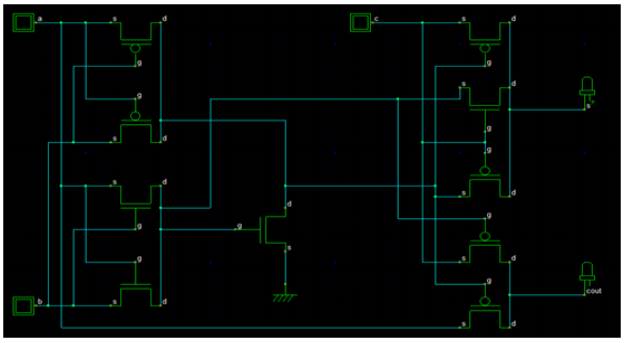

Fig 4: Schematic of single gate MOSFET full adder

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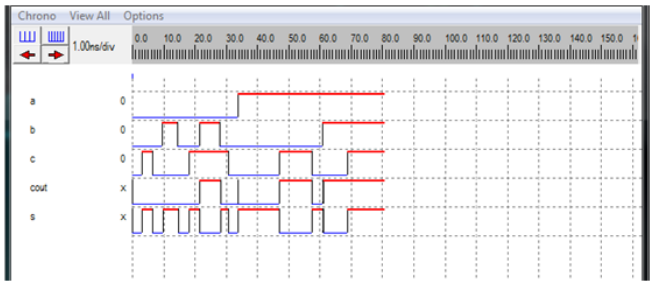

Fig 5: Timing Diagram of single gate MOSFET full adder

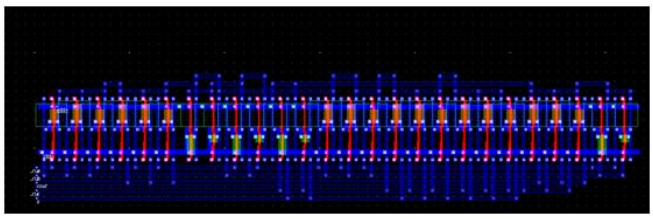

Fig 6: Layout of single gate MOSFET full adder

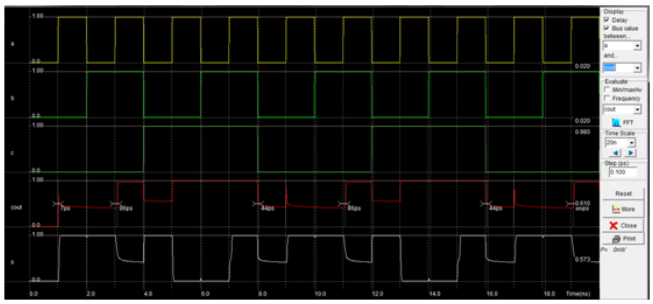

Fig 7 Layout Simulation of single gate MOSFET full adder

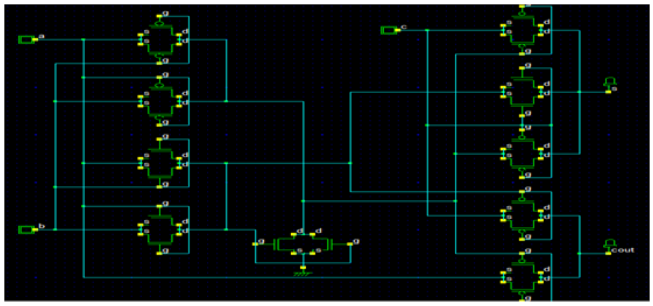

Fig 8: Schematic of Double gate MOSFET full adder

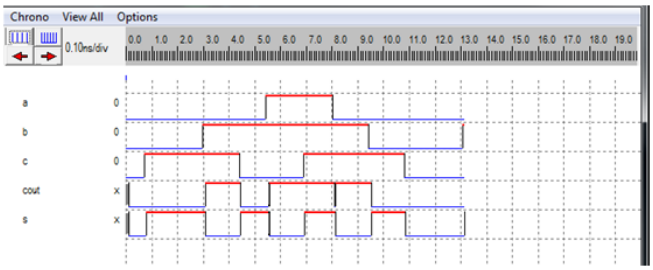

Fig 9: Timing Diagram of Double gate MOSFET full adder

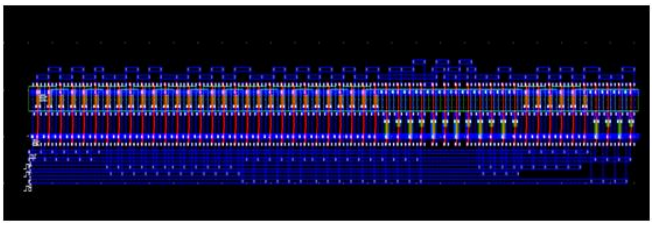

Fig 10: Layout of DoubleMOSFET full adder

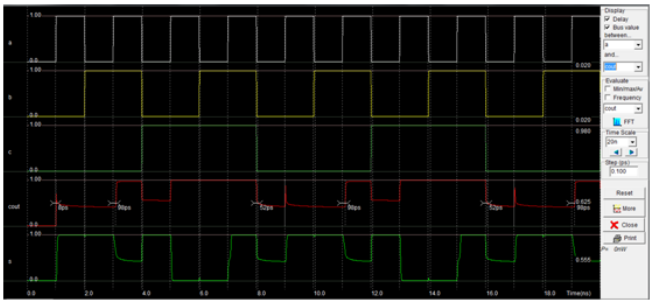

Fig 11: LayoutSimulation of Double gate MOSFET full adder

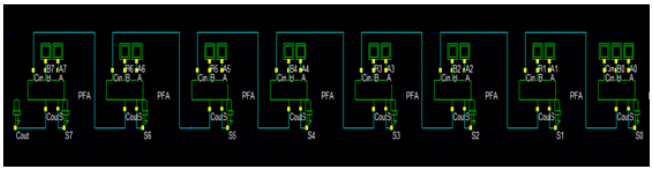

Fig 12: schematicof 8-bit RCA using Double gate MOSFET full adder

CONCLUSION:

The single gate MOSFET based full adder and DGMOSFET based full adder circuit has analyzed for various parameters. The power consumption is reduced for DGMOSFET based full adder cell as compare to other.

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The proposed circuit has higher speed and low power while it intact the digital characteristics. The proposed circuit can be used in designing low power ALU's and digital signal processors.

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