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Fully Reused VLSI Architecture of FMO/Manchester Encoding Using Sols Techinque for DSRC Applications

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Abstract:
Dedicated Short vary Communication could be a simplex or duplex short vary to medium vary wireless communication. It's wont to support Intelligent Transport System (ITS) applications like electronic toll assortment, parking zone, border crossing identification etc. It proposes a VLSI design style victimization similarity-oriented logic simplification (SOLS) technique. The SOLS consists of 2 core methods: area-compact retiming and balance logical operation sharing. The area-compact retiming relocates the hardware resource to scale back five transistors. The balance logical operation sharing with efficiency uses miller encodings with the absolutely reused hardware design with SOLS technique, we tend to constructs a totally reused VLSI design of Manchester and FMO encodings for DSRC applications. The experiment results reveal that this style achieves associate in nursing economical performance compared with subtle works. To attain dc balance, enhancing signal dependability, FMO and Manchester codes are employed in DSRC standards. The performance of this VLSI design is evaluated on cadence-post layout simulation tool with a hundred and eighty nm CMOS technology. The Manchester codes consumes most operation frequency is 2GHz with one. 58 mW power consumption Associate in Nursing d 900 megacycle for FMO secret writing with power consumption. The DSRC standards with FMO and Manchester cryptography will support America, Europe, and Japan. This paper conjointly shown that space compaction of planned VLSI design compared to existing technique.

Keywords:
Manchester coding, Encoder, Decoder, NRZ, Moore's law, UART, clock frequency.

I. INTRODUCTION:

Manchester secret writing technique may be a digital secret writing technique during which all the bits of the binary knowledge square measure organized in an exceedingly explicit sequence. Here a touch '1' is delineated by transmitting a high voltage for [*fr1] period of the signal and for consecutive intermission period associate degree inverted signal are send. When transmitting '0' in Manchester format, for the first half cycle an occasional voltage can send, and for consecutive [*fr1] cycle a high voltage is send. The advantage of Manchester secret writing is that, once causation an information having continuous high signals or continuous low signal (e.g.:11110000), it's tough to calculate the quantity of one S and Os within the knowledge. as a result of there's no transition from low to high or high to low for a selected period (Here it's four x T, T is the time period for one pulse). The detection is feasible solely by shrewd the time period of the signal. However after we code this signal in Manchester format there will invariably be a transition from high to low or low to high for every bit. Therefore for a receiver it is easier to find the information in Manchester format and additionally the likelihood for incidence of an error is incredibly low in Manchester format and it is a universally accepted digital cryptography technique. The dedicated short vary communication may be a protocol for one or 2 manner medium vary communication.

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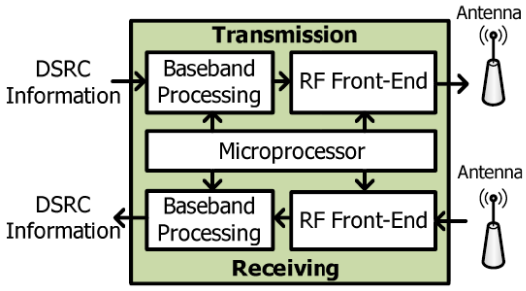
The DSRC will be briefly classified into 2 categories: automobile-to-automobile and automobile-to roadside. In automobile-to-automobile, the DSRC allows the message causation and broadcasting among automobile. The automobile-to-roadside focuses on the intelligent transportation service, such as electronic toll assortment (ETC).The DSRC architecture having the transceiver. The transceiver having the baseband processor forepart and micro chip. The microprocessor is employed to transfer the instruction to the baseband process and RF front end. the RF forepart is employed to transmit and receive the wireless signals mistreatment the antenna. The baseband process is accountable for modulation, error correction, cryptography and synchronization. The transmitted signal consists of the whimsical binary sequence, it is very difficult to get the dc-balance.the FMO and Manchester square measure gives the transmitted signal and then the dc-balance. The (SOLS) similarity oriented logic simplification having the 2 methods: space compact retiming and balance logic operation sharing. The world compact retiming wont to cut back the junction transistor counts .the balance operation sharing is employed to combine the FMO and Manchester cryptography. The system design of DSRC transceiver is shown in Fig. 1. The higher and bottom elements square measure dedicated for transmission and receiving, severally.



This transceiver is classified into 3 basic modules: microprocessor, baseband process, and RF front-end. The micro chip interprets instructions from media access management to schedule the tasks of baseband process and RF front-end. The baseband process is accountable for modulation, error correction, clock synchronization, and cryptography.

The RF frontend transmits and receives the wireless signal through the antenna. The DSRC standards are established by many organizations in numerous countries. These DSRC standards of America, Europe, and Japan square measure shown in Table I. The data rate singly targets at five hundred kb/s, 4 Mb/s, and 27 Mb/s with carrier frequency of five.8 and 5.9 GHz. The modulation ways incorporate amplitude shift keying, section shift keying, and orthogonal frequency division multiplexing. Generally, the undulation of transmitted signal is expected to own zero mean for lustiness issue, and this can be additionally remarked as dc-balance.

II. Literature Survey:

The transmitted signal consists of arbitrary binary sequence that is tough to get dc-balance. The needs of FMO and Manchester codes will offer the transmitted signal with dc-balance. Each FMO and Manchester codes are wide adopted in coding for downlink. The VLSI architectures of FMO and Manchester encoders' are reviewed as follows

A. Review of VLSI Architectures for FMO Encoder and Manchester Encoder

The literature [4] proposes a VLSI design of Manchester encoder for optical communications. This style adopts the CMOS electrical converter and also the gated electrical converter because the switch to construct Manchester encoder. it's enforced by zero.35-µm CMOS technology and its operation frequency is one Gc. The literature [5] additional replaces the design of switch in [4] by the nMOS device. It's completed in 90-nm CMOS technology, and also the most operation frequency is as high as five Gc. The literature [6] develops a high-speed VLSI design nearly absolutely reused with Manchester and Miller encodings for oftenest identification (RFID) applications. This style is completed in zero.35-µm CMOS technology and also the most operation frequency is two hundred rates. The literature [7] conjointly proposes Manchester encryption design for UHF (UHF) RFID tag.

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This hardware design is conducted from the finite state machine (FSM) of Manchester code, and is completed into field programmable gate array (FPGA) prototyping system. The utmost operation frequency of this style is concerning 256 rates. The similar style methodology is additional applied to singly construct FMO and Miller encoders conjointly for UHF RFID Tag apery [8]. Its most operation frequency is concerning 192 rates. What is more, [9] combines frequency shift keying (FSK) modulation and reception with Manchester codec in hardware realization.

III. CODING PRINCIPLES OF FMO CODE AND MANCHESTERCODE:

n the following discussion, the clock signal and the input data are abbreviated as CLK, and X, respectively. With the above parameters, the coding principles of FMO and Manchester codes are discussed as follows. A. FMO Encoding As shown in Fig. 2, for each X, the FMO code consists of two parts: one for former-half cycle of CLK, A, and the other one for later-half cycle of CLK,B. The coding principle of FMO is listed as the following three rules.

1) If X is the logic-0, the FMO code must exhibit a transition between A and B.
2) If X is the logic-1, no transition is allowed between A and B.
3) The transition is allocated among each FMO code no matter what the X is.

A FMO coding example is shown in Fig. 3. At cycle 1, the X is logic-0; therefore, a transition occurs on its FMO code, according to rule 1. For simplicity, this transition is initially set from logic-0 to -1. According to rule 3, a transition is allocated among each FMO code, and thereby the logic-1 is changed to logic-0 in the beginning of cycle 2. Then, according to rule 2, this logic-level is hold without any transition in entire cycle 2 for the X of logic-1. Thus, the FMO code of each cycle can be derived with these three rules mentioned earlier.

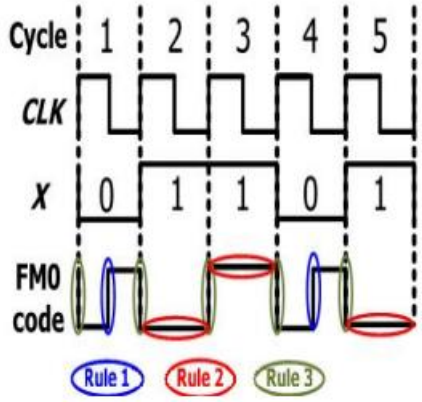

Illustration of FMO coding example.

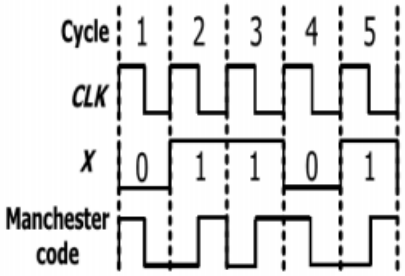

Illustration of Manchester coding example

Hardware Architecture of FMO/Manchester Code:

This is the hardware design of the FMO/Manchester code. The highest half is denoted the FMO code so rock bottom half is denoted because the Manchester code. in FMO code the DFFA and DFFB area unit accustomed store the state code of the FMO code and additionally mux_1 and not gate is employed within the FMO code. once the mode=0 is for the FMO code. The Manchester code is developed solely mistreatment the X-OR circuit and once the mode=1 is for the Manchester code. The hardware utilization rate is outlined because the following the active elements means that the elements area unit add the each FMO and Manchester code. the entire elements means that the amount of the elements area unit gift within the hole circuit. The HUR rate is given below the subsequent section

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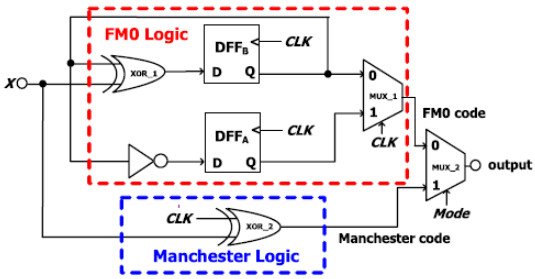
Coding	Active components (transistor count) / Total components (transistor count)	HUR
FM0	6 (86) / 7 (98)	85.71%
Manchester	2 (26) / 7 (98)	28.57%
Average	4 (56) / 7 (98)	57.14%



Hardware architecture

HUR OF FMO AND MANCHESTER ENCODINGS

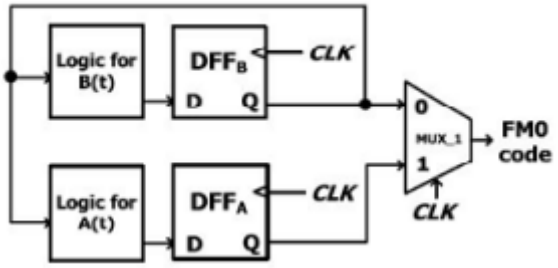
For each the encryption ways the entire elements is seven. for the FMO code the entire element is seven so the active element is six. In Manchester code the entire element is seven the active element is two. in each committal to writing having ninety eight transistors area unit used while not SOLS. The FMO is having eighty six semiconductor device, so the Manchester having the twenty six semiconductor device. The common for each committal to writing is fifty six transistors .In planned work scale back the entire elements from seven to six and scale back the semiconductor device counts. During these paper 2 electronic devices is employed in planned work scale back 2 electronic device from one electronic device, once scale back the electronic device the entire elements area unit reduced the realm so the ability consumption additionally reduced.

IV. FMO and Manchester Encoder Using Sols Technique:

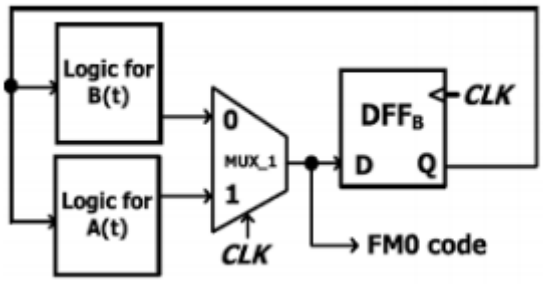
The SOLS technique is classified into two parts area compact retiming and balance logic operation sharing

A. Area Compact Retiming:

For FMO the state code of the each state is stored into DFFA and DFFB .the transition of the state code is only depends on the previous state of B(t-1) instead of the both A(t-1) and B(t-1)



Area compact retiming



FMO encoding without area compact retiming

The previous state is denoted as the A(t-1) and then the B(t-1).and then the current state is denoted as the A(t) and then the B(t). Thus, the FMO encoding just requires a single 1-bitflip-flop to store the previous value B(t−1).If the DFFA is directly removed, a non synchronization between A(t) and B(t)causes the logic fault of FMO code. To avoid this logic-fault, the DFFB is relocated right after the MUX−1, where the DFFB is assumed be positive-edge triggered flip flop. At each cycle, the FMO code, comprising A and B, is derived from the logic of A(t) and the logic of B(t), respectively. The FMO code is alternatively switched between A(t) and B(t) through the MUX−1 by the control signal of the CLK. In the Q of DFFB is directly updated from the logic of B(t)with 1-cycle latency. When the CLK is logic-0, the B(t) is passed through MUX−1 to the D of DFFB. Then, the upcoming positive-edge of CLK updates it to the Q of DFFB. The timing diagram for the Q of DFFB is consistent whether the DFFB is relocated or not.

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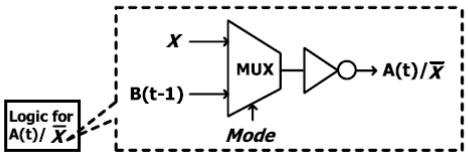
The B(t) is passed through MUX−1 to the D of DFFB. Then, the upcoming positive-edge of CLK updates it to the Q of DFFB. The timing diagram for the Q of DFFB is consistent whether the DFFB is relocated or not. The transistor count of the FMO encoding architecture without area-compact retiming is 72, and that with area-compact retiming is 50. The area-compact retiming technique reduces 22 transistors.

B. Balance logic operation sharing:

The Manchester encoding is derived using the XOR operation. The equation of the XOR gate is given below.

$$X \oplus CLK = X\,CLK + \sim X\,CLK$$

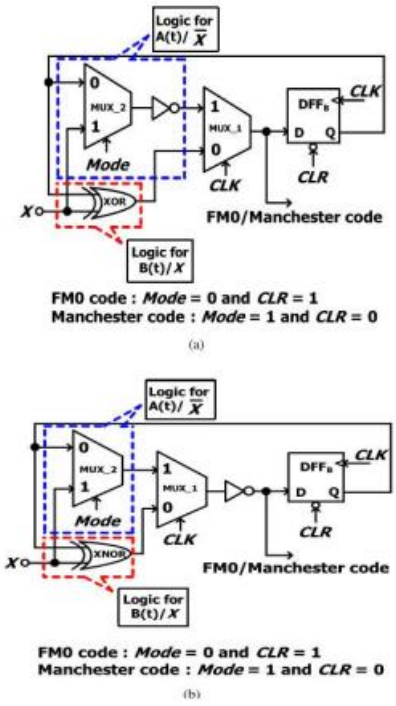
The concept of balance logic-operation sharing is to integrate the X into A(t) and X into B(t).the FMO and Manchester logics have a common point of the multiplexer like logic with the selection of the CLK. the diagram for the balance logic operation sharing given the following. The A(t) can be derived from an inverter of B(t − 1), and X is obtained by an inverter of X. The logic for A(t)/X can share the same inverter, and then a multiplexer is placed before the inverter to switch he operands of B(t − 1) and X. The Mode indicates eitherFMO or Manchester encoding is adopted. The similar concept can be also applied to the logic for B(t)/X.



Balance logic-operation sharing of A(t) and X:

Nevertheless, this architecture exhibits a drawback that the XOR is only dedicated for FMO encoding, and is not shared with Manchester encoding. Therefore, the HUR of this architecture is certainly limited. The X can be also interpreted as the X 0, and thereby the XOR operation can be shared with Manchester and FMO encodings, where the multiplexer irresponsible to switch the operands of B(t−1) and logic-0. This architecture shares the XOR for both B(t) and X, and there by increases the HUR.

When the FMO code is adopted, the CLR is disabled, and the B(t −1) can be derived from DFFB .Hence, the multiplexer can be totally saved, and its function can be completely integrated into the relocated DFF. The logic for A(t)/X includes the MUX−2 and an inverter. Instead, the logic for B(t)/X just incorporates a XOR gate. In the logic for A(t)/X, the computation time of MUX−2is almost identical to that of XOR in the logic for B(t)/X. However, the logic for A(t)/X further incorporates an inverter in the series of MUX−2. This unbalance computation time between A(t)/X and B(t)/X results in the glitch to MUX−1,possibly causing the logic fault on coding. To alleviate this unbalance computation time, the architecture of the balance computation time between A(t)/X and B(t)/X The XOR in the logic for B(t)/X is translated into the XNOR with an inverter, and then this inverter is shared with that of the logic for A(t)/X. This shared inverter is relocated backward to the output of MUX−1. Thus, the logic computation time between A(t)/X and B(t)/X is more balance to each other.



VLSI architecture of FMO and Manchester encodings using SOLS technique. (a) Unbalance computation time between A(t)/Xand B(t)/X. (b) Balance computation time between A(t)/XandB(t)/X.

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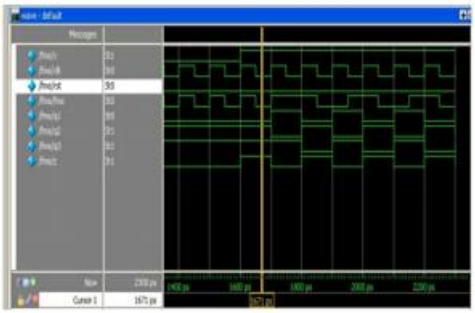
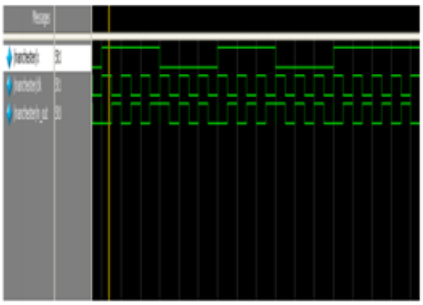
The adoption of FMO or Manchester code depends on Mode and CLR. Additionally, the CLR more has another individual operate of a hardware format. If the CLR is solely derived by inverting Mode while not assignment a personal CLR management signals, this ends up in a conflict between the secret writing mode choice and the hardware format. To avoid this conflict, each Mode and CLR area unit assumed to be on an individual basis allotted to the present style from a system controller. Whether or not FMO or Manchester code is adopted, no logic part of the projected VLSI design is wasted. Each part is active in each FMO and Manchester encodings. Therefore, the HUR of the projected VLSI design is greatly improved.

V. Simulation Results

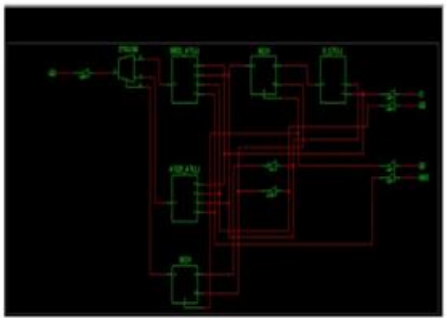
FMO Waveform Result:



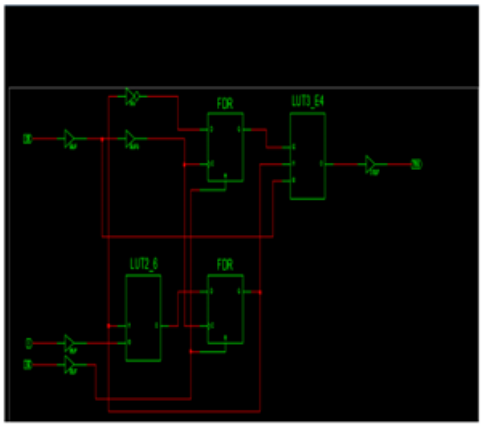
Manchester Waveform Result:



RTL Schematic:



Technology Schematic:



CONCLUSION:

The coding-diversity between FMO and Manchester encodings causes the limitation on hardware utilization of VLSI architecture design. A limitation analysis on hardware utilization of FMO and Manchester encodings is discussed in detail. In this paper, the fully reused VLSI architecture using SOLS technique for both FMO and Manchester encodings is proposed. The SOLS technique eliminates the limitation on hardware utilization by two core techniques: area compact retiming and balance logic operation sharing. The area-compact retiming relocates the hardware resource to reduce the transistors. The balance logic-operation sharing efficiently combines FMO and Manchester encodings with the identical logic components. This paper is realized in180nm technology with outstanding device efficiency. The power consumption is 29392.843nW for Manchester encoding and FMO encoding.

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