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Implementation of High Performance of SRAM Cell Using Transmission Gate

Dr. P. John Paul
Professor,
Department of ECE,
Malla Reddy College of Engineering.

Ms. Anna Saipriya
Student,
Department of ECE,
Malla Reddy College of Engineering.

ABSTRACT:

Static Random Access Memory (SRAM) has become a major component in many VLSI Chips due to their large storage density and small access time. SRAM has become the topic of substantial research due to the rapid development for low power. SRAM plays a most substantial role in the microprocessor world, but as the technology is scaling down in nano meters, leakage parameters and delay are the most common problems for SRAM cell which is basically designed for very low power application. Transmission gate is used to further reduced leakage current penetrating in the 8T SRAM cell. Comparative analysis is performed by using transmission gate. This paper represents a method for design a variability aware SRAM cell. The proposed architecture of the TG8T SRAM cell is analogous to the standard 6T SRAM cell, the only exception is that they possess full transmission gates which replace an access pass transistor.

Keywords ***–6T SRAM cell, Power dissipation, Transmission Gates, 8T SRAM.***

I.INTRODUCTION

Static random-access memory is a type of semiconductor memory that uses bistable latching circuitry to store each bit. The term static differentiates it from dynamic RAM which must be periodically refreshed. SRAM exhibits data remembrance, but is still volatile in conventional sense, that data is eventually lost when memory is not powered.The continuous scaling down of bulk CMOS creates major issues due to its base material .The primary obstacles to the scaling of bulk CMOS to 32nmgatelengths include short channel effects ,Sub-threshold leakage ,gate-dielectric leakage and device to device variations. Due to sudden increase in threshold voltage i.e. Vt oscillation produced by overall and general process variations occur in ultra-short channel devices, 6T SRAM cell and their modifications cannot be operated at advance scaling of supply voltages without functional and parametric failure causes yield loss. The design of standard 6T SRAM cell undergoes a lot of problem on write delay [1].The design of Low power 6T SRAM cell could decrease the write power and access delay [2] but could not improve their stability. In deep submicron ranges, none of the earlier works has studied about the improvement of variability in SRAM cell at the schematic level .Therefore, we design a vigorous and variation accepting SRAM cell design technique capable of gripping Vt shift due to random dopant fluctuation(RDF), and variation in further device and their process parameters (such as length, width, sub-wavelength-lithography ,oxide thickness, etching, and annealing) and still be able to perform expected functions need to be investigated. To fulfill this drawback we propose a transmission gate 8T SRAM cell (TG8T) and compare their performance with standard 6T SRAM cell at cadence virtuoso tool at 45nm technology.

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The rest of the paper is designed as follows. Section 2 shows the existing design and its operation. Section 3 shows the proposed design and its operation. Section 4 shows the simulation result with standard 6T SRAM cell and TG8T SRAM. At last we show the conclusion in Section 5.

II.6T SRAM CELL OPERATION

The memory circuit is said to be static if the stored data can be retained indefinitely, as long as the power supply is on, without any need for periodic refresh operation. The data storage cell, i.e., the one-bit memory cell in the static RAM arrays, invariably consists of a simple latch circuit with two stable operating points. Depending on the preserved state of the two inverter latch circuit, the data being held in the memory cell will be interpreted either as logic '0' or as logic '1'.operations of SRAM as follows

1. Standby Mode (the circuit is idle)

In standby mode word line is not asserted (word line=0), so pass transistors N3 and N4 which connect 6t cell from bit lines are turned off. It means that cell cannot be accessed. The two cross coupled inverters formed by N1-N2 will continue to feed back each other as long as they are connected to the supply, and data will hold in the latch.

2. Read Mode (the data has been requested)

In read mode word line is asserted (word line=1), Word line enables both the access transistor which will connect cell from the bit lines. Now values stored in nodes (node a and b) are transferred to the bit lines. Assume that 1 is stored at node a so bit line bar will discharge through the driver transistor (N1) and the bit line will be pull up through the Load transistors (P1) toward VDD, a logical 1. Design of SRAM cell requires read stability (do not disturb data when reading).

3. Write Mode (updating the contents)

Assume that the cell is originally storing a 1 and we wish to write a 0. To do this, the bit line is lowered to 0V and bit bar is raised to VDD, and cell is selected by raising the word line to VDD.

Typically, each of the inverters is designed so that PMOS and NMOS are matched, thus inverter threshold is kept at VDD/2. If we wish to write 0 at node a, N3 operates in saturation. Initially, its source voltage is 1. Drain terminal of N2 is initially at 1 which is pulled down by N3 because access transistor N3 is stronger than N1. Now N2 turns on and P1 turns off, thus new value has been written which forces bit line lowered to 0V and bit bar to VDD. SRAM to operate in write mode must have write-ability which is minimum bit line voltage required to flip the state of the cell.

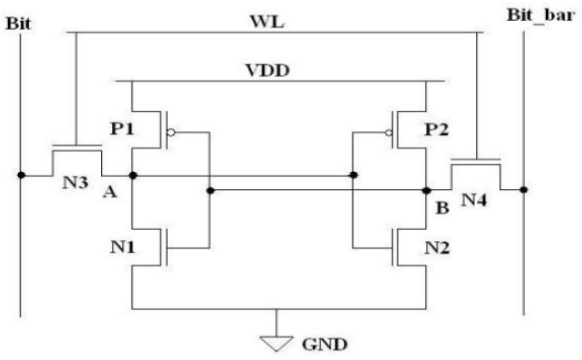

Fig 1: Schematic of 6T SRAM cell

II. PROPOSED TRANSMISSION GATE BASED 8T SRAM CELL (TG8T)

This fragment shows the proposed architecture of TG8T SRAM which is resembles to the standard 6T SRAM cell.

Architecture of TG8T SRAM cell

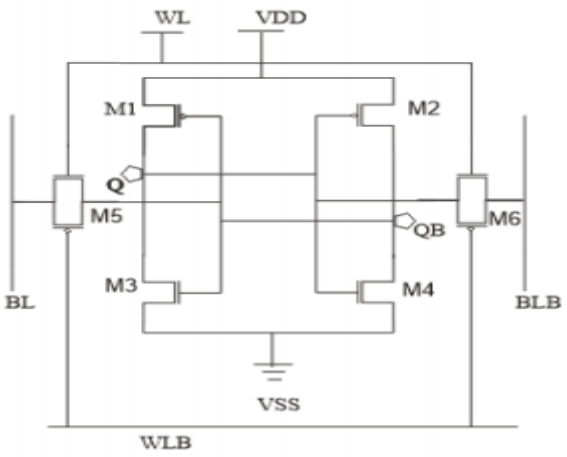

Fig.2 Proposed TG-based fully 8T SRAM cell (TG8T).

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The main motive behind the forceful device scaling is toachieve enriched performance and increased integration.These improvements led to the costof increased sensitivity to standby leakage, delay mostly in areaconstrained circuit such as SRAM that requires minimumgeometry devices[3]. In this work, an effort has to be done to solve these problems in conventional 6T SRAM cell by considering minimum area consequences and achieve its fully differential architecture. This paper proposes a design of TG-based fully differential 8T SRAM cell (Fig.2) and their design metrics shows in the conventional 6T SRAM cell shown at Fig.1.

TG8T uses differential operation and does not possess as much architectural changes except adding a PMOS in parallel with each access NMOS in conventional 6T SRAM cell shown by M5 and M6, by this we make it TG8T SRAM cell. An additional control WLB is required for switching the access PMOS. The WLB and WL (word line) are non-overlapping opposite signals. Therefore, during read and write operation, to retrieve the data from cell all access FETs are swapped simultaneously. But, during hold mode all access FETs remain shot off.

Working of TG8T SRAM cell.

The working of TG8T SRAM cell consist of two operation i.e. write and read operation. When we performing a write operation ,both the bit lines are at opposite voltages which represent if bit line BL is at high then BLB is at low and vice versa (BL=1 and BLB =0 or BL =0 and BLB =1). When WL becomes high and also WLB =0 which enables NMOS and PMOS transistors M5 and M6 then data writes on the output nodes Q and QB of back to back connected inverter.

When we perform the read operation which is just opposite to the write operation, both the bit lines are at high voltages also behave as an output and WL is raised to high and WLB at 0. Since one of the output nodes (Q and QB) is at low then one of pre-charged bit lines start discharging and at that instant data is going to be read.

IV.SIMULATION RESULTS

All the simulations are performed on Microwind and DSCH.The main focus of this work is to meet all challenges faces in designing of memory circuit at Nano scale technology, where deviations arisesdue to process and environmental parameters such as operating voltage and temperature. The basic cause of variations is scaling. The leakage current of TG8T SRAM cell is improved as compared to conventional 6T SRAM cell. The simulation results are shown below figures.

Table:1 Comparisons results of 6T and 8T SRAM cells

DESIGN	PARAMETERS		
	POWER	DEALY	NO.OF TRANSISTORS
EXISTING SRAM	7.315uw	0.30ns	6T
PROPOSED SRAM	6.647uw	0.13ns	8T

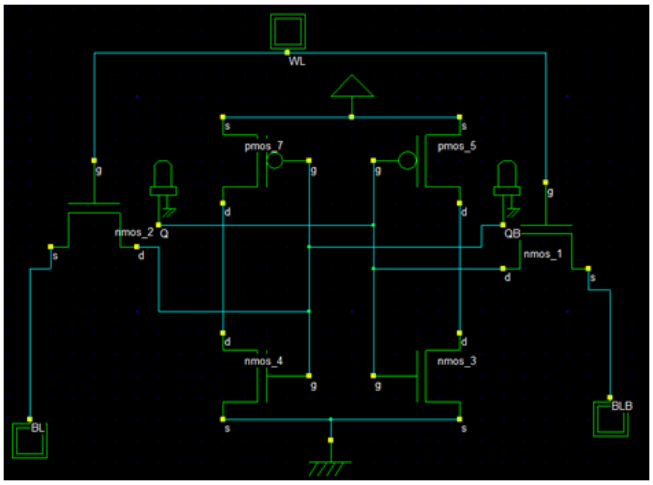

Fig 3: Schematic of 6T SRAM cell

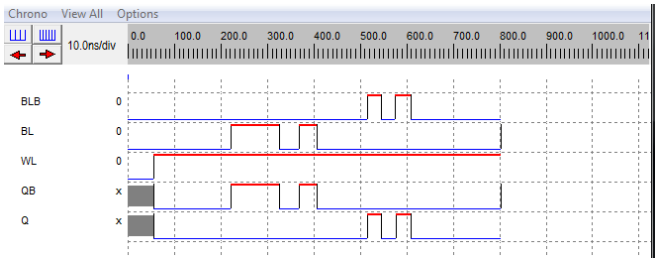

Fig 4: Timing Diagram of 6T SRAM cell

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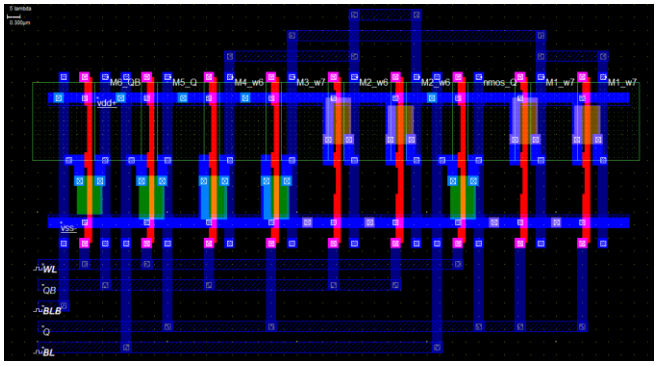

Fig 5: Layout of 6T SRAM cell

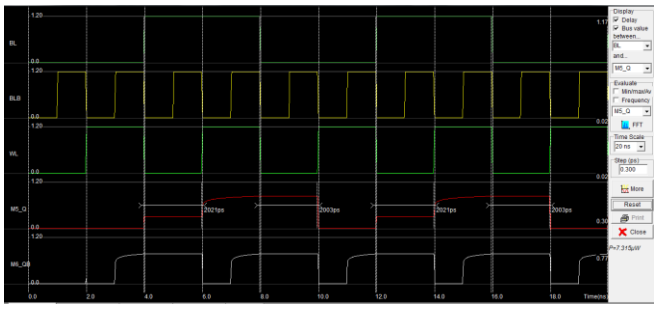

Fig 6: Simulation of Layout of 6T SRAM cell

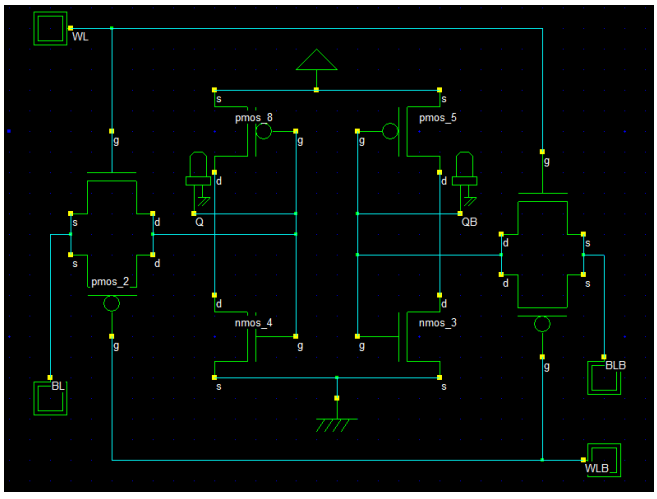

Fig 7: Schematic of 8T SRAM cell

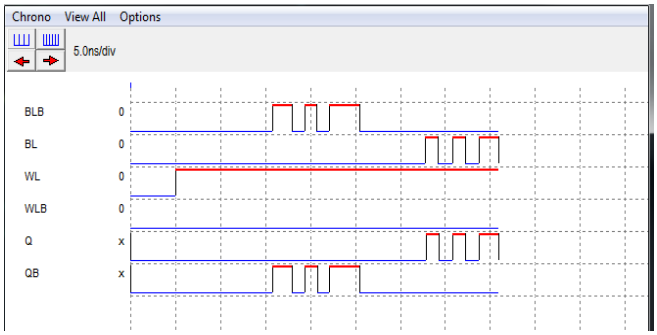

Fig 8: Timing Diagram of 8T SRAM cell

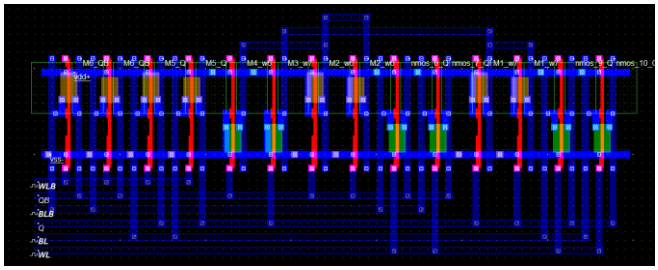

Fig 9: Layout of 8T SRAM cell

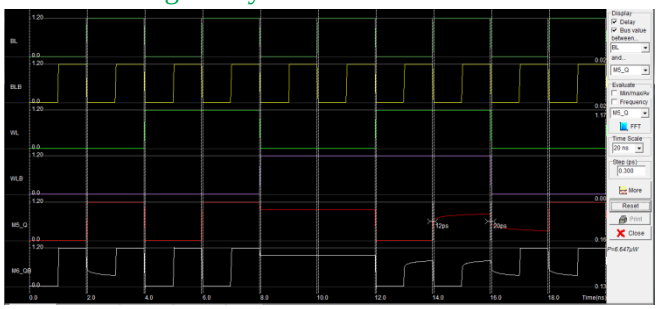

Fig 10: Simulation of Layout of 6T SRAM cell

CONCLUSION

The improved read and write-ability (data stability), reduced dynamic and leakage power dissipation compared to standard 6T, makes the new approach attractive for nano scale technology regime, in which process variation is a major design constraint. By comparing I conclude that in TG based 8T SRAM cell leakage power is reduced to6.6315uW than Conventional 6TSRAM leakage power is reduced to 6.974 uW. Theresults show major enhancement in most of the design parameters over standard 6T SRAM cell signifying its strength and functionality.

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