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Ultra Low Energy Variation Aware Design Adder Architecture Study

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Abstract

Power consumption of digital systems is an important issue in nanoscale technologies and growth of process variation makes the problem more challenging. In this brief, we have analyzed the latency, energy consumption, and effects of process variation on different structures with respect to the design structure and logic depth to propose architectures with higher throughput, lower energy consumption, and smaller performance loss caused by process variation in application specific integrated circuit design. We have exploited adders as different implementations of a processing unit, and propose architectural guidelines for finer technologies in subthreshold which are applicable to any other architecture. The results show that smaller computing building blocks have better energy efficiency and less performance degradation because of variation effects. In contrast, their computation throughput will be mid or less unless proper solutions, such as pipelined or parallel structures, are used.

Therefore, our proposed solution to improve the throughput loss while reducing sensitivity to process variations is using simpler elements in deep pipelined designs or massively parallel structures.

Index Terms— Adder structures, architecture, deep pipeline, massive parallel, statistical static timing analysis (SSTA), ultra low energy, variation-aware.

INTRODUCTION

As technology advances, the density of integrated circuits grows and power consumption becomes more and more serious [1]. This problem affects the performance of design and causes heating and power supply shortage problems. One major solution is using near/subthreshold computing to reduce power consumption over the complex systems-on-chip [2]. Near and subthreshold computing is attractive in energy-constrained applications, such as sensor networks, to increase lifetime and provide energy harvesting capability for some emerging applications. In subthreshold region, both static and dynamic ingredients of power consumption are severely reduced because of lower supply voltage.

However, circuit delay grows exponentially by descending voltage level and hence, the static energy consumption is increased.

In this brief, we use SSTA method to analyze adder structures considering process variations and extract effective architectural level design guidelines to

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improve speed performance and energy efficiency. The rest of this brief is organized as follows. In Section II, we will introduce existing designs of adders. In Section III advantages and disadvantages of some popular adder structures as basic blocks of arithmetic units. In Section IV, we will describe our method and analyze the results and introduce some key guidelines. Finally, the conclusion is drawn in Section V.

PREVIOUS DESIGNS

Ripple-carry adder (RCA) has simple architecture and linearly extensible for wider computations with respect to area. However, this adder has limited performance because of long carry propagation path from LSB to MSB. Because of long critical path delays in RCA, designers have tried to look ahead carry bit for each higher bit independent of lower neighboring carry bits using a logarithmic delay tree structure, and each tree optimization strategy implies a new prefix adder.

PRIMILIRIES

In minimum energy point of energy-voltage curve, this increase in static energy dominates the dynamic energy consumption, and scaling supply voltage to lower levels means more delay and more total energy consumption [2], [3]. Because of feature size scaling, the impact of process variations becomes significant and near/subthreshold design intensifies the effects of variations and severely degrades the performance parameters [4]–[6]. In order to control process variation effects, we need to do careful timing analysis and employ statistical approaches rather than the classic worst case analysis. Static timing analysis (STA) was previously implemented in commercial tools [7] and worst case conditions were considered for each cell timing. Then, cell parameters were used to calculate delays of paths in a complex design by adding up delays of gates in series (n = number of gates)

$$\text{Delay}_{\text{Critical-path}} = \sum_{i=1}^{n} (\mu_i + 3 \times \delta_i) \quad \ldots.(1)$$

where μi and δi represent mean and standard deviation of delay for each gate, respectively. In new technologies, variation has grown and using STA yields losing much of the speed performance, unnecessarily. However, statistical STA (SSTA) is another way to analyze the timing specifications of critical paths of a design for getting more realistic results. Variation of each cell is assumed as a normal (Gaussian) variable [5], [8] (2) and (3) [9]

$$\mu_{\text{Critical-path}} = \sum_{i=1}^{n} \mu_i, \quad \delta^2_{\text{Critical-path}} = \sum_{i=1}^{n} \delta_i^2 \quad (2)$$

$$\text{Delay}_{\text{Critical-path}} = \mu_{\text{Critical-path}} + 3 \times \sigma_{\text{Critical-path}} \quad (3)$$

The SSTA is an accepted method based on statistical manner of variations and supported by recent commercial tools [7], [10]. In this method, σ /μ [3], [5], [9] is an important ratio to compare the severity of variations in cells to have better standard cell design in deep subthreshold region. Verma et al. [11] extracted logic chains for Kogge–Stone adder (KSA) to measure delay variability in both 0.3 and 1.2 V voltages. σ /μ ratio contours have been drawn based on delay variability histogram, logic depth, and gate width, and variability mitigation is performed by gate up-sizing. Newer technologies such as dual gate silicon on insulator [12] have lower variability in comparison with bulk CMOS to design robust subthreshold logic cells in 32-nm CMOS. Thakur et al. [13] analyzed the effects of variations in gate oxide thickness, supply voltage, and temperature in four adders and they tried to rank the variation effect of each parameter on delay. As a new design method in [14], SSTA is used to sieve a standard cell library with different variation constraints during synthesis of arithmetic circuits. They have verified the results by Monte Carlo simulations. Islam et al. [15] have designed a robust (lower σ /μ ratio) subthreshold full adder considering power-delay product. Arthurs and Di [16] evaluate the variations of both Schmitt-trigger and NULL convention logic 1-bit adders by four-gate libraries characterized at different supply voltages for better static noise margin.

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SERIAL FULL ADDER (SFA) STRUCTURE

We choose adder as the key building block of arithmetic units in every processor ranging from general purpose to application specific, because it can be used to implement more complex operations such as multiplication and division or even more complex units, such as fast Fourier transform and finite-impulse response filters. We have selected six different 16-bit adder structures [17], [18] to study in subthreshold region. Ripple-carry adder (RCA) has simple architecture and linearly extensible for wider computations with respect to area.

However, this adder has limited performance because of long carry propagation path from LSB to MSB. Because of long critical path delays in RCA, designers have tried to look ahead carry bit for each higher bit independent of lower neighboring carry bits using a logarithmicdelay tree structure, and each tree optimization strategy implies a new prefix adder. The first candidate prefix adder discussed is Brent–Kung adder (BKA). This structure has balanced area and timing overheads with shortening the long carry chains [((2×log2 N)−2) logic stages] which is a proper technique to co-optimize area and performance of design. In KSA, addition is performed with higher speed because of parallel computations in shorter paths with only log2 N logic stages besides higher area overhead. Han–Carlson adder (HCA) is a combination of BKA and KSA to reduce the complexity and make a tradeoff between area and delay with log2 N +1 logic stages. Another prefix adder which has minimum logic depth (log2 N) is known as Lander–Fisher adder (LFA).

In this architecture, some nodes have very high fan-outs (up to N/2) to reduce the area and this may degrade the performance. Serial full adder (SFA) is a basic full adder which is combined with a flip-flop to utilize the adder unit at different clock cycles in time-serialized ripple-carry manner (Fig. 1) and the number of clock cycles that it takes is equal to the number of bits.

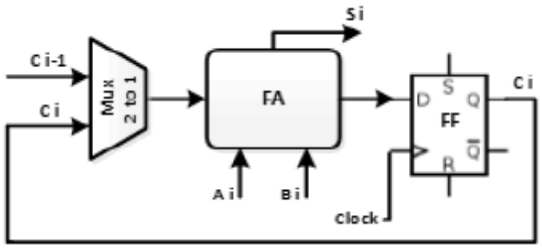

Fig. 1. Single-bit full adder in combination with a flip-flop to do n-bit addition sequentially at different clock cycles.

SIMULATION RESULTS

We have coded the all Serial Full Adders techniques in Verilog HDL. All the designs are synthesized in the Xilinx Synthesis Tool and Simulated using Xilinx ISE 14.4 simulator. The synthesis and simulation results are as shown below figures.

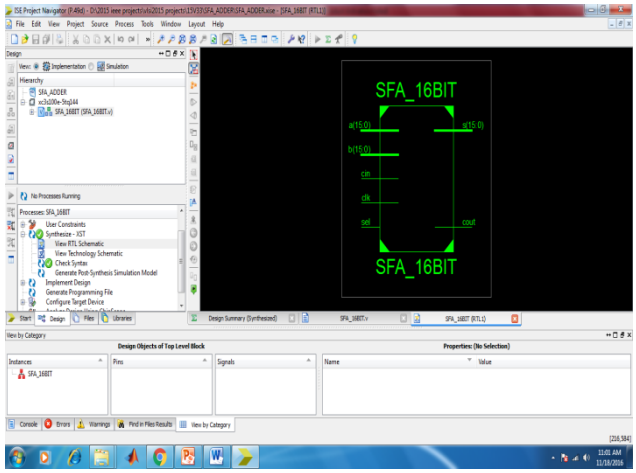

Fig2: Block diagram of 16bit-SFA Adder

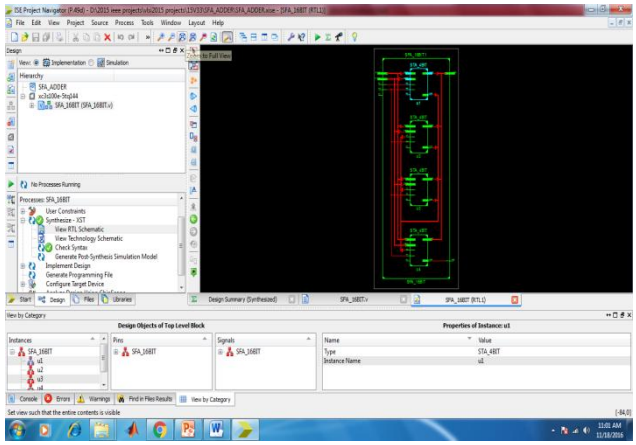

Fig3: RTL Schematic of 16bit- SFA Adder

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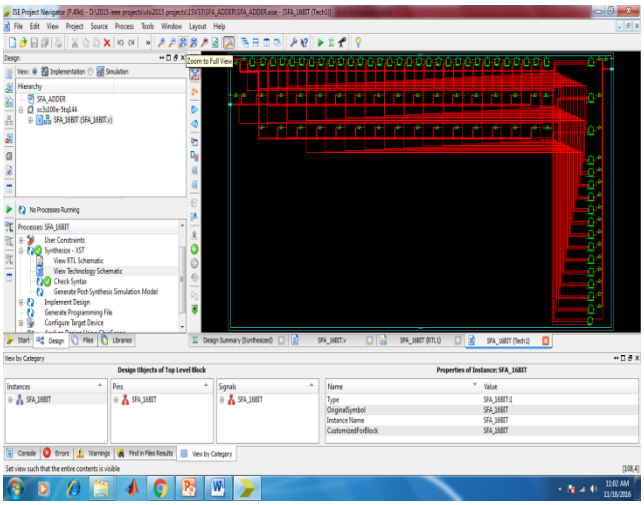

Fig4: Technology Schematic of 16bit- SFA Adder

SFA_16BIT Project Status (11/18/2016 - 11:01:36)			
Project File:	SFA_ADDER.xise	**Parser Errors:**	No Errors
Module Name:	SFA_16BIT	**Implementation State:**	Synthesized
Target Device:	xc3s100e-5tq144	**• Errors:**	No Errors
Product Version:	ISE 14.4	**• Warnings:**	23 Warnings (0 new)
Design Goal:	Balanced	**• Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	**• Timing Constraints:**	
Environment:	System Settings	**• Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	17	960	1%
Number of Slice Flip Flops	16	1920	0%
Number of 4 input LUTs	33	1920	1%
Number of bonded IOBs	51	108	47%
Number of GCLKs	1	24	4%

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**

Fig5: Design summary of 16bit- SFA Adder

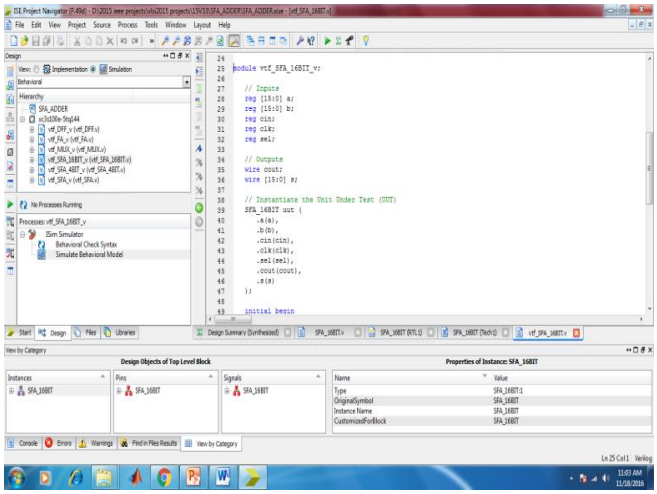

Fig6: Test bench of 16bit- SFA Adder

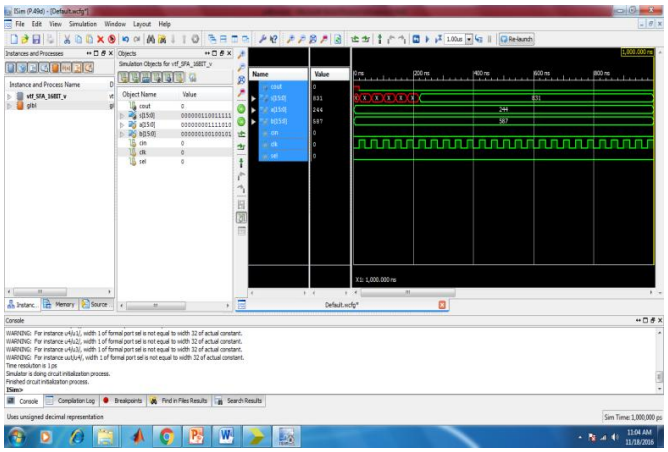

Fig7: Simulation output waveform of 16bit- SFA Adder

CONCLUSION

In this brief, we have analyzed the latency, energy consumption, and effects of process variation on different adder structures as different implementations of a popular processing unit with respect to the design structure and logic depth to propose architectural guidelines. These guidelines are applicable to any other architecture without any dependence to functionality of the design to achieve higher throughput, lower energy consumption, and smaller performance loss caused by process variation in application-specific integrated circuit design. Simulation results and analysis confirm that, SFA has smaller area, less timing fluctuations, and the highest working frequency, and its throughput is similar to RCA. Utilizing SFA in parallel architecture or pipelined version of RCA improves the throughput besides the energy efficiency and variation resistance.

Finally, we conclude that utilizing such blocks in a massively parallel architecture is another way to compensate the process variation effects and lower the frequency uncertainty plus lowering timing fluctuations due to process variations.

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