

Fault Tolerant Parallel Filters Based on Error Correction Codes



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Abstract

Digital Signal Processing is used in wide range of applications such as radio, television, and video. Its main basic tool Finite Impulse Response (FIR) digital filters. In some cases, the reliability of those systems is critical, and fault tolerant filter implementations are needed. Over the years, many techniques that exploit the filters' structure and properties to achieve fault tolerance have been proposed. As technology scales, it enables more complex systems that incorporate many filters. In those complex systems, it is common that some of the filters operate in parallel, for example, by applying the same filter to different input signals. Recently, a simple technique that exploits the presence of parallel filters to achieve fault tolerance has been presented.

In this brief, that idea is generalized to show that parallel filters can be protected using error correction codes (ECCs) in which each filter is the equivalent of a bit in a traditional ECC. This new scheme allows more efficient protection when the number of parallel filters is large. The technique is evaluated using a case study of parallel finite impulse response filters showing the effectiveness in terms of protection and implementation cost.

Index Terms— Error correction codes (ECCs), filters, soft errors.

I.INTRODUCTION

FIR filters are one of two primary types of digital filters used in digital signal processing (DSP) applications, the other type being IIR. High performance FIR filters have applications in several video processing and digital communications systems.

Electronic circuits are increasingly present in automotive, medical, and space applications where reliability is critical. In those applications, the circuits have to provide some degree of fault tolerance. This need is further increased by the intrinsic reliability challenges of advanced CMOS technologies that include, e.g., manufacturing variations and soft errors.

A number of techniques can be used to protect a circuit from errors. Those range from modifications in the manufacturing process of the circuits to reduce the number of errors to adding redundancy at the logic or system level to ensure that errors do not affect the system functionality [1]. To add redundancy, a general technique known as triple modular redundancy (TMR) can be used. The TMR, which triplicates the design and adds voting logic to correct errors, is commonly used. However, it more than triples the area and power of the circuit, something that may not be acceptable in some applications. When the circuit to be protected has algorithmic or structural properties, a better option can be to exploit those properties to implement fault

tolerance. One example is signal processing circuits for which specific techniques have been proposed over the years [2].

Digital filters are one of the most commonly used signal processing circuits and several techniques have been proposed to protect them from errors. Most of them have focused on finite-impulse response (FIR) filters. For example, in [3], the use of reduced precision replicas was proposed to reduce the cost of implementing modular redundancy in FIR filters. In [4], a relationship between the memory elements of an FIR filter and the input sequence was used to detect errors. Other schemes have exploited the FIR properties at a word level to also achieve fault tolerance [5]. The use of residue number systems [6] and arithmetic codes [7] has also been proposed to protect filters. Finally, the use of different implementation structures of the FIR filters to correct errors with only one redundant module has also been proposed [8]. In all the techniques mentioned so far, the protection of a single filter is considered. However, it is increasingly common to find systems in which several filters operate in parallel. This is the case in filter banks [9] and in many modern communication systems [10]. For those systems, the protection of the filters can be addressed at a higher level by considering the parallel filters as the block to be protected. This idea was explored in [11], where two parallel filters with the same response that processed different input signals were considered. It was shown that with only one redundant copy, single error correction can be implemented. Therefore, a significant cost reduction compared with TMR was obtained. In this brief, a general scheme to protect parallel filters is presented. As in [11], parallel filters with the same response that process different input signals are considered. The new approach is based on the application of error correction codes (ECCs) using each of the filter outputs as the equivalent of a bit in an ECC code word. This is a generalization of the scheme presented in [11] and enables more efficient implementations when the number of parallel filters is

large. The scheme can also be used to provide more powerful protection using advanced ECCs that can correct failures in multiples modules.

The rest of this brief introduces the new scheme by first summarizing the parallel filters considered in Section II. Then, in Section III, the proposed scheme is presented. Section IV presents a results and discussion to illustrate the effectiveness of the approach. Section V presents a synthesis and simulations of the parallel filters approach. Finally, the conclusions are summarized in Section VI.

II. PARALLEL FILTERS DESIGN

A discrete time filter implements the following equation:

$$y[n] = \sum_{l=0}^{\infty} x[n-l] \cdot h[l] \tag{1}$$

where $x[n]$ is the input signal, $y[n]$ is the output, and $h[l]$ is the impulse response of the filter [12]. When the response $h[l]$ is nonzero, only for a finite number of samples, the filter is known as a FIR filter, otherwise the filter is an infinite impulse response (IIR) filter.

There are several structures to implement both FIR and IIR filters. In the following, a set of k parallel filters with the same response and different input signals are considered.

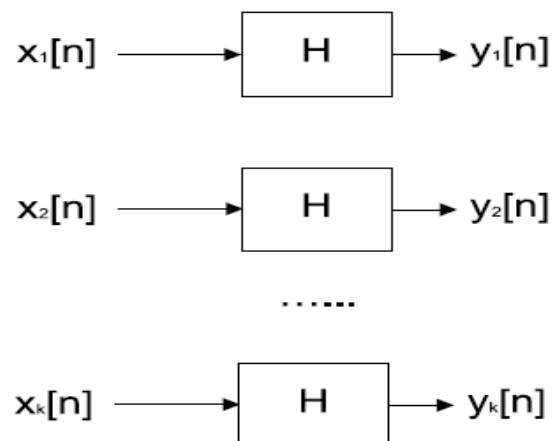


Fig.1. Parallel filters with the same response.

These parallel filters are illustrated in Fig. 1. This kind of filter is found in some communication systems that use several channels in parallel.

In data acquisition and processing applications is also common to filter several signals with the same response. An interesting property for these parallel filters is that the sum of any combination of the outputs $y_i[n]$ can also be obtained by adding the corresponding inputs $x_i[n]$ and filtering the resulting signal with the same filter $h[l]$. For example

$$y_1[n] + y_2[n] = \sum_{l=0}^{\infty} (x_1[n-l] + x_2[n-l]) \cdot h[l]. \quad (2)$$

III. PROPOSED SCHEME FOR PARALLEL FILTERS

The new technique is based on the use of the ECCs. A simple ECC takes a block of k bits and produces a block of n bits by adding $n-k$ parity check bits [13].

The parity check bits are XOR combinations of the k data bits. By properly designing those combinations it is possible to detect and correct errors. As an example, let us consider a simple Hamming code [14] with $k = 4$ and $n = 7$. In this case, the three parity check bits p_1, p_2, p_3 are computed as a function of the data bits d_1, d_2, d_3, d_4 as follows

$$\begin{aligned} p_1 &= d_1 \oplus d_2 \oplus d_3 \\ p_2 &= d_1 \oplus d_2 \oplus d_4 \\ p_3 &= d_1 \oplus d_3 \oplus d_4. \end{aligned} \quad (3)$$

The data and parity check bits are stored and can be recovered later even if there is an error in one of the bits. This is done by recomputing the parity check bits and comparing the results with the values stored. In the example considered, an error on d_1 will cause errors on the three parity checks; an error on d_2 only in p_1 and p_2 ; an error on d_3 in p_1 and p_3 ; and finally an error on d_4 in p_2 and p_3 . Therefore, the data bit in error can be located and the error can be corrected. This is

commonly formulated in terms of the generating G and parity check H matrixes. For the Hamming code considered in the example, those are

$$G = \begin{bmatrix} 1 & 0 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix} \quad (4)$$

$$H = \begin{bmatrix} 1 & 1 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & 1 \end{bmatrix}. \quad (5)$$

Encoding is done by computing $y = x \cdot G$ and error detection is done by computing $s = y \cdot H^T$, where the operator \cdot is based on module two addition (XOR) and multiplication. Correction is done using the vector s , known as syndrome, to identify the bit in error. The correspondence of values of s to error position is captured in Table I. Once the erroneous bit is identified, it is corrected by simply inverting the bit.

TABLE I ERROR LOCATION IN THE HAMMING CODE

$s_1 s_2 s_3$	Error Bit Position	Action
0 0 0	No error	None
1 1 1	d_1	correct d_1
1 1 0	d_2	correct d_2
1 0 1	d_3	correct d_3
0 1 1	d_4	correct d_4
1 0 0	p_1	correct p_1
0 1 0	p_2	correct p_2
0 0 1	p_3	correct p_3

This ECC scheme can be applied to the parallel filters considered by defining a set of check filters z_j . For the case of four filters y_1, y_2, y_3, y_4 and the Hamming code, the check filters would be

$$\begin{aligned}
 z_1[n] &= \sum_{l=0}^{\infty} (x_1[n-l] + x_2[n-l] + x_3[n-l]) \cdot h[l] \\
 z_2[n] &= \sum_{l=0}^{\infty} (x_1[n-l] + x_2[n-l] + x_4[n-l]) \cdot h[l] \\
 z_3[n] &= \sum_{l=0}^{\infty} (x_1[n-l] + x_3[n-l] + x_4[n-l]) \cdot h[l]
 \end{aligned}
 \tag{6}$$

and the checking is done by testing if

$$\begin{aligned}
 z_1[n] &= y_1[n] + y_2[n] + y_3[n] \\
 z_2[n] &= y_1[n] + y_2[n] + y_4[n] \\
 z_3[n] &= y_1[n] + y_3[n] + y_4[n].
 \end{aligned}
 \tag{7}$$

For example, an error on filter y1 will cause errors on the checks of z1, z2, and z3. Similarly, errors on the other filters will cause errors on a different group of z_i. Therefore, as with the traditional ECCs, the error can be located and corrected.

The overall scheme is illustrated on Fig. 2. It can be observed that correction is achieved with only three redundant filters.

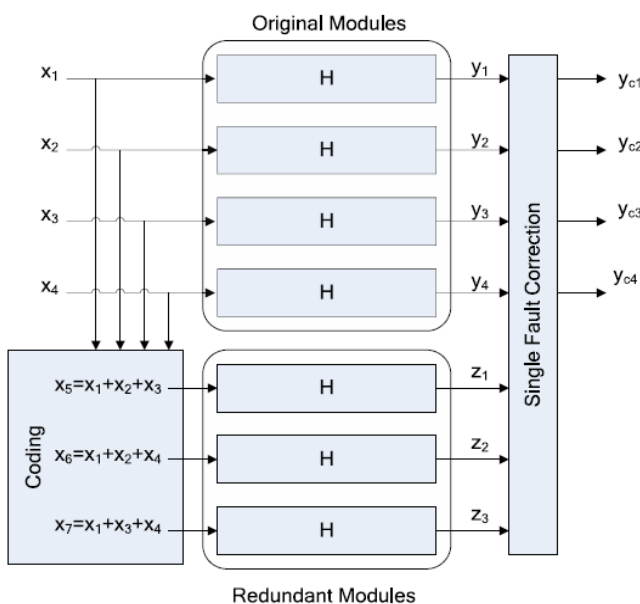


Fig.2. Proposed scheme for four filters and a Hamming code.

For the filters, correction is achieved by reconstructing the erroneous outputs using the rest of the data and check outputs. For example, when an error on y₁ is detected, it can be corrected by making

$$y_{c1}[n] = z_1[n] - y_2[n] - y_3[n]. \tag{8}$$

Similar equations can be used to correct errors on the rest of the data outputs. In our case, we can define the check matrix as

$$H = \begin{bmatrix} 1 & 1 & 1 & 0 & -1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & -1 & 0 \\ 1 & 0 & 1 & 1 & 0 & 0 & -1 \end{bmatrix}
 \tag{9}$$

and calculate $s = y H^T$ to detect errors. Then, the vector s is also used to identify the filter in error. In our case, a nonzero value in vector s is equivalent to 1 in the traditional Hamming code. A zero value in the check corresponds to a 0 in the traditional Hamming code. It is important to note that due to different finite precision effects in the original and check filter implementations, the comparisons in (7) can show small differences.

Those differences will depend on the quantization effects in the filter implementations that have been widely studied for different filter structures. The interested reader is referred to [12] for further details. Therefore, a threshold must be used in the comparisons so that values smaller than the threshold are classified as 0. This means that small errors may not be corrected. This will not be an issue in most cases as small errors are acceptable. The detailed study of the effect of these small errors on the signal to noise ratio at the output of the filter is left for future work. The reader can get more details on this type of analysis in [3]. With this alternative formulation, it is clear that the scheme can be used for any number of parallel filters and any linear block code can be used. The approach is more attractive when the number of filters k is large.

For example, when $k = 11$, only four redundant filters are needed to provide single error correction. This is the same as for traditional ECCs for which the overhead decreases as the block size increases [13]. The additional operations required for encoding and decoding are simple additions, subtractions, and comparisons and should have little effect on the overall complexity of the circuit. This is illustrated in Section IV in which a results and discussion is presented. In the discussion, so far the effect of errors affecting the encoding and decoding logic has not been considered.

The encoder and decoder include several additions and subtractions and therefore the possibility of errors affecting them cannot be neglected. Focusing on the encoders, it can be seen that some of the calculations of the z_i share adders. For example, looking at (6), z_1 and z_2 share the term $y_1 + y_2$. Therefore, an error in that adder could affect both z_1 and z_2 causing a miscorrection on y_2 . To ensure that single errors in the encoding logic will not affect the data outputs, one option is to avoid logic sharing by computing each of the z_i independently. In that case, errors will only affect one of the z_i outputs and according to Table I, the data outputs y_j will not be affected. Similarly, by avoiding logic sharing, single errors in the computation of the s vector will only affect one of its bits. The final correction elements such as that in (8) need to be tripled to ensure that they do not propagate errors to the outputs. However, as their complexity is small compared with that of the filters, the impact on the overall circuit cost will be low. This is confirmed by the results presented in Section IV for a results and discussion.

IV. RESULTS AND DISCUSSION

To evaluate the effectiveness of the proposed scheme, a case study is used. A set of parallel FIR filters with 16 coefficients is considered. The input data and coefficients are quantized with 8 bits. The filter output is quantized with 18 bits. For the check filters z_i , since the input is the sum of several inputs x_j , the input bit-

width is extended to 10 bits. A small threshold is used in the comparisons such that errors smaller than the threshold are not considered errors. As explained in Section III, no logic sharing was used in the computations in the encoder and decoder logic to avoid errors on them from propagating to the output.

Two configurations are considered. The first one is a block of four parallel filters for which a Hamming code with $k = 4$ and $n = 7$ is used. The second is a block of eleven parallel filters for which a Hamming code with $k = 11$ and $n = 15$ is used. Both configurations have been implemented in HDL and mapped to a Xilinx ISE Spartan 3E XC3S500E device. The first evaluation is to compare the resources used by the proposed scheme with those used by TMR, the protection method proposed in [7] (with $m = 7$) and by an unprotected filter implementation. Those results are presented in Tables II and III for each of the configurations considered. It can be observed that the proposed technique provides significant savings (from 26% to 41%) for all the resource types (slices, flip-flops, and LUTs) compared with the TMR. The benefits are larger for the second configuration as expected with values exceeding 40% for all resource types. In that case, the relative number of added check filters $(n - k)/n$ is smaller. When compared with the arithmetic code technique proposed in [7], the savings are smaller but still significant ranging from 11% to 40%. Again, larger savings are obtained for the second configuration. In summary, the results of this results and discussion confirm that the proposed scheme can reduce the implementation cost significantly compared with the TMR and provides also reductions when compared with other methods such as that in [7].

V. SIMULATION RESULTS

All the synthesis and simulation results are performed using Verilog HDL. The proposed circuit has been simulated using Xilinx ISE14.4. The simulation results are shown below figures. Both synthesis and simulation are have been implemented in HDL and mapped to a Xilinx ISE Spartan 3E XC3S500E device.

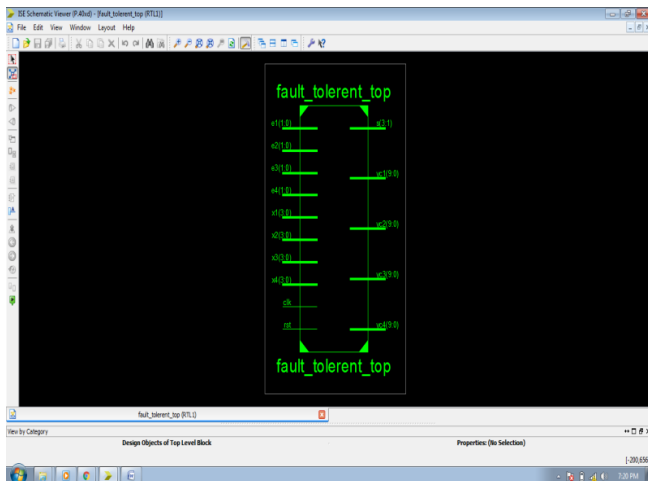


Fig.3: RTL schematic of Proposed Parallel Filters

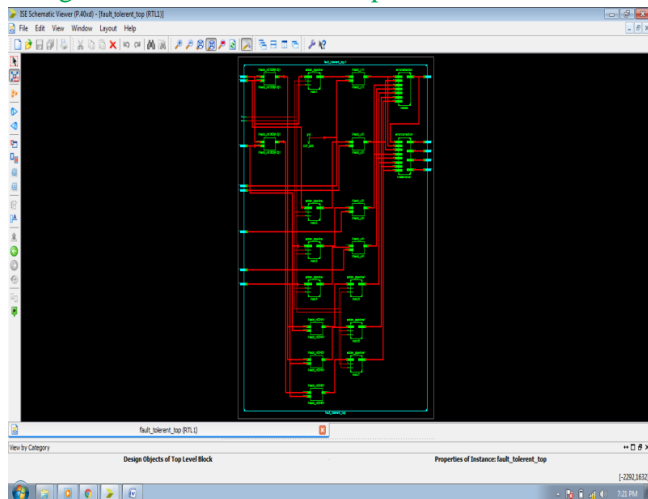


Fig.4: RTL sub schematic of Proposed Parallel Filters

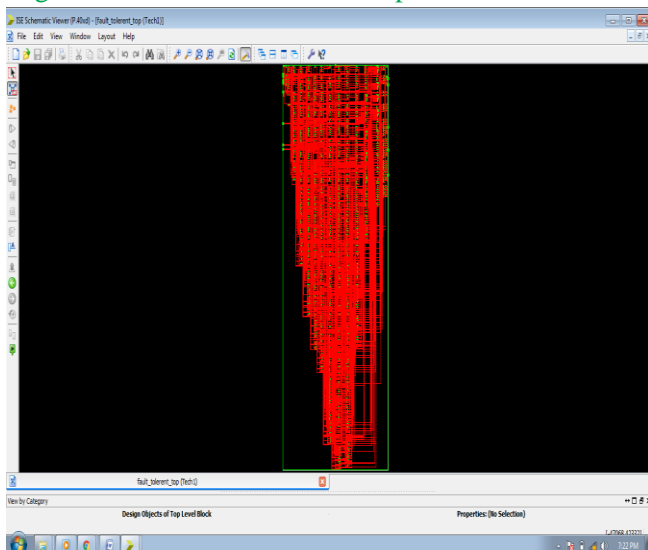


Fig.5: Technology schematic of Proposed Parallel Filters

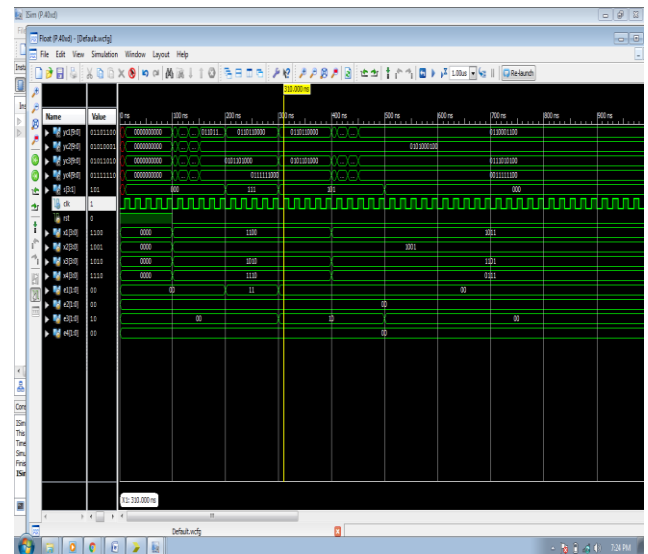


Fig.6: Simulation of Proposed Parallel Filters

VI. CONCLUSION AND FUTURE SCOPE

In this paper, a new scheme to protect parallel filters that are commonly found in modern signal processing circuits. The approach is based on applying ECCs to the parallel filters outputs to detect and correct errors. The scheme can be used for parallel filters that have the same response and process different input signals. A case study has also been discussed to show the effectiveness of the scheme in terms of error correction and also of circuit overheads. The technique provides larger benefits when the number of parallel filters is large. The proposed scheme can also be applied to the IIR filters. Future work will consider the evaluation of the benefits of the proposed technique for IIR filters. The extension of the scheme to parallel filters that have the same input and different impulse responses is also a topic for future work.

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