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A Single-Ended with Dynamic Feedback Control 8T Subthreshold SRAM Cell

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Abstract

Static Random Access Memory (SRAM) has become a major component in many VLSI Chips due to their large storage density and small access time. SRAM has become the topic of substantial research due to the rapid development for low power. SRAM plays a most substantial role in the microprocessor world, but as the technology is scaling down in Nano meters, leakage parameters and delay are the most common problems for SRAM cell which is basically designed for very low power application. A novel 8-transistor (8T) static random access memory cell with improved data stability in sub threshold operation is designed. The proposed single-ended with dynamic feedback control 8T static RAM (SRAM) cell enhances the static noise margin (SNM) for ultralow power supply.

Index Terms—Single ended, static noise margin (SNM), static RAM (SRAM), sub threshold, ultralow power.

Introduction:

The portable microprocessor controlled devices contain embedded memory, which represents a large portion of the system-on chip (SoC). These portable systems need ultralow power consuming circuits to utilize battery for longer duration. The power consumption can be minimized using nonconventional device structures new circuit topologies, and optimizing the architecture. Although, voltage scaling has led to circuit operation in subthreshold regime with minimum power consumption, but there is a disadvantage of exponential reduction in performance [1]. The circuit operation in the Sub threshold regime has paved path toward ultralow power embedded memories, mainly static RAMs (SRAMs) [1], [2]. However, in subthreshold regime, the data stability of SRAM cell is a severe n problem and worsens with the scaling of MOSFET to subnanometer technology. Due to these limitations it becomes difficult to operate the conventional 6-transistor (6T) cell at ultralow voltage (ULV) power supply [1]–[6]. In addition, 6T has a severe problem of read disturb. The basic and an effective way to eliminate this problem is the decoupling of true storing node from the bit lines during the read operation in [2]. This read decoupling approach is utilized by conventional 8-transistor [read decoupled 8-transistor (RD-8T)] cell which offers read static noise margin (RSNM) comparable with hold static noise margin (HSNM) [2]–[4]. However, RD-8T suffers from leakage introduced in read path. This leakage current increases with the scaling thereby, increasing the probability of failed read/write operations. Similar cells that maintain the cell current without disturbing the storage node are also proposed in [4]–[7].

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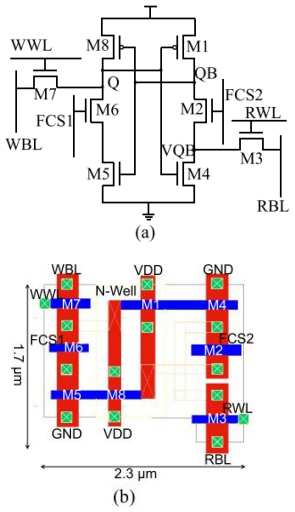

Proposed 8T. (a) Schematic. (b) Layout.

Furthermore, to reduce the power consumption of differential bit line, a single-ended 5T bit cell is attractive due to its reduced area and considerable active and standby power saving capability as compared with conventional 6T SRAM cell [8]. However, writing 1 through an nMOS pass transistor in 5T is a design challenge. Another problem is to obtain optimized noise margin against process variations at all operations. In addition, the read stability of single ended 5T severely degrades in comparison with conventional 6T SRAM cell [8]. Various approaches like boosted supply (gate voltage of access transistor M5 is greater than VDD) generated from an additional circuit [8], gated-feedback write assist [9], 7T dual VTH [10], asymmetrical write/read-assist 8T [11], and cross-point data-aware 9T [12] have been proposed to mitigate the above issues associated with 5T. Still, none of the cell could fulfill the requirement of improving both read and write stability in subthreshold regime for ultralow power applications. In this brief, we have designed a new subthreshold 8T SRAM cell that operates in subnanometer technology node at ULV. This 8T SRAM cell uses single-ended write with dynamic feedback cutting to enhance write ability and dynamic read decoupling to avoid read disturb [12]–[16]. Due to read decoupled mechanism, the 9T cell [16] improves the RSNM by 4.1× as compared with conventional 6T cell. The 9T cell not only has larger write margin (WT) but also has faster write time [16]. As 8T is single-ended it can save more power consumption and area as compared with [16]. Here, we focus mainly on the stability of the cell which is affected by the process parameter variations. This brief is an elaborate discussion of our previous work [15] on 8T, including comparisons with other single-ended cells like conventional 5T and 8T [11]. We have also emphasized on delay, power and half-select issues for both row and column. Apart from this, a 1-kb SRAM array for proposed 8T and conventional 6T was also designed. The circuit simulations are done in United Microelectronics Corporation (UMC) 90-nm process technology at different power supplies.

PROPOSED 8T SRAM CELL DESIGN

To make a cell stable in all operations, single-ended with dynamic feedback control (SE-DFC) cell is presented in Fig. 1(a). The single-ended design is used to reduce the differential switching power during read–write operation. The power consumed during switching toggling of data on single bit line is lesser than that on differential.

A. Cell Layout

For comparison of area, layout of 5T, 6T, RD-8T, and proposed 8T are drawn in Microwind and DSCH3.5 CMOS technology, as shown in Table I. The sizes of MOSFETs used in proposed 8T cell are depicted in Fig. 1(b). The RD-8T occupies area as compared with that of 6T. Due to the design constraints and contact area between M2, M3, M4, and M8 for proposed 8T, there is area overhead as compared with 6T cell. Even though it has 2× area of 6T, but its better built-in process tolerance

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and dynamic voltage applicability enables it to be employed similar to cells with area overhead [3]–[7].

B. Write Operation

The feedback cutting scheme is used to write into 8T. In this scheme, during write 1 operation FCS1 is made low which switches OFF M6. When the RWL is made low and FCS2 high, M2 conducts connecting Complementary Q (QB) to the ground. Now, if the data applied to word bit line (WBL) is 1 and WWL is activated (Table II), then current flows from WBL to Q and creates a voltage hike on Q via M7-writing 1 into the cell. Moreover, when Q changes its state from 0 to 1, the inverter (M1– M2–M4) changes the state of QB from 1 to 0. To write a 0 at Q, WWL is made high, FCS2 low and WBL is pulled to the ground. The low going FCS2 leaves QB floating, which can go to a small negative value, and then the current from pull-up pMOS M1 charges QB to 1. The WT is measured as the time taken by WWL signal-to-rise to VDD/2 until the storage nodes intersect each other. The simulations for WT were performed at all process corners. The WT (for write 1 and write 0) for 8T increases (Fig. 3) with the decrease in power supply. The WT is highest for slow nMOS and slow pMOS (SS) worst case corner, as shown in Fig. 3(a) and (b). During write 1/0 operation, the power consumption of 8T is highest for fast nMOS and fast pMOS (FF) process corner dominated by the fast switching activities (Fig. 4). As write 0 operation is faster than write 1, the write 0 power consumption during write 0 is more as compared with that of write 1 [Fig. 4(a) and (b)].

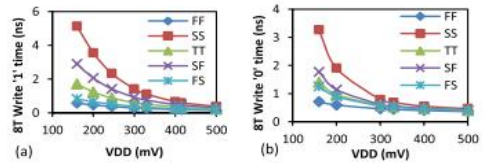

Fig. 3. (a) Write 1 time of 8T. (b) Write 0 time of 8T.

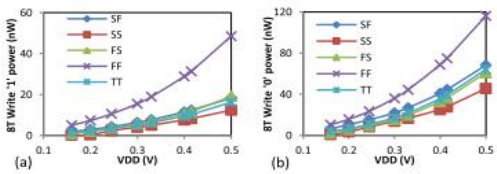

Fig. 4. (a) Write 1 power of 8T. (b) Write 0 power of 8T.

C. Read Operation

The read operation is performed by precharging the RBL and activating RWL. If 1 is stored at node Q then, M4 turns ON and makes a low resistive path for the flow of cell current through RBL to ground. This discharges RBL quickly to ground, which can be sensed by the full swing inverter sense amplifier. Since WWL, FCS1, and FCS2 were made low during the read operation (Table II), therefore, there is no direct disturbance on true storing node QB during reading the cell. The low going FCS2 leaves QB floating, which goes to a negative value then comes back to its original 0 value after successful read operation. If Q is high then, the size ratio of M3 and M4 will govern the read current and the voltage difference on RBL. During read 0 operation, Q is 0 and RBL holds precharged high value and the inverter sense amplifier gives 0 at output. Since M2 is OFF so virtual QB (VQB) is isolated from QB and this prevents the chance of disturbance in QB node voltage which ultimately reduces the read failure probability and improves the RSNM. During read operation, if FCS1/FCS2 turns 1 before RWL is turned 0 then QB and VQB can share charge. As WWL is 0 no strong path exists between WBL and Q, and any disturbance in QB will not affect Q. After that if RWL goes low, the positive feedback will restore the respective states (Q = 1 and QB = 0).

The read time is measured as the time the RWL signal is activated until the RBL is discharged to 90%. The SS process corner shows maximum read time, as shown in Fig. 5(a). It is followed by the SF corner and then by the other process corners. Similar to write power, the FF process corner condition draws the highest read power. While read power consumption at other process corners closely follows for different power supplies [Fig. 5(b)].

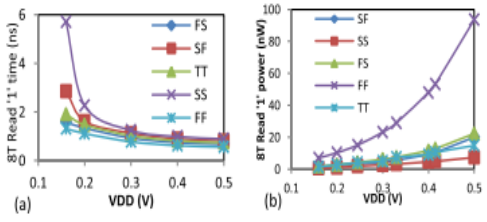

Fig. 5. (a) Read 1 time. (b) Read 1 power of 8T.

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D. Half-Selected Issue

Whenever a cell is selected for write operation, the voltage of true storage node (Q) of row half-selected cells will rise due to charge transfer from WBL [Fig. 6(a)]. The complementary storage node QB does not have strong connection to the bit line (RWL is OFF) (Table II), and therefore, less chances to flip the cell as compared with conventional 6T/RD-8T cell. This can be verified by 1000 Monte Carlo (MC) simulations, as shown in Fig. 6(a). Similarly, during read operation [Fig. 6(b)], the 1000 MC simulations show leakage immunity in row half-selected cells.

TABLE II
OPERATION TABLE OF PROPOSED 8T SRAM CELL

	Hold	Read	Write '1'	Write '0'	Row half-selected		Column half-selected	
					Write	Read	Write	Read
WWL	'0'	'0'	'1'	'1'	'1'	'0'	'0'	'0'
RWL	'0'	'1'	'0'	'0'	'0'	'1'	'0'	'0'
FCS1	'1'	'0'	'0'	'1'	'1'	'1'	'1'	'0'
FCS2	'1'	'0'	'1'	'0'	'1'	'1'	'0'	'0'
WBL	'1'	'1'	'1'	'0'	'1'	'1'	'1'	'1'
RBL	'1'	Dis-charge	'1'	'1'	'1'	'1'	'1'	'1'

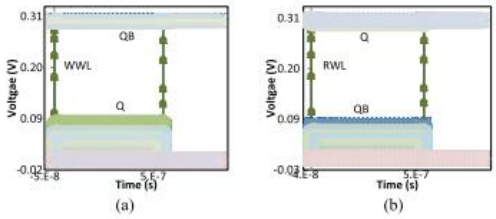

Fig. 6. Thousand MC simulations of row half-selected 8T. (a) Write. (b) Read.

The control signals (FCS2 and FCS2) are common for all the cells connected in a column and during write operation of a cell, the other cells in same column will retain the data successfully. When column half-selected cells QB is 0 and FCS2 goes low (write 0 operation in selected cell in same column), then, QB will be floating for write period. The parasitic and gate capacitance of the transistors M5 and M8 connected to the true storage node QB of column half-selected cells will hold the data during write operation for selected cell [Fig. 7(a)]. The pulsewidth needed for write operation is very small as compared with the data retention time (in microseconds) of half-selected cells while, FCS2 is OFF to write 0 in selected cell. During read operation, FCS1 and FCS2 go low (Table II) in whole column and QB of column half-selected cell will be floating for read period. There is a small variation in the floating QB because of weak driving currents from power supply charging it, as shownin Fig. 7(b). The column half-selected cells can retain the data successfully even if the write/read or FCS1/FCS2 period greater than the required. To verify leakage immunity, 1000 MC simulations were performed during write [Fig. 7(a)] and read [Fig. 7(b)] operations.

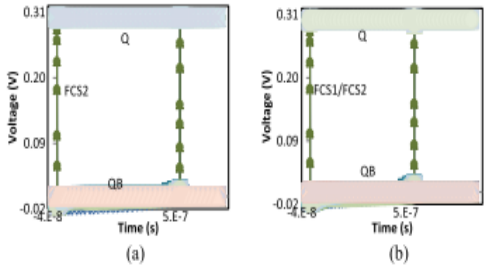

Fig. 7. 1000 MC simulations of column half-selected 8T. (a) Write. (b) Read.

E. Control Signal Generation

The feedback control signals, namely, FCS1 and FCS2 are data dependent. These signals connected in column-wise configuration [14]–[16]. Input data and column address signals are used to generate these control signals.

A common circuit is used for a single column, therefore, there would be a small area overhead at array level. The proposed 8T cell has single-ended read port (as conventional read decoupled RD-8T), and therefore, the number of cells per bit line would be smaller as compared with differential 6T. Due to small length RBL the parasitic capacitances are less and the delay/power in read/write operation would not be affected significantly. The operation of proposed cell is based on the conditions of word lines, bit lines, and control signals, as shown in Table I.

TABLE I
LAYOUT AREA IN UMC 90-nm TECHNOLOGY

	5T	6T	RD-8T	8T
Area (μm^2)	1.2	1.4	2.1	3.9
Area/(5T area)	1x	1.16x	1.75x	3.2x

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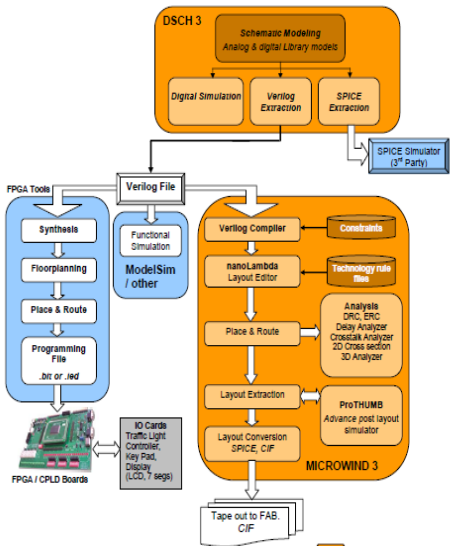
TABLE VI
COMPARISON OF SNM WITH [6] AND [7] AT 300 mV AND 25 °C

UMC 90nm	SNM (Monte Carlo analysis)	μ (mV)	σ (mV)
Proposed 8T	HSNM (FS corner)	89.57	5.44
	RSNM (FS corner)	70.33	5.98
	WSNM (SF corner)	227.29	7.00
10T cell [6]	HSNM (FS corner)	130	8.6
	RSNM (FS corner)	43.1	13
	WSNM (SF corner)	38.5	28.2
10T cell [7]	HSNM (FS corner)	74.2	11.4
	RSNM (FS corner)	84.3	9.2
	WSNM (SF corner)	44.5	13.3

MICROWIND TOOL DESIGN FLOW



Integrated circuits have changed the way of our life. You name one gadget and will find the power of silicon which has made such complex electronic circuits possible. Integrated circuits come in many different flavors these days. User designed chips in particular , CPLDs and FPGAs have revolutionized the way of system design. But ASIC remains in lead, due to their speed, power and performance advantages. Every critical system design is flagged with ASICs. To learn the IC design process, techniques & 'critical' requirement handling, engineers practice for hours and hours.on EDA tools to master know-how of design fundamentals.

The n-channel MOS device requires a logic value 1 (or a supply VDD) to be on. In contrary, the p-channel MOS device requires a logic value 0 to be on. When the MOS device is on, the link between the source and drain is equivalent to a resistance. The order of range of this 'on' resistance is 100Ω-5KΩ. The 'off' resistance is considered infinite at first order, as its value is several MΩ.

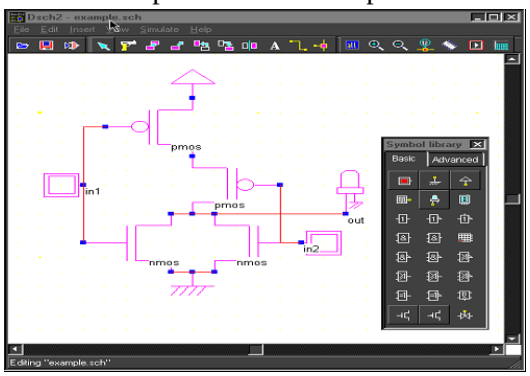
4THREE LEVELS OF DESIGN IN MICROWIND AND DSCH

- The specifications we are going to see may be different for different foundry and technology.
- Design Example (3 Levels): NOR Gate

– Logic Design
– Circuit Design
– Layout Design

Microwind / DSCH NOR Example: NOR Gate Logic

- Open the Schematic Editor in Microwind (DSCH3). Click on the transistor symbol in the symbol Library on the right.
- Instantiate NMOS or PMOS transistors from the symbol library and place them in the editor window.
- Instantiate 2 NMOS and 2 PMOS transistors.
- Connect the drains and sources of transistors.
- Connect Vdd and GND to the schematic.
- Connect input button and output LED.



Now we have NOR schematic ready.

- Use your logic simulator to verify the functionality of your schematic.
- The next step is to simulate the circuit and check for functionality.
- Click on, Simulate -> Start simulation.
- This brings up a Simulation Control Window.

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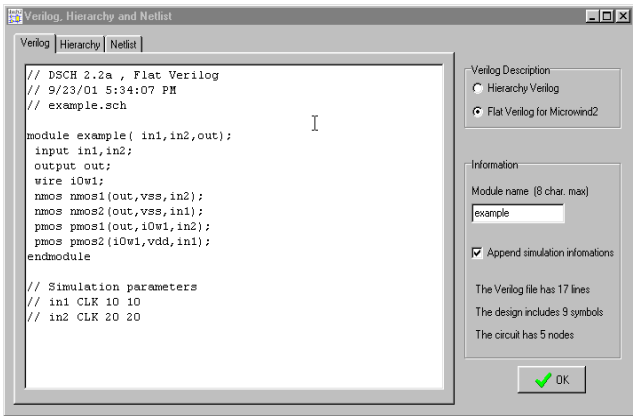
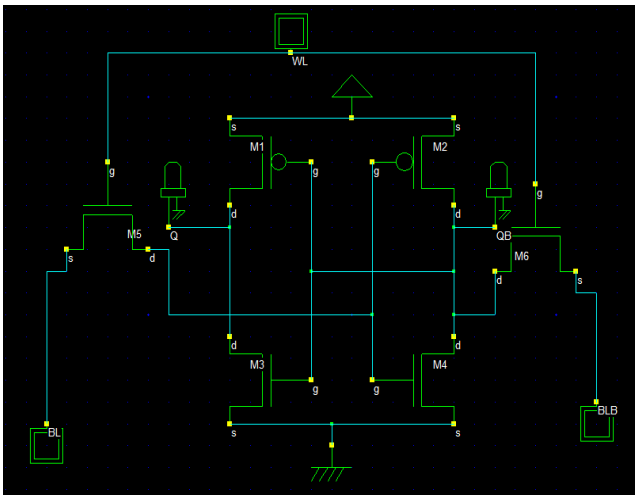
- Click on the input buttons to set them to 1 or 0. Red color in a switch indicates a '1'. As shown,

Simulate your system with your hand calculated transistor sizes. Click File -> Make Verilog File. The Verilog, Hierarchy and Netlist window appears. This window shows the verilog representation of NOR gate. Click OK to save the Verilog as a .txt file.

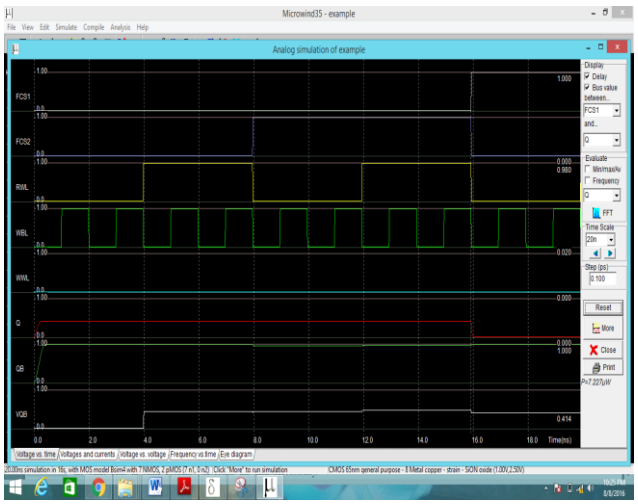


SIMULATION RESULTS

All the simulations are performed on Microwind3.5 and DSCH3.5. The main focus of this work is to meet all challenges faces in designing of memory circuit at Nano scale technology, where deviations arises due to process and environmental parameters such as operating voltage and temperature. A novel 8-transistor (8T) static random access memory cell with improved data stability in subthreshold operation is designed. The simulation results are shown below figures.



Schematic of 6T SRAM cell



Simulation of Layout of 8T SRAM cell

CONCLUSION

An 8T SRAM cell with high data stability (high μ and low σ) that operates in ULV supplies is presented. We attained enhanced SNM in subthreshold regime using SE-DFC and read decoupling schemes. The proposed cell's area is twice as that of 6T. Still, it's better built-in process tolerance and dynamic voltage applicability enables it to be employed similar to cells (8T, 9T, and 10T) along with area overhead. The proposed 8T cell has high stability and can be operated at ULV of 200–300 mV power supplies. The advantage of reduced power consumption of the proposed 8T cell enables it to be employed for battery operated SoC design. Future and applications of the proposed 8T cell can potentially be in low/ULV and medium frequency operation like neural signal processor, subthreshold processor, wide-operating-range IA-32 processor, fast Fourier transform core, and low voltage cache operation.

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