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# A Novel Design of Reversible Combinational and Sequential Circuits Using Mach Zehnder Interferometer (MZI) Switch

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## ABSTRACT:

Reversible computing offers a possible solution for high performance computing and low power consumption. For hardware implementation of reversible logic, optical computers are emerging as one of the promising alternative. Recently, reversible logic gates and combinational circuits have been proposed in optical domain using Semiconductor Optical Amplifier (SOA) based Mach Zehnder interferometer (MZI) switches due to its significant advantages such as high speed, low power, fast switching and ease of fabrication. In this work, an optical reversible MNOT gate and all-optical realization of 4×4 Toffoli Gate have been proposed which is used in all-optical realization of optimized reversible combinational circuits. A general design approach to realize all-optical reversible circuits based on MZI switches has been proposed first time in the literature. Optimized all-optical reversible 2×1 multiplexer and full adder circuits have been designed using these proposed gates and design approach. All-optical reversible designs of 4×1 multiplexer, 1×4 De-multiplexer and 3to8 Decoder circuits have also been presented. We are extending this project for all optical reversible sequential circuits. Our results have shown significant improvements over existing designs in terms of MZI switches and optical delay.

**Keywords:**
Optical Reversible computing; Mach-Zehnder Interferometer(MZI); Full Adder; Multiplexer; Decoder; Flip Flops; Counters; optical cost.

## I. INTRODUCTION:

The growing technologies have increased the demand of high performance computing. According to G. Moore's low [1], number of transistor counts to be integrated per unit area in devices will almost double in one and half year. To achieve high speed computation, high packaging density in the logic circuits is required which results in more heat dissipation. The conventional computing is found unable to deal with low power, high compaction and heat dissipation issues of the current computing environment. In 1961, R. Laundaur [2] stated that heat dissipation occurs due to energy loss in irreversible logics. Each bit of information dissipates an amount of energy equal to KTln2 joules where K is Boltzmann's Constant and T is the absolute temperature. In 1973, C. H. Bannett [3] stated that reversible logic can overcome the heat dissipation problem of VLSI circuits because the bits of information are not erased in reversible computing. New technologies are emerging to deal with these issues. Reversible Computing is one way to overcome the problem of heat dissipation in computing chips which in turn help in increasing the packaging density. Reversible Logic seems to be hopeful due to its wide application in emerging technologies such as quantum computing, optical computing and power efficient nanotechnologies etc. Reversible circuits do not lose information. A reversible logic gate has one to one mapping between input and output vectors i.e. number of input lines are equal to number of output lines in the reversible gate [12], [14]. Fan-out is not permitted in the reversible logic.

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Constant inputs and garbage outputline can be added to the circuit to make it reversible[12], [13], [14]. Optical Computing is computation with photon as opposed to conventional electron based computation. Unmatched high speed and zero mass of photon have attracted the researchers towards the optical realization of reversible logic gates using Semiconductor Optical Amplifier (SOA) based Mach Zehnder Interferometer (MZI) switches. MZI Switches are preferred because of its high speed, fast switching, low power and ease in fabrication [4], [5], [6]. The authors have presented the optical realization of popular reversible logic gates such as Feynman and Toffoli Gates [4], Fredkin Gate [5], and Peres Gate [6] etc. All-optical reversible combinational circuits for instance 2×1 Multiplexer [7], Binary Ripple Carry Adder [8], NOR Gate [9], New Gate [10], Hybrid New Gate (HNG) [11] and Modified Fredkin Gate [15] etc. are proposed by the authors in the literature.

In this paper, we have proposed an optical reversible MNOT gate using one MZI switch. All-optical realization of 3×3 Toffoli Gate, 4×4 Toffoli Gate has been presented which is used in alloptical realization of optimized reversible combinational circuits. A general design approach to realize all-optical reversible circuits based on MZI switches has been proposed first time in the literature. Optimized all-optical reversible 2×1 multiplexer and full adder circuits have been designed using these proposed gates and design approach. All-optical reversible designs of 4×1 multiplexer, 1×4 D e-multiplexer and 3to8 Decoder circuits have also been prese nted in this work first time in the literature. Our results have shown significant improvements over existing designs in terms of MZI switches, BS, BC and optical delay.Till date, insufficient number of works on reversible memory element has been reported. Some preliminary works on the reversible implementation of latches, flipflops, shift register, counters using quantum technology have been reported. We have reviewed works where all optical functionally reversible gates are designed by various researchers.

Getting inspired by the existing works in the domain of reversible implementation of sequential circuits, after several investigations we have focused on the designing of all optical implementation of reversible counters.

## II.BASICS OF ALL OPTICAL REVERS IBLE LOGIC:

Reversible logics are implemented with optical technology using some building blocks such as MZI based optical switch, beam splitter and beam combiner.

### A. SOA Based MZI Switch:

An SOA based MZI switch can be designed using two Semiconductor Optical Amplifiers (SOA-1, SOA-2) and two couplers (C -1, C-2) [8], [9]. In an MZI switch, there are two inputs ports A and B, and two output ports called bar port and cross port, respectively, as shown in Figure 1 and 2.

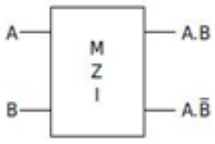


**Fig.1. Block diagram of Mach-Zehnder Interferometer switch [8]**

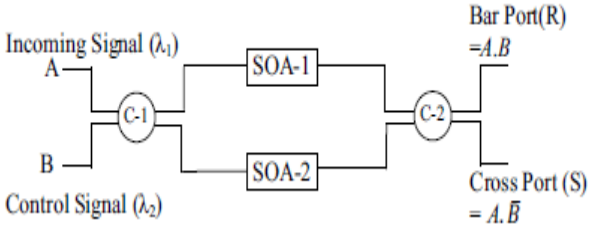


**Fig.2. SOA based Mach-Zehnder Interferometer switch [8]**

The optical signal at port B is termed as the control signal and signal at port A is termed as incoming signal. When there are signals present at port A and port B then there is a presence of light signal at the bar port an d absence of light signal at the cross port. In the absence of co ntrol signal at port B and presence of incoming signal at port A, the outputs of MZI are

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interchanged and results in the presence of light at the cross port and no light at the bar port. Here, absence of light is considered as the logic value 0 and p resence of light is considered as logic value 1. This behavior of SOA based MZI switch can be written as Boolean functions having inputs to outputs mapping as (A, B) → (P=A.B, Q = A.B ), where A, B are the inputs and P, Q are the outputs of MZI, respectively. The optical cost and the delay ( ) of MZI based all optical switch is considered as unity. The authors have considered the following optimization parameters for the all-optical reversible logics: optical cost i.e. number of MZI switches, number of BC and BS used in the logic circuit, and optical delay i.e. number of stages of MZI switches used in the design of logic circuit.

### All-Optical Feynman Gate:

The Feynman gate (FG) has mapping (A, B) → (P=A, Q=A⊕B) where A, B are the inputs and P=A, Q=A⊕B are the outputs, respectively. The Feynman gate can be realized using 2 MZI switches, 2 bea m combiners (BC) and 3 beam splitters (BS) in all optical dom ain as shown in figure 3 [4].

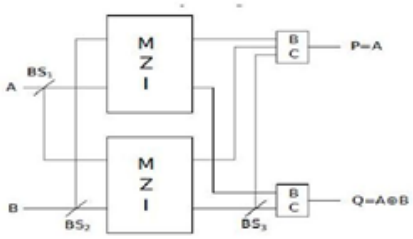


**Fig. 3. Feynman gate and its all-optical implementation [4]**

## III.PROPOSED ALL-OPTICAL REVERSIBLE LOGIC GATE:

We have proposed a new M NOT gate and presented an all-optical realization of 4×4 Toffoli Gate which are efficient to design optimized optical reversible circuits.

### A. Proposed all-optical reversible MNOT Gate:

A new 2×2 all-optical reversible MNOT gate (1, A) → (P, Q) has been proposed, where P =A and Q = A . Figure 4 shows the Block diagram of M NOT gate.

This gate generates logical NOT of the input logic A. Table I shows the truth table of MNOT gate.

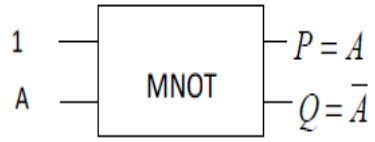


**Fig. 4. Block diagram of Proposed 2×2 MNOT gate**

**TABLE I TRUTH TABLE OF THE PROPOSED REVERSIBLE GATE:**

| Input | | Output | |
|---|---|---|---|
| *1* | *A* | $P = A$ | $Q = \bar{A}$ |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

The all-optical reversible MNOT gate has been shown in figure 5. This gate is designed with single MZI switch. The incoming signal of MZI switch is set to 1 then output generated at cross port is inverse of the input at control signal.The optical cost of MNOT gate is one. NO Beam Splitter (BS) or Beam Combiner (BC) is used in this gate. As only one MZI switch is used, so the delay is 1Δ.

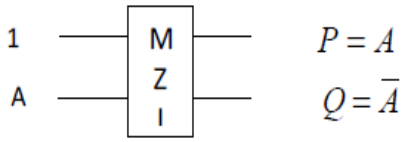


**Fig. 5. Proposed 2×2 Optical Reversible MNOT gate**

The optical MNOT gate is a useful logic gate in all-optical reversible circuit realization. Earlier the authors has used Feynman gate to generate inverse of logic with optical cost 2 MZI switches. Using this gate cost has been reduced to one MZI switch.

### B.Optical Realization of 3x3, 4×4 Toffoli Gates:

The 4×4 Toffoli Gate (4×4 TG) is mapped from input vector (A, B, C, D) to output vector (P, Q, R, S), where P=A, Q=B, R=C, and S=D ⊕ABC, respectively.

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Basically, 4×4 Toffoli gate is Multiple Controlled Toffoli gate (MCT) with 3.

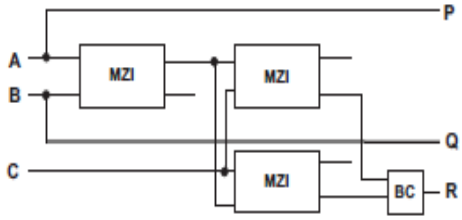


**Fig. 6. All-optical Realization of 3×3 Toffoli gate**

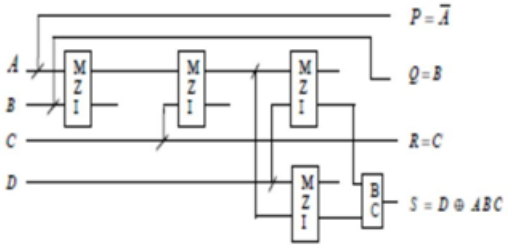


**Fig. 7. All-optical Realization of 4×4 Toffoli gate**

control lines. Figure 6 shows and Figure 7 Shows the all -optical realization of 3x3,4×4 Toffoli gates. The 4x4 Toffoli gate has been realized with 4 MZI Switches, Five Beam splitters (BS) and one Beam Combiners (BC). The optical delay of this gate is considered as 3Δ.

## IV.PROPOSED ALL-OPTICAL REVERSIBLE LOGIC CIRCUITDESIGNS

### A. Proposed All-optical Reversible 2×1 Mūltiplexer

This section describes the design and realization of the reversible 2×1 Multiplexer in all-optical domain using the proposed MNOT gate and optical Toffoli Gate (TG) [4]. It has two data inputs ($D_0$ and $D_1$), a single output O and a select line $S_0$ to select one of the two input data lines. The output function of 2×1 Multiplexer is given by $O = S_0D_0+S_0D_1$ .The truth table of 2×1 Multiplexer is shown in table II. The optical realization of 2×1 Reversible Multiplexer is shown in figure 8. It is designed with one MNOT and two TG gates. Here, MNOT gate behaves as NOT gate. When the third input line of TG is set to Constant 0 (Zero), the TG behaves as AND gate.

**TABLE II TRUTH TABLE OF 2×1 MULTIPLEXER:**

| Input | | | Output |
|---|---|---|---|
| $D_0$ | $D_1$ | $S_0$ | O |
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

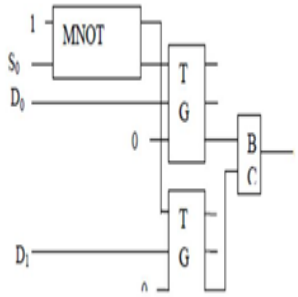


**Fig. 8. Optical Realization of 2×1 Reversible Multiplexer**

The MNOT gate is made of 1 MZI Swit ch. No BS and BC are used in the design of MNOT gate. The TG is made of 3 MZI Switches, 4 BS and one BC [4]. The delay of MNOT gate is 1Δ and that of TG is 2Δ. Thus, total optical cost of Optical Reversible 2×1 Multiplexer is 7 MZI Switches; total Beam splitters used are 8; beam Combiners used are 3 and Delay of the multiplexer circuit is calculate d as 3Δ as the two TG are working in parallel. It can be observ ed that optical cost of the Optical Reversible 2×1 Multiplexer h as been improved significantly in compare to existing one [7] which was implemented using 8 MZI switches, 12 Beam splitters, 5 Beam combiners, and optical delay 3Δ.

### B. Proposed All-optical Reversible Full Adder Circuit:

This section describes a design of all-Optical reversible full Adder circuit using two existing all-Optical Reversible Logic gates with improved Optical cost.

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The truth table of the full adder circuit is shown in the table III. The output functions of Full Adder circuit are given as follows:

$S = A \oplus B \oplus C$ ; $C_{out} = AB + (A \oplus B) C$

**TABLE III TRUTH TABLE OF THE FULL ADDER CIRCUIT**

| Input | | | Output | |
|---|---|---|---|---|
| *A* | *B* | *C* | *S* | $C_{out}$ |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

The new improved Optical Reversible F ull Adder circuit is designed using two existing all-optical reversible logic gates; One is Optical Feynman Gate which is mapped as (A, B) → (P,Q) where P=A and Q=A⊕B, and another is ORG-I [8] which is mapped as (A, B, C) → (P, Q, R ) where P=AB+(A⊕B)C,Q=A⊕B and

$$R = A\bar{B} + \overline{(A \oplus B)}C.$$

The ORG-I gate is shown in the Figure 9. T he improved all-optical reversible full adder is shown in the figure 10. Input bit A, B and C are passed at three inputs of the ORG -I gate. The output P of ORG-I implements the output carry function of Full adder; Output Q of ORG-I and input C are passed to input lines of Feynman gate which produces output Sum Function of Full Adder.

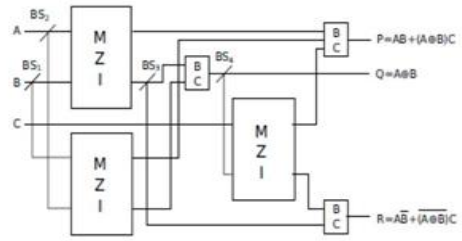


**Fig. 9. Optical Reversible Gate (ORG)-I [8]**

The ORG-I has 3 MZI switches, 4 BS and 3 BC with optical delay as 2Δ. The Feyn man Gate is realized with 2MZI switches, 3 BS, 2 BC and optical delay is 1Δ . Thus, it can be observed from the figure that All-Optical Reversible Full Adder is realized with 5 MZI switches, 8 Beam Splitters and 5

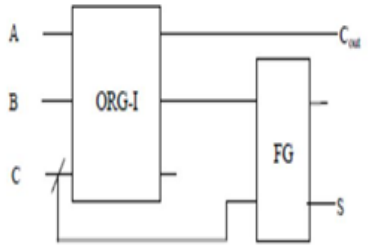


**Fig. 10.The improved All- Optical Reversible Full Adder**

Beam Combiners. The optical delay is considered as 3Δ. It can be seen that the optical cost of the All-Optical Reversible Full Adder Circuit is improved significantly compared to the existing design of Full adder circuit [8] in terms of MZI switches and Beam Combiners.

### B.1. 4-bit Optical Reversible Full Adder Circuit:

A 4 -bit optical reversible full adder circuit is designed using 4 ORFA (optical reversible full adder). The diagram of the 4-bit optical reversible full adder is shown in the Figure 11. The carry output of first ORFA is passed to carry input of second ORFA, carry output of second ORFA is passed to carry input of third ORFA and so on. Finally the carry output line of the fourth ORFA produces output carry of addition of two 4-bit numbers. The sum output line of all he ORFA collectively produces 4-bit sum of two 4-bit numbers.

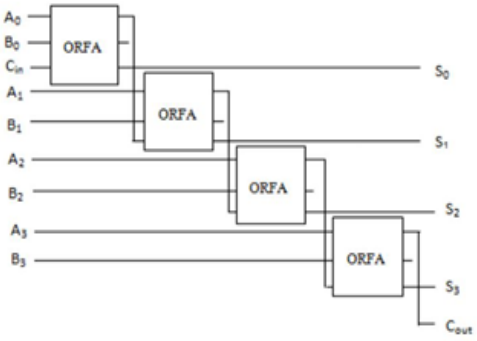


**Fig. 11. 4-bit Optical Reversible Full Adder Circuit**

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Optical cost of the circuit is 20 MZI switches as each ORFA is designed with 5 MZI switches, 8 Beam Splitters and 5 Beam Combiners. Thus, total 32 BS and 20 BC are used in the design of 4-bit optical reversible full adder. The optical delay of the circuit is 12Δ.

### C. Design of Optical Reversible 4×1 Multiplexer:

This is first attempt in the literature for designing all-Optical Reversible 4×1 multiplexer circuit. The all-optical Reversible 4×1 Multiplexer circuit has been realized with proposed Optical Reversible MNOT gate and Optical 4×4 Toffoli Gate (4×4 TG). It has four data input lines ($D_0$-$D_3$), two selection lines $S_0$ and $S_1$ to select one of the four inputs and a single output line O. the expression for data output O is given as

$$O = D_0\overline{S}_0\overline{S}_1 + D_1S_0\overline{S}_1 + D_2\overline{S}_0S_1 + D_3S_0S_1$$

The truth table of 4×1 Multiplexer is shown in table IV .The optical realization of the 4×1 Reversible Multiplexer is shown in the figure 12. It is designed using two MNOT gates and four optical 4×4 TG gates. The fourth input lines of all the 4×4 TG are set to constant 0, which results in Logical AND of the remaining three inputs at fourth output line of 4×4 TG. The fourth output lines of all the 4×4 TG are combined using Beam Combiner (BC) at the final output. The MNOT gate is designed with 1 MZI Switch. No BS and BC are used in the design of MNOT gate.

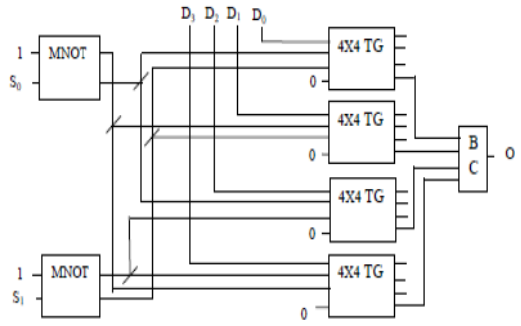


**Fig. 12. Design of 4×1 Optical Reversible Multiplexer**

**TABLE IV THE TRUTH TABLE OF 4×1 MULTIPLEXER**

| Input | | Output |
|---|---|---|
| $S_1$ | $S_0$ | $O$ |
| 0 | 0 | $D_0$ |
| 0 | 1 | $D_1$ |
| 1 | 0 | $D_2$ |
| 1 | 1 | $D_3$ |

The 4×4 TG is realized with four M ZI Switches, Five Beam splitters (BS) and one Beam Combiners (BC). The delay of this gate is considered as 3Δ. Thus, the optical cost of the all -optical 4×1 Reversible Multiplexer circuit comes out to be 18 MZI Switches, 24 BS, 5 BC. The delay is calculated 4Δ as two MNOT gates as well as four 4×4 T G are working in parallel.

### D. Design of Optical Reversible 1×4 De-Multiplexer:

Authors, in the literature, have not yet designed any single Reversible 1×4 De-Multiplexer in optical domain. This is first time, an All -optical Reversible 1×4 De-Multiplexer has been proposed. It has one input data line D, 2 select input lines ($S_0$ and $S_1$) and four output lines ($O_0$- $O_3$). The truth table of 1×4 De-Multiplexer is shown in table V. The expression for output lines are given as follows:

$$O_0 = D\overline{S}_1\overline{S}_0, O_1 = D\overline{S}_1S_0, O_2 = DS_1\overline{S}_0 \text{ and } O_3 = DS_1S_0$$

For optical realization of Reversible 1×4 De-Multiplexer, transformation based approach is used. The Optical Reversible 1×4 De-Multiplexer is designed with optical MNOT gate and optical 4×4 TG gates. The logical NOT Gate and the logical AND are replaced with proposed optical reversible MNOT gate and 4×4 TG, respectively. Optical realization is shown in Figure 13.

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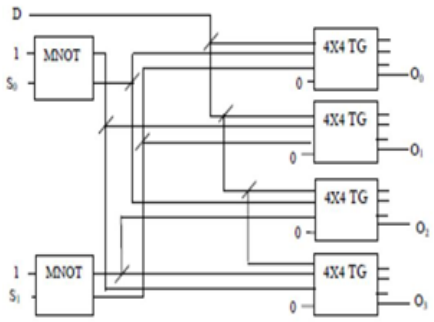


**Fig. 13. Optical realization of reversible 1×4 De-Multiplexer**

It can be observed that 2 optical MNOT gates and four 4×4 TG gates have been used in optical realization of 1×4 De-Multiplexer. This circuit is designed using 18 MZI Switches, 27 Beam Splitters and 4 Beam Combiners. Two MNOT Gates as well as four 4×4 TG are connected in parallel. Thus, Delay is calculated as 4Δ.

### TABLE V TRUTH TABLE OF 1×4 DE-MULTIPLEXER

| Input | | Output | | | |
|---|---|---|---|---|---|
| $S_1$ | $S_0$ | $O_3$ | $O_2$ | $O_1$ | $O_0$ |
| 0 | 0 | 0 | 0 | 0 | D |
| 0 | 1 | 0 | 0 | D | 0 |
| 1 | 0 | 0 | D | 0 | 0 |
| 1 | 1 | D | 0 | 0 | 0 |

### E. Design of Optical Reversible 3to8 Decoder:

A Decoder circuit is similar to the De- Multiplexer circuit but there is no data input line. This is also first time attempt in the literature to design an all- Optical Reversible 3to8 Decoder circuit. A 3to8 Decoder has three input li nes (P, Q, R) and eight output lines ($O_0$ - $O_7$). The truth table of 3to8 decoder has been given in table VI. The output function of the 3to8 Decoder is expressed as follows:

$$O_0 = \bar{P}\bar{Q}\bar{R}\ ;\ O_1 = \bar{P}\bar{Q}R\ ;\ O_2 = \bar{P}Q\bar{R}\ ;\ O_3 = \bar{P}QR$$

$$O_4 = P\bar{Q}\bar{R}\ ;\ O_5 = P\bar{Q}R\ ;\ O_6 = PQ\bar{R}\ ;\ O_7 = PQR$$

### TABLE VI TRUTH TABLE OF 3TO8 DECODER

| Input | | | Output | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| $P$ | $Q$ | $R$ | $O_0$ | $O_1$ | $O_2$ | $O_3$ | $O_4$ | $O_5$ | $O_6$ | $O_7$ |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

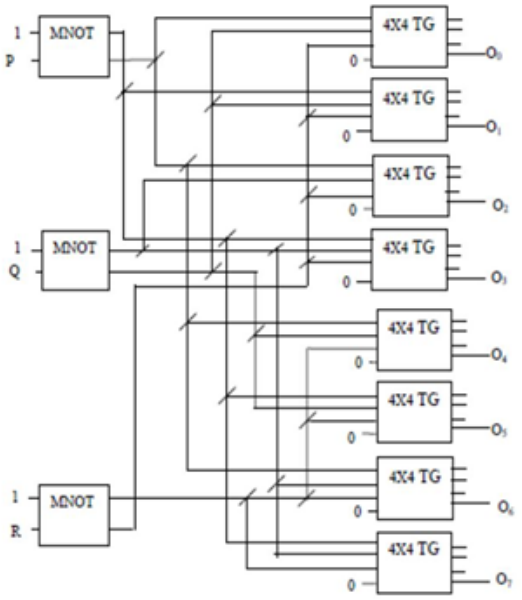


**Fig. 14. All-Optical realization of the reversible 3to8 Decoder**

Optical reversible 3t08 decoder design using proposed MNOT gate and Optical 4×4 T G. To realize this circuit, three MNOT gates and eight 4×4 TG gates are needed. The all-Optical realization of the reversible 3to8 Decoder is shown in the figure 14. The circuit is designed with 35 MZI switches, 58 Beam Splitters and 8 Beam Combiners. Delay of the circuit is 4Δ.

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## V.PROPOSED REVERSIBLE MZI SEQUENTIAL CIRCUITS:

In this section, we present all optical implementation of counters with the property of functional reversibility. Semiconductor Optical Amplifier (SOA) based Mach-Zehnder Interferometer (MZI) switches are used to design the sequential circuits. Our primary objective in this work is to achieve the reversible implementation of counters with minimum number of ancilla lines and MZI switches. All optical implementation of MZI-based asynchronous and synchronous counter is presented. Mathematical model to simulate the proposed architecture has also been presented. Finally, design complexities of all the counters are analyzed.

### A. Asynchronous Counters:

Asynchronous counter is known as ripple counter. Design architecture and working principle of all optical functionally reversible asynchronous down counter is presented here. The mathematical model for simulation of this memory element is described.

### A.1. Design of 2-bit positive edge triggered down counter:

The schematic diagram of MZI based 2-bit positive edge triggered down counter is depicted in Fig. 15(a), which is constituted with two positive edge triggered D flip flops viz. FF-0 and FF-1. Each of the positive edge triggered D flipflop consists of three MZI switches viz. MZI-1, MZI-2 and MZI-3, two beam combiner (BC) namely BC-1, BC-2 and four (expect the last flip flop viz. FF-1) beam splitters namely BS-1, BS-2, BS-3, BS-4. For proper understanding, we discuss the signal flow characteristic of the counter as shown in Fig. 15(a). A light from input port CP (Clock Pulse) directly incidents on MZI- 1 of FF-0 and acts as incoming signal. Similarly, another light signal from input port D0 directly enters into MZI-1 of FF-0 and acts as control signal of MZI-1. The light from bar port of MZI-1(B1) and a part of light from cross port of MZI-3(C3) is combined by BC-1 together to produce control signal of MZI-2.

In the same way, the output lights from cross port of MZI-1 (C1) and MZI-2 (C2) are combined by BC-2 and acts as control signal of MZI-3. A constant light signal (denoted by 1) incidents on the beam splitter (BS-1) and splits into two parts, where one part acts as incoming signal of MZI-3 and another part again incidents on another beam splitter (BS-2) and splits into two parts. One part appears to MZI-2 as incoming signal and another part that goes to next flip flop (FF-1) acts as a constant input light signal. The light from the cross port of MZI-3(C3) is the final output Q0 where as another light signal which emits from the cross port of MZI-2 (C2) goes back to port D0 and acts as incoming signal. A part of light comes from BS-5 of FF-0 incident on MZI-1 of FF-1 and acts as clock pulse of FF-1. Again, D1 acts as the input value of FF-1. We have obtained both the signals (clock pulse and input signal) for FF-1 and as the design architecture of FF-1 is same as FF-0, we omitted the control flow description of FF-1.

### A.2. Operational principle of 2-bit positive edge triggered down counter:

The operational principle of all the optical asynchronous down counter as shown in Fig 3(a), is described below. Here, the presence of light is denoted as 1 state and absence of light is denoted as 0 state.

• State I: Let Q0=0 and Q1=0. As D0 is directly connected to $Q_0$', hence, the value of D0 is 1. Now, the value of clock pulse is 1 i.e., both the control signal and incoming signal are present in MZI-1. Hence, according to the working principle of MZI, only bar port of MZI-1 of FF-0 emits light which incidents on BC-1 and as a result, an output light signal emits from BC-1. On the contrary, the cross port of MZI-1 emits no light which incidents on BC-2. Now, the output signal of BC-1 acts as the control signal of MZI-2 and the input signal of MZI-2 is also present. Therefore, the cross port of MZI-2 emits no light, as a result, no light incidents on BC-2. The output signal of BC-2 emits no light and as a consequence, the control signal of MZI-3 is absent.

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As the input signal of MZI-3 is present, the cross port of MZI-3 of FF-0 receives light which is the final output Q0 i.e. Q0=1. Now, this Q0 acts as incoming signal of MZI-1 of FF-1 and D1, which is directly connected to the $Q_{1bar,}$ acts as control signal of MZI-1. Therefore, both the incoming signal and control signal are present at MZI-1 as both the value of D1 and Q0 are 1. Hence, the operational principle of FF-1 becomes similar to FF-0 and the cross port of MZI-3 of FF-1 emits light i.e. the final output Q1=1. So the next state becomes Q1=1 and Q0=1.

• State II: Now, Q1= Q0= 1. Again the clock pulse (CP = 1) and D0 (equals the value of $Q_0$') act as incoming signal and control signal of MZI-1 of FF-1 respectively. Hence, only incoming signal is present at MZI-1. According to the working principle of MZI, the bar port of MZI-1 of FF-0 emits no light and cross port of MZI-1 of FF-0 emits light which incidents on BC-2. So the output signal of BC-2 is present that acts as control signal of MZI-3. Again, the input signal of MZI-3 is also present. So the cross port of MZI-3 receives no light i.e. the value of final output Q0=0.

This output Q0 acts as incoming signal of MZI-1 of FF-1 and D1 is directly connected toQ1bar. So the value of D1 is 0. As both the incoming signal and control signal are absent at MZI-1 of FF-1, no operation is performed in FF-1. Hence, the final output value of FF-1 does not change and it is same as the previous state's output value of Q1. Therefore, the final output of FF-1 is Q1=1.So the next state becomes Q1=1 and Q0=0.

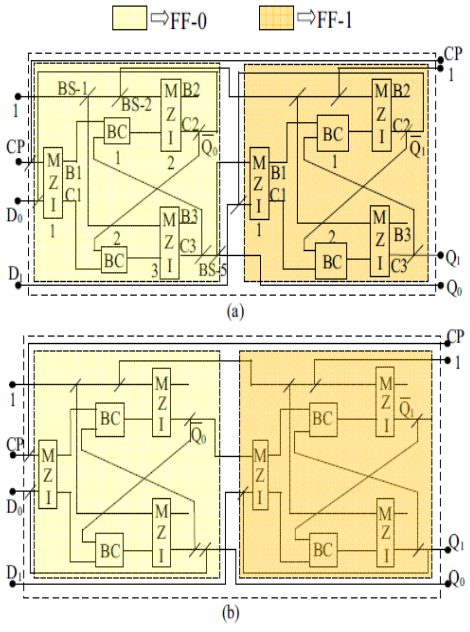
State III: Now, Q1 =1 and Q0 =0. The value of D0 (directly connected to Q0bar) is 1 and the value of clock pulse is 1 i.e. both the control signal and incoming signal are present at MZI-1. So the situation becomes same as that of FF-0 at first stage. Hence, according to working principle of FF-0 described in first stage, the final output of FF-0 is 1 i.e. Q0=1.

As Q0 acts as incoming signal of MZI-1 of FF-1 and D1 is directly connected to , so the value of D1 is 0. Therefore, only incoming signal is present at MZI-1 of FF-1. This situation is same as FF-0 of second stage. Hence, according to the working principle of FF-0 as described in second stage, the final output of FF-1 is 0 i.e. Q1=0. So the next state becomes Q1=0 and Q0=1.

• State IV: In this state, Q1=0, Q0=1 and the value of D0 (control signal of MZI-1) is 0. As the value of clock pulse is 1, only incoming signal is present at MZI-1 of FF-0. This situation is same as FF-0 of second stage. Hence, according to working principle of FF-0 as described in second stage, the final output of FF-0 is 0 i.e. Q0=0.

**TABLE-VII: DIFFERENT STATES OF ASYNCHRONOUS POSITIVE EDGETRIGGERED DOWN COUNTER**

| Clock Pulse | FF-0 | | | | FF-1 | | | |
|---|---|---|---|---|---|---|---|---|
| | $CP_0$ | $Q_0$ | $D_0$ $(\bar{Q}_0)$ | $Q_0^+$ | $CP_1$ $(Q_0^+)$ | $Q_1$ | $D_1$ $(\bar{Q}_1)$ | $Q_1^+$ |
| First | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| Second | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| Third | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| Fourth | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| Fifth | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |



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BC: Beam Combiner; BS: Beam Splitter; CP: Clock PulseThe states of the counter are shown in Table VII. The pictorial representation of positive edge triggered asynchronous up counter, negative edge triggered asynchronous down and up counter is depicted in Fig. 15(b), Fig 15(c), Fig 15(d), respectively. The flow chart of this simulation is shown in Fig. 15(e).

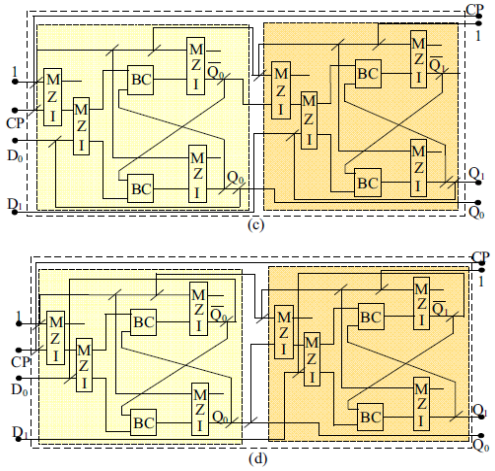

**Fig. 15: Design of all optical reversible (a) asynchronous positive edge triggered down counter, (b) asynchronous positive edge-triggered up counter (c) asynchronous negative edge-triggered down counter (d) asynchronous negative edge-triggered up counter using MZI switch.**

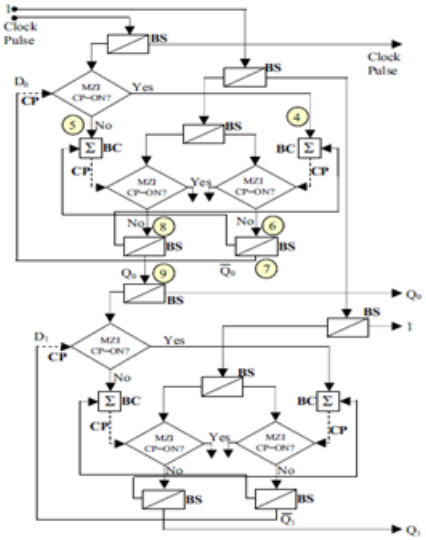

**Fig. 15(e): Control flow analysis of Asynchronous Positive edge-triggered down counter.**

CP: Control Pulse; BS: Beam Splitter; BC: Beam Combiner

### B. Synchronous Counter:

In the synchronous counter, all the flip-flops are triggered simultaneously. As we have already explained the working principle of asynchronous counter with detailed diagram, here only the pictorial representation of all optical reversible architecture of MZI based synchronous up counter (negative edge triggered) and down counter (positive edge triggered) is depicted in Fig. 15(f) and Fig. 15(g), respectively

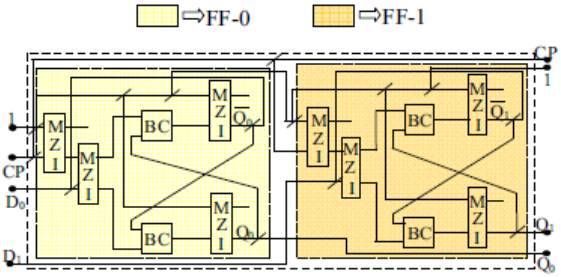


**Fig. 15(f): Synchronous negative edge-triggered up counter implemented by MZI switch**

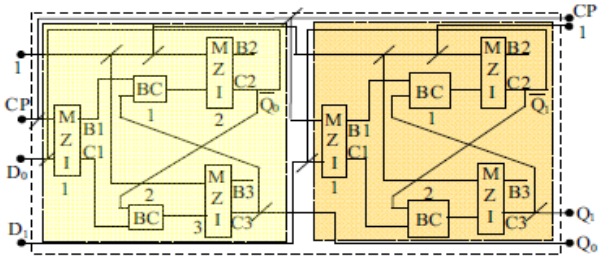

**Fig. 15(g): Synchronous Positive edge-triggered down counter implemented by MZI switch**

## VI. COMPARISION RESULTS:

The optical cost and optical propagation delay of the proposed all-optical reversib le logic circuits have been calculated in the previous section. Here the same have been analyzed and a summery has been presented in the following tables.Comparative studies of proposed designs of all-optical reversible 2×1 multiplexer and full adder circuits with the existing designs are presented in table VIII and XI respectively. This comparison is based on the optimization parameters such as optical cost, beam splitters, beam combiners,

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and optical delay of the circuits.The improvement percentage (IP) is calculated using the formulae: (1-proposed design cost/existing design cost) ×100.

### TABLE VIII COMPARATIVE STUDY OF ALL OPTICAL REVERSIBLE 2×1

| Proposed Design | MZI Switch {IP in %} | BS {IP in %} | BC {IP in %} | Optical delay {IP in %} |
|---|---|---|---|---|
| Our proposed design | 7 {12.5% } | 8 {33.33%} | 3 {40%} | 3Δ {No IP } |
| G. K. Maity et al. | 8 | 12 | 5 | 3Δ |

### TABLE XI COMPARATIVE STUDY OF ALL-OPTICAL REVERSIBLE FULL ADDER CIRCUIT

| Proposed Design | MZI Switch {IP in %} | BS {IP in %} | BC {IP in %} | Optical delay {IP in %} |
|---|---|---|---|---|
| Our proposed design | 5 {16.66%} | 8 { No IP } | 5 {16.66%} | 3Δ {No IP } |
| S. Kotiyal et al. | 6 | 8 | 6 | 3Δ |

All-optical reversible designs of 4×1 multiplexer, 1×4 De-multiplexer and 3to8 Decoder circuits are proposed first time, therefore, optical cost and optical delay of the these circuits have been presented in table X.

### TABLE X OPTICAL COST AND DELAY OF ALL-OPTICAL REVERSIBLE 4×1MULTIPLEXER, 1×4 DE-MULTIPLEXER AND 3TO8 DECODER

| Proposed Design | MZI Switch | BS | BC | Optical delay |
|---|---|---|---|---|
| 4×1 multiplexer | 18 | 24 | 5 | 4Δ |
| 1×4 De-multiplexer | 18 | 27 | 4 | 4Δ |
| 3to8 Decoder | 35 | 58 | 8 | 4Δ |

It can be observed that the proposed designs have been optimized in terms of MZI switch BS and BC. Analysis of design complexities of all optical reversible counters is presented in table XI.

Analysis of design complexities of all optical reversible counters is presented in table XI.

| Different types of n-bit counters | | No. of MZI (Optical Cost) | No. of Beam Combiner | No. of Beam splitter | Garbage Output |
|---|---|---|---|---|---|
| Asynchronous | down counter (positive edge-triggered) | 3n | 2n | 6n | 4 |
| | up counter(negative edge-triggered) | 4n | 2n | 7n | 6 |
| Synchronous | up counter(negative edge-triggered) | 4n | 2n | 7n | 6 |
| | down counter (positive edge-triggered) | 3n | 2n | 6n | 4 |

## VII. SIMULATION RESULTS:

All the synthesis and simulation results are performed using Verilog HDL. The synthesis and simulation are performed on Xilinx ISE 14.4. The simulation results are shown below figures.

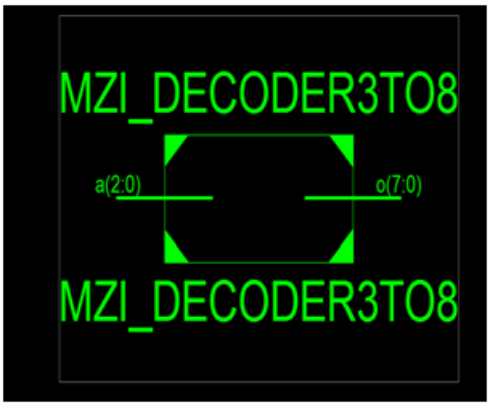


**Fig.16.a: RTL schematic of All-Optical realization of the reversible 3to8 Decoder**

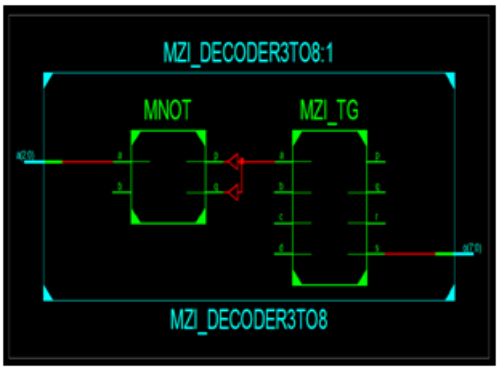


**Fig.16.b: RTL sub schematic of All-Optical realization of the reversible 3to8 Decoder**

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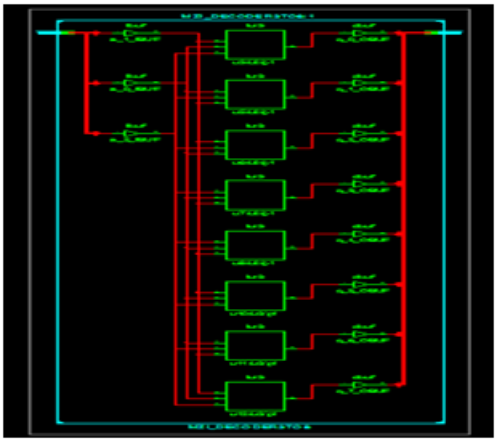

Fig.16.c: Technology schematic of All-Optical realization of the reversible 3to8 Decoder

Fig.16.d: Simulation of All-Optical realization of the reversible 3to8 Decoder

| MMOT Project Status (09/23/2016 - 18:10:22) | | | |
|---|---|---|---|
| Project File: | ORLGC.xise | Parser Errors: | No Errors |
| Module Name: | MZI_DECODER3TO8 | Implementation State: | Synthesized |
| Target Device: | xc3s500e-4fg320 | • Errors: | No Errors |
| Product Version: | ISE 14.4 | • Warnings: | 23 Warnings (15 new) |
| Design Goal: | Balanced | • Routing Results: | |
| Design Strategy: | Xilinx Default (unlocked) | • Timing Constraints: | |
| Environment: | System Settings | • Final Timing Score: | |

| Device Utilization Summary (estimated values) | | | |
|---|---|---|---|
| Logic Utilization | Used | Available | Utilization |
| Number of Slices | 4 | 4656 | 0% |
| Number of 4 input LUTs | 8 | 9312 | 0% |
| Number of bonded IOBs | 11 | 232 | 4% |

Fig.16.e: Design summary of the reversible 3to8 Decoder

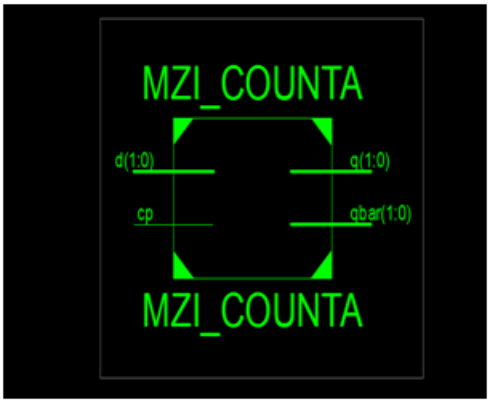


Fig.17.a: RTL schematic of Synchronous Positive edge-triggered down counter

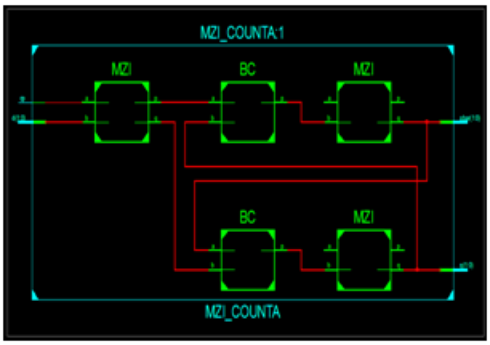


Fig.17.b: RTL schematic of Synchronous Positive edge-triggered down counter

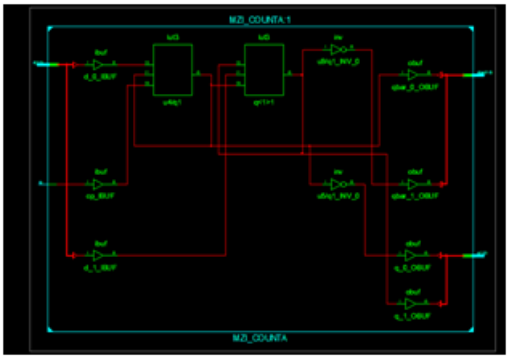

Fig.17.c: Technology schematic of synchronous positive edge-triggered up counter

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| MZI_COUNTA Project Status | | | |
|---|---|---|---|
| Project File: | MZI_COUNTERS.xise | Parser Errors: | No Errors |
| Module Name: | MZI_COUNTA | Implementation State: | Synthesized |
| Target Device: | xc3s500e-4fg320 | • Errors: | No Errors |
| Product Version: | ISE 14.4 | • Warnings: | 6 Warnings (0 new) |
| Design Goal: | Balanced | • Routing Results: | |
| Design Strategy: | Xilinx Default (unlocked) | • Timing Constraints: | |
| Environment: | System Settings | • Final Timing Score: | |

| Device Utilization Summary (estimated values) | | | |
|---|---|---|---|
| Logic Utilization | Used | Available | Utilization |
| Number of Slices | 2 | 4656 | 0% |
| Number of 4 input LUTs | 4 | 9312 | 0% |
| Number of bonded IOBs | 7 | 232 | 3% |

**Fig.17.d:Synthesis report of asynchronous positive edge-triggered up counter**

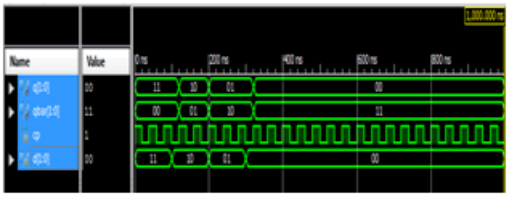

**Fig.17.e: Simulated output for asynchronous positive edge-triggered up counter**

## CONCLUSION AND FUTURE SCOPE:

Optical computing is emerging as a feasible technology to implement reversible logic. We have proposed a new general design approach to realize all-optical reversible logic circuits using SOA based MZI switches. An all-optical reversible MNOT gate has been proposed. The optical costs of the all optical reversible 2×1 multiplexer and full adder circuits have been minimized in the proposed designs. A 4-bit full adder circuit has been also designed using this full adder circuit. New designs of All-optical reversible designs of 4×1 multiplexer, 1×4 De-multiplexer and 3to8 Decoder circuits are proposed first time. An optimization algorithm may be proposed to minimize the optical cost of the all optical reversible circuits and the existing designs may be optimized. All –optical reversible sequential circuits may be designed. The proposed design techniques implement all the optical functionally reversible counters with minimum number of ancillary lines and minimum optical cost. Mathematical model has also been formulated.

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