ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

A Low Power Single Phase Clock Distribution Multiband Network

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Abstract :

Frequency synthesizer is one of the important elements for wireless communication application. The speed of VCO and prescaler determines how fast the frequency synthesizer is. A dual modulus prescaler contains logic gates and flip-flops. This project aim for developing a low power single clock multiband network which will supply for the multi clock domain network.

The multiband divider consists of a proposed wide-band multi modulus 32/33/47/48 prescaler and an improved bit-cell for swallow (S) counter and can divide the frequencies in the three bands of 2.4–2.484 GHz, 5.15–5.35 GHz, and 5.725– 5.825 GHz with a resolution selectable from 1 to 25 MHz The proposed multiband flexible divider is silicon verified and consumes power of 0.96 and 2.2 mW in 2.4- and 5-GHz bands, respectively, when operated at 1.8-V power supply.

Keywords:

D flip-flop (DFF), extended TSPC (ETSPC), frequency divider, operating frequency, power-delay-product (PDP), prescaler.

I. INTRODUCTION:

Frequency division is one of the important applications of flip-flops. A wide-band frequency synthesizer implemented by phase-locked loop (PLL) uses prescaler (also called N/N+1 counter) as fundamental block. In PLL high frequency output of VCO is coupled directly to the prescaler directly. As process technology is reducing, channel length and supply voltage is decreasing rapidly.

Therefore prescaler has to work at high frequency as well as low operating voltage. Due to incorporation of additional logic gates between the flip-flops to achieve the two different division ratios, the speed of the prescaler is affected by creating another propagation delay and the increases the switching power. Since flip-flop works as a part of the clock network, it consumes 30-50% of chip energy.

The demand for lower cost, lower power, and multiband RF circuits increased in conjunction with need of higher level of integration. The frequency synthesizer, usually implemented by a phase-locked loop (PLL), is one of the power hungry blocks in the RF front-end and the first stage frequency divider consumes a large portion of power in frequency synthesizer. Dynamic latches are faster and consume less power compared to static dividers. The TSPC and E-TSPC designs are able to drive the 97dynamic latch with a single clock phase and avoid the skew problem.

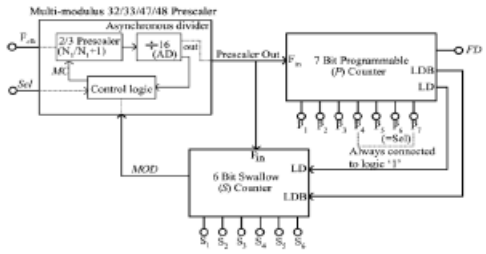

Fig I: Proposed dynamic logic multiband flexible Divider.

The frequency synthesizer uses an E-TSPC prescaler as the First-stage divider, but the divider consumes around 6.25 mW. Most IEEE 802.11a/b/g frequency synthesizers employ SCL dividers as their first stage while dynamic latches are not yet adopted for multiband synthesizers.

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In this paper, a Dynamic logic multiband flexible integer-n divider based on pulse-swallow topology is proposed which uses a low-power wideband 2/3 prescaler and a wideband multimodulus 32/33/47/48 prescaler as shown in Fig.1 The divider also uses an improved low power loadable bit-cell for the Swallow S-counter. a true-single-phase-clock (TSPC) policy was introduced. Single-phase-clock policies are superior to the others due to the simplification of the clockdistribution on the chip and reducing the transistor number.

They reduce the number of clock-signal requirements and the wiring costs also they have no problems with phase overlapping. Thus, higher frequencies and simpler designs can be achieved. Further enhancement in the design is achieved by using extended true-single phase clock (ETSPC) DFFs.

II. CONVENTIONAL TSPC BASED DIV-BY-2/3 PRESCALER :

The TSPC architecture has the advantage of a higher operating frequency compared to that of master-slave and differential flip-flops. In order to reduce the power consumption and propagation delay digital gates are embedded into the flip-flops where the conventional 2/3 prescaler consists of an OR gate, AND gate and two D flip-flops [5].

The conventional 2/3 prescaler uses two DFFs where DFF1 is loaded by an OR gate and DFF2 is loaded by DFF1, an AND gate and an output stage which makes a larger load.

This large load on DFF2 causes substantial power dissipation and limits the speed of operation. The difficulty in embedding the OR, AND gates into the DFF introduces additional delay by the digital gates which limits the speed of operation in conventional one.

A low power and improved speed 2/3 prescaler implemented in the TSPC logic format is proposed in [13]. Fig 4 shows the new prescaler which uses two neither embedded NOR gates instead of an OR and an AND gate for the conventional 2/3 TSPC prescaler. This arrangement reduces the number of switching nodes from 12 to 7 and consumes less power compared to the conventional 2/3 prescaler.

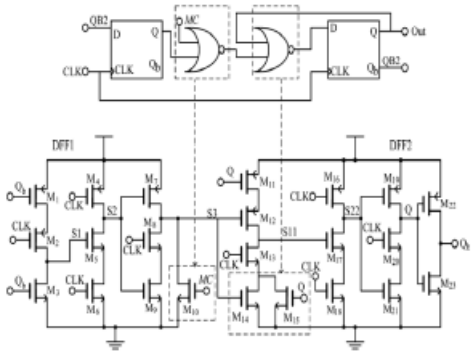

Fig 2: Design-I TSPC 2/3 prescaler circuit and equivalent gate level schematic.

Later an ultra-low power 2/3 prescaler (Design-II) in [6], a further improved version of the Design-I is shown in Fig 5. In this design a pMOS transistor, connected between power supply and DFF1 with the control logic signal MC selects the divide-by-2 or divide-by-3 mode. When MC is logically high DFF1 will disconnected from the power supply and DFF2 alone work to form the divide-by-2 operation. Therefore the short circuit power and switching power of DFF1 is removed. When the control signal MC goes low pMOS transistor will turns on and both flip-flops combine give the divide-by-3 operation. Operating frequency is directly related to the supply voltage. Since due to the Vds drop across transistor M1a, DFF1 operates at a decreased voltage level which limits the maximum operating frequency [13]. However, by decreasing the stacked connection in the first stage of Design-II similar to the design in [10] improves the frequency range to almost same as that of the Design-I.

III. ETSPC 2/3 PRESCALERS :

As a part of increasing operating frequency and reducing supply voltage ETSPC FFs outstand the TSPC FFs. The two major conventional divide-by-2/3 ETSPC designs are in [4] and [5]. Design causes redundant power consumption in the div-by- 2 mode operation. Design in overcomes the toggling of FF1 during divide-by-2 operation by changing the control logic from output of FF1 to its input. But the first stage in design causes larger power consumption. Even though both designs are simpler, the inverter between both flip-flops and parallel connected transistor introduce extra delay and larger parasitic capacitance [7]. To prevent these issues a new method is proposed using ETSPC technique.

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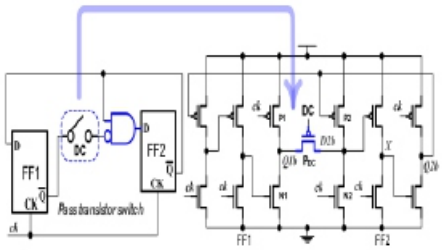

Fig 3: Schematic of proposed E-TSPC based divide-by-2/3 prescaler.

IV. MULTTMODULUS 32/33/47/48 PRESCALER The proposed wideband multimodulusprescaler which can divide the input frequency by 32, 33, 47, and 48 is shown in Fig.4. It is similar to the 32/33 prescaler but with an additional inverter and a multiplexer. The proposed prescaler performs additional divisions (divide-by-47 and divide-by-48) without any extra flip-flop, thus saving a considerable amount of power and also reducing the complexity of multi band divider.

The multimodulusprescaler consists of the wideband 2/3 (N/(N]+I)) prescaler, four asynchronous TSPC divide-by-2 circuits ((AD)=16) and combinational logic circuits to achieve multiple division ratios. Beside the usual MOD signal for controlling N/(N+I) divisions, the additional control signal sel is used to switch the prescaler between 32/33and 47/48 modes.

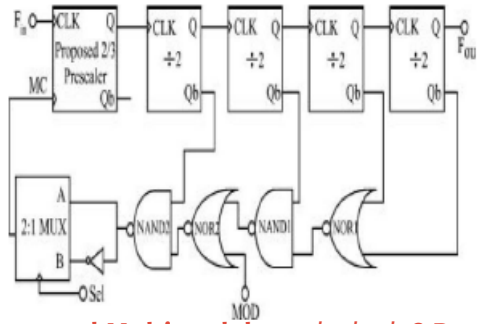

Fig 4: Proposed Multimodulus 32/33/47/48 Prescaler.

Fig.4 shows that the Prescaler work as a divide-by-2 counter. Alternatively when DC is low pMOS transistor will turn on and both flip-flops are linked to form divide-by-3 operation.showsprescaler functioning as a div-by-3 frequency divider. Besides the reduction of supply voltage and capacitance load, the proposed prescaler reduces the area since it uses only 13 transistors to perform divide-by-2 or divide-by-3 compared to the conventional prescalers. The minimum height transistor stacked connections create less capacitance load for the previous stage and reduce the dynamic power consumption.

However, reduced stacked connection increases short circuit power.The delay of dual modulus prescaler for divide-by-2 and divide-by-3 operation respectively. The operation speed of proposed design is 33.3% and 63.5% faster than WPMS, which took maximum delay, in divide-by-2 and divide-by-3 respectively. From both figures it is understood that ETSPC technique obtain less delay compared with others. This is due to the advantage of reduced transistorstacked height and load capacitance of ETSPC technique.

A. Swallow (S) Counter :

The 6-bit s-counter shown in Fig.4.consists of six asynchronous loadable bit-cells, a NOR-embedded DFF and additional logic gates to allow it to be programmable from 0 to 31 for low-frequency band and from 0 to 47 for the high-frequency band. The asynchronous bit cell used in this design shown in Fig.4.is similar to the bit-cell except it uses two additional transistors M6 and M7whose inputs are controlled by the logic signal MOD. If MOD is logically high, nodes S 1 divide-by-48) and P, S counters start down counting the input clock cycles.

When the S-counter finishes counting, MOD switches to logic "1" and the prescaler changes to the divide-by-n mode (divide-by-32 or divide-47) for the remaining P-S clock cycles. During this mode, since S-counter is idle, transistors M6 and M7 which are controlled by MOD, keep the nodes S 1 and S2 at logic "0," thus saving the switching power in S counter for a period of (N*(P-S)) clock cycles. the programmable input (PI) is used to load the counter to a specified value from 0 to 31 for the lower band and o to 48 for the higher band of operation.

B. Programmable (P) Counter :

The programmable P-counter is a 7-bit asynchronous down counter which consists of 7 loadable bit-cells and additional logic gates. Here, bit P7 is tied to the Sel signal of the multi modulus prescaler and bits P 4 and P7 are always at logic "1." The remaining bits can be externally programmed from 75 to 78 for the lower frequency band and from 105 to 122 for the upper frequency band.

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When the P-counter finishes counting down to zero, LD switches to logic "1" during which the output of all the bit-cells in S-counter switches to logic "1" and output of the NOR embedded DFF switches to logic "0" (MOD=O) where the programmable divider get reset to its initial state and thus a fixed division ratio is achieved. If a fixed 32/33 (N/(N+ 1)) dual-modulus prescaler is used, a 7bit P counter is needed for the low-frequency band (2.4 GHz) while an 8-bit S-counter would be needed for the high frequency band(5-5.825 GHz) with a fixed 5-bit S counter. Thus, the multimodulus32/33/47/48 prescaler eases the design complexity of the P-counter.

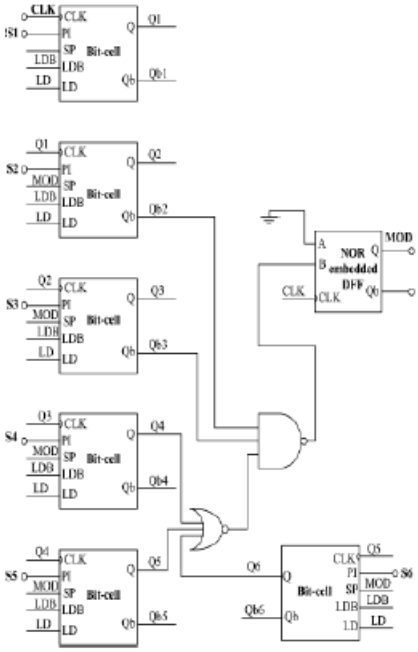

Fig 5: Asynchronous 6-Bit S-Counter.

V. SIMULATIONS AND SILICON VERIFICATIONS:

The simulations of the designs are performed using TANNAR EDA TOOL for a 180nm CMOS process. The simulation results show that the wide band 2/3 prescaler has the maximum operating frequency of 8 GHz with a power consumption of 0.92 and 1.73 mW during the divide-by-2 and divide-by-3 modes, respectively. The proposed wide band multimodulusprescaler has the maximum operating frequency of 7.2 GHz (simulation) with power consumption of 1.52, 1.60, 2.10, and 2.13 mW during the divide-by-32, divide-by-33, divide-by-47 and divide-by-48, respectively. On-wafer measurements are carried out using an 8 inch RF probe station.

The input signal for the measurement is provided by the 83650B 10 MHz- 50 GHz HP signal generator and the output signals are captured by the 8600A 6G oscilloscope. The measurement results shows that the wideband 2/3 prescaler has a maximum operating frequency of 6.5 GHz [10] and the multimodulus 32/33/47/48 prescaler designed using wideband 2/3 prescaler has a maximum operating frequency of 6.2 GHz. However, the maximum operating frequency that can be achieved by the multimodulus 32/33/47/48 prescaler is limited by the wideband 2/3 prescaler. The performance of the multiband flexible divider is measured in both the lower frequency and higher frequency bands by programming the P-and S-counters. Fig. 8 shows the measured output waveform of the multiband divider at an input frequency of 2.47 GHz where counters are programmed to have values 77 and 6 respectively.

Fig. 9 shows the measured output waveform of the multiband divider at an input frequency of 5.818 GHz where P and S counters are programmed to have values 122 and 38, respectively. The proposed multiband flexible divider consumes an average power of 0.96 mW during lower frequency band (2.4–2.484 GHz), while it consumes 2.2 mW during the high-frequency band (5–5.825 GHz) of operation compared to the dual-band divider reported in [9], which consumes 2.7 mW at 1-V power supply. The proposed multiband divider has a variable resolution of K MHz for lower frequency band (2.4– 2.484 GHz) and for the higher frequency band (5–5.825 GHz), where K is integer from 1 to 5 for 2.4- GHz band and 5, 10, and 20 for WLAN applications.

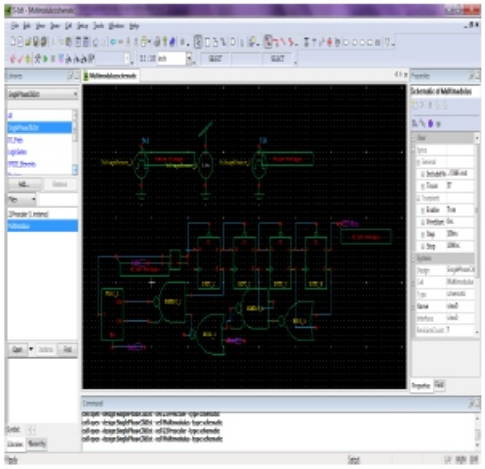

Fig 6: Designing of Multimodulus

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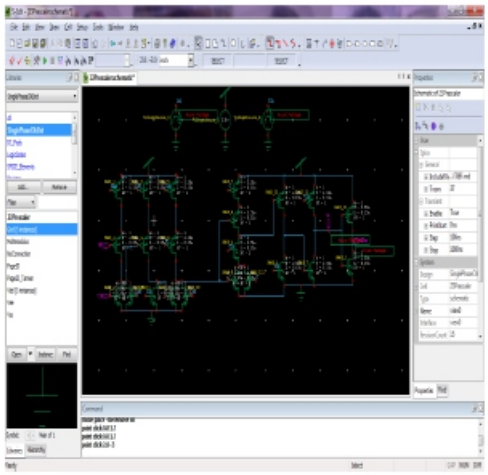

Fig 7: Designing of Prescaler

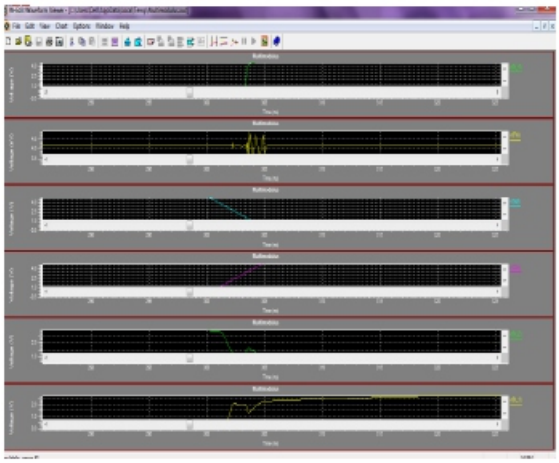

Fig 10: Prescaler 32/33/47/48 output

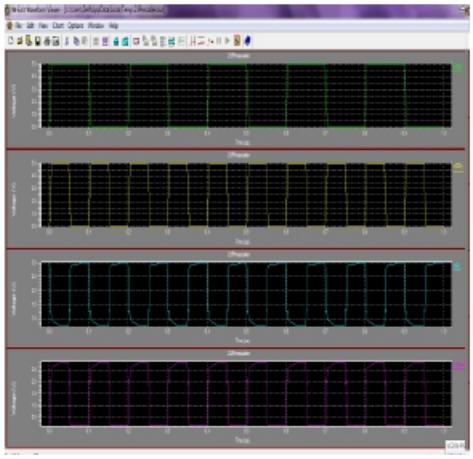

Fig 8: DFF1 Output Waveform

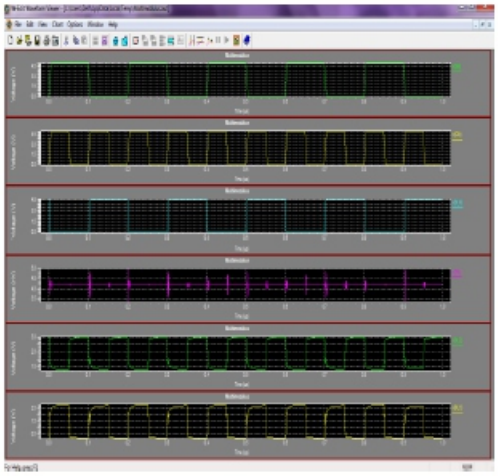

Fig 9: Multimodulus Output Waveform

VI. CONCLUSION :

In this paper, a wideband 2/3 prescaler is verified in the design of proposed wide band multimodulus 32/33/47/48 prescaler. A dynamic logic multiband flexible integer-N divider is designed which uses the wideband 2/3 prescaler, multimodulus 32/33/47/48 prescaler, and is silicon verified using the 0.18micro meter CMOS technology. Since the multimodulus 32/33/47/48 prescaler has maximum operating frequency of 6.2 GHz, the values of P and S-counters can actually be programmed to divide over the whole range of frequencies from 1 to 6.2GHz with finest resolution of 1 MHz and variable channel spacing.

However, since interest lies in the 2.4- and 5–5.825-GHz bands of operation, the P and S-counters are programmed accordingly. The proposed multiband flexible divider also uses an improved loadable bit-cell for Swallow _-counter and consumes a power of 0.96 and 2.2 mW in 2.4- and 5-GHz bands, respectively, and provides a solution to the low power PLL synthesizers for Bluetooth, Zigbee, IEEE 802.15.4, and IEEE 802.11a/b/g WLAN applications with variable channel spacing. By using this multimodulusprescaler, the Clock Jitter can be avoided.

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