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Low Power MSIC Signatures for Effective BIST Design

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Abstract: ***In BIST architecture the ATPG is the one of important consideration .the performance also the depends on the appropriate ATPG generation .in our paper we propose the novel method of multiple single input change (MSIC) test patterns that are intended for the scan chain. In order to develop any method we need to consider the area and power aspects for the advanced VLSI designs, and also able to perform the test efficiently using test-per-clock and the test-per-scan strategies. The proper analysis for the design of MSIC also provided. The output signatures of the tested circuit also verified to check by using the multiple input signature registers (MISR). The performance evaluation is done by designing in verilog and using simulation and synthesis tools like Model-sim 6.6 and Xilinx14.3 the output demonstration and verification ISCAS benchmarks can be used. The proposed method provides efficient fault coverage without increase of BIST architecture and test time.***

I. INTRODUCTION

VLSI on chip testing is very difficult and also an important consideration for the present advance systems. In order to achieve the run time testing we introduces the concept called built-in self-test

(BIST),in this providing the testing environment along with the circuit-under-test (CUT).in traditional BIST structures the relay on the linear feedback shift register (LFSR) and multiple input signature register (MISR) are used for the generation of Test patterns. By using the methods of test patterns causes the drawbacks like high switching activity and high Power consumption and more test time, this may affect the behavior operation of the CUT and also has the aging problem. By using these methods we need to generate the more number of test pattern for the effective fault coverage.

The traditional pseudorandom patterns cannot have the ability to detect the new faults. They are generally mended for the traditional fault detections. These test methods have high fault coverage with minimum number of test patterns also. But the major problem that associated with these methods are the high area and power overhead conditions.

Different advance less power scan-based method are proposed in previous by changing the less power architectures and made several changes in scan path designs in order to obtained unchanged input when handling the shift operations. In another approach that uses the many scan enables by using the many scan chains that activates any one at ones that also reduces the overall consumption of operation power of scan based tests of CUT .

II. LITERATURE REVIEW

This is one of the designs for testability (DFT) mechanism that can able to test the circuit at the run time. The advance design feature that has capable of tasting using the built-in test setup that able to increase the testing standards and also the testing time

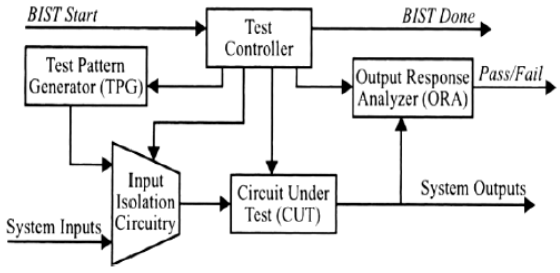

Figure1. BIST Basic block diagram

The basic BIST requires the elements like pest pattern generator for proving the test input patterns, test controller used for entire test control and response analyzer used for the

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analysis of outputs of form the CUT and tells whether test is pass or fail.

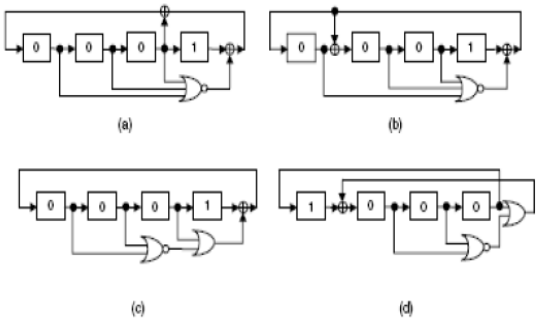

Figure2. Example of LSFR

The above shown are the different LFSRs used for the generation of test pattern generation. But the major drawback that has with use of these LFSRs as test pattern generator (TPG) that provides high switching power even more than the normal operation of the CUT that causes the increase of operation power and that also leads the operation delay.

III. PROPOSED METHOD

This section describes the proposed test patter design that able to provide the less transition test vectors applied for the multiple scan chains. First, the basic signature vector is unwound to poly code words and these are XOR with the proposed design signatures and fed to the all scan chains. The proposed BIST setup consists of the basic LFSR and signature evaluation circuit that consists of the Johnson Counter and the gray code converter.

The primary vectors that are generated from the LFSR are can be termed as the $S(t) = S0(t)S1(t)S2(t), \ldots, Sm-1(t)$ and the vector generated by an l-bit Johnson counter can be labeled as as $J(t) = J0(t)J1(t)J2(t), \ldots, Jl-1(t)$.For the first clock cycle, $J = J0\ J1\ J2, \ldots, Jl-1$ willbit-XOR with $S = S0S1S2, \ldots, SM-1$, and the results$X1Xl+1X2l+1, \ldots, X(M-1)l+1$ will be shifted into Mscan chains, respectively. In next clock cycle,$J = J0\ J1\ J2, \ldots, Jl-1$ will be gray coded as $J = g0,g1\ g2, \ldots, gl-1$, which can be bit-XOR withthe seed $S = S0S1S2, \ldots, SM-1$. The resulting$X2Xl+2X2l+2, \ldots, X(M-1)l+2$ will be agitated into Mscan chains, respectively. After the l clocks, every scan chain willbe fully adulterated with a singular Johnson codeword, and signatures$S0S1S2, \ldots, Sm-1$ will be fed to m PIs. Depend upon the scan lengths this method able to generate two different types of SIC generators to generate Johnson code words and vectors separately.

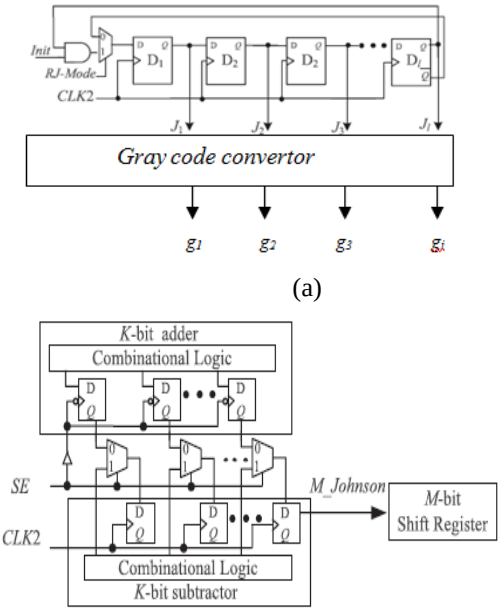

Figure3. SIC generators. (a) Gray coded Johnson counter. (b) Scalable SIC counter.

The main intention of our proposed concept is to minimize the switching activity of CUT. The area of the design can be reduced by providing the appropriate relation with the decomposed vectors of certain particular vectors. That has feature of providing the selective patter allocation which increase the evaluation. Major aspect that these patters should has unique to the each other that facilitates the reduction of test conduction time, in general when the pattern are repeating the overall test time also will increased what will not be ideal for the present advance VLSI systems.Finally, unique patterns are intended to reduce thetest length (patterns that are required for theefficient fault coverage). The main aim of this section is to provide the required test vectors for the selective configured CUT. Un uniformly distributed test vectors there may be a chance of occurring the same input to the particulate element causes the undetectable faults may occurs where the patters may not cover because in un uniform test vector generation

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some bits are same for all or most of patterns. Therefore those can be undetected by the test mechanism these faults may escape. Hence in order to perform the efficient circuit test the uniformly distributed test vectors are required.

From the above the efficient unique MSIC patterns can bepatternized by the proposed architectures that covers the appropriate fault coverage. Also, there are linear renationalized patterns or within a pattern.The main feature that provided to the system apart from the previous system that can able to provide the patters are very high random in nature. In order to achieve this we made certain changes in the previous architecture, we replaces the step after the Johnson counter sequences arrived. The shifter operation can be limited so we propose new architecture of gray code converter that can able to provide the efficient unique test patterns for multiple scan chains.Efficient low power single input test pattern can be achieved in previous method by using the LFSR and Johnson counter and scan shift register but if clock frequency is much high this concept also failed to provide the low power BIST environment.

Linear feedback shift register (LFSR) used in many architecture because it has the feature of low power and also occupies less area. In this paper also we consider the LFSR as the basic element in proposed method organization and followed by the modified Johnson counter and gray code converter

IV.RESULT AND DESCUSSIONS

We have designed our proposed method that will provide the novel test patterns that is shown in bellow fig4 simulated wave form. By this we can note that the dynamic power of the test pattern generation can be reduced because the change of test patterns are not that much assaulted compared to previous. The static power of the proposed method can be reduced. Where as in the existing method total power consumption can be 0.042A but our proposed method can utilizes only 0.020A only. The power of the system can be reduced that can be shown in fig5

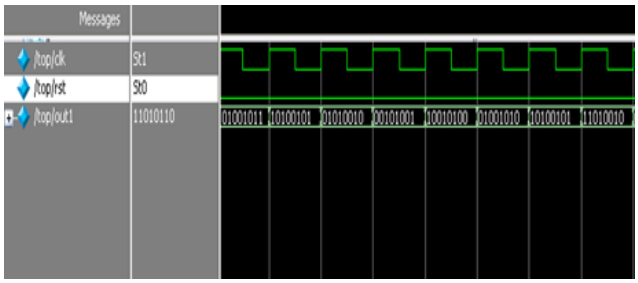

Fig 4: simulation of test pattern generator

Supply Summary		Total	Dynamic	Quiescent
Source	Voltage	Current (A)	Current (A)	Current (A)
Vccint	1.200	0.006	0.000	0.006
Vccaux	2.500	0.003	0.000	0.003
Vcco25	2.500	0.002	0.000	0.002

	Total	Dynamic	Quiescent
Supply Power (W)	0.020	0.000	0.020

Fig 5: power of test pattern generator circuit

V.CONCLUSION

We designed a novel advanced method of test patter generator circuit which can reducers the static and dynamic power efficiently. And also reduces the ageing problem of the circuit. When compared with the previous method the hard ware overhead can be reduced and also abbreviates the total test time and also the total power. Experimental results and verification can be described

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