Flexible and an Efficient Frequency Divider

Gandikota Jilan Basha
M.Tech in VLSI System Design,
Srinivasa Institute of Technology and Science (SITS),
Kadapa.

G.Venkata Karthik, M.Tech
Assistant Professor
Srinivasa Institute of Technology and Science (SITS),
Kadapa.

Abstract: *A low-power single-phase clock multiband flexible divider for Bluetooth, Zigbee and IEEE 802.15.4 and 802.11a/b/g WLAN frequency synthesizers is proposed based on pulse-swallow topology. The multiband divider consists of a proposed wideband multimodulus 32/33/47/48 prescaler and an improved bit-cell for swallow (S) counter and can divide the frequencies in the three bands of 2.4–2.484 GHz, 5.15–5.35 GHz, and 5.725–5.825 GHz with a resolution selectable from 1 to 25MHz.*

Index Terms—DFF, dual modulus prescaler, dynamic logic, E-TSPC, frequency synthesizer, high-speed digital circuits, true single-phase clock(TSPC), wireless LAN (WLAN).

INTRODUCTION

WirelessLAN (WLAN) in the multigigahertz bands, such as HiperLAN II and IEEE 802.11a/b/g, are recognized as leading standards for high-rate data transmissions, and standards like IEEE 802.15.4 are recognized for low-rate data transmissions. The demand for lower cost, lower power, and multiband RF circuits increased in conjunction with need of higher level of integration. The frequency synthesizer, usually implemented by a phase-locked loop (PLL), is one of the power-hungry blocks in the RF front-end and the first-stage frequency divider consumes a large portion of power in a frequency synthesizer.

The integrated synthesizers for WLAN applications at 5 GHz CMOS realizations, where the first-stage divider is implemented using an injection-locked divider which consumes large chip area and has a narrow locking range. The

best published frequency synthesizer at 5 GHz consumes 9.7mWat 1-V supply, where its complete divider consumes power around 6mW [3], where the first-stage divider is implemented using the source-coupled logic (SCL) circuit [4], which allows higher operating frequencies but uses more power. Dynamic latches are faster and consume less power compared to static dividers. The TSPC [5] and E-TSPC [6] designs are able to drive the dynamic latch with a single clock phase and avoid the skew problem [5].

However, the adoption of single-phase clock latches in frequency dividers has been limited to PLLs with applications below 5 GHz [7], [8]. The frequency synthesizer reported in [6] uses an E-TSPC prescaler as the first-stage divider, but the divider consumes around 6.25mW. Most IEEE 802.11a/b/g frequency synthesizers employ SCL dividers as their first stage [3], [9], while dynamic latches are not yet adopted for multiband synthesizers.

A frequency divider, also called a clock divider or scaler or prescaler, is a circuit that takes an input signal of a frequency, f_{in}, and generates an output signal of a frequency:

$$f_{out} = \frac{f_{in}}{n}$$

where n is an integer. Phase-locked loop frequency synthesizers make use of frequency dividers to generate a frequency that is a multiple of a reference frequency. Frequency dividers can be implemented for both analog and digital applications.

In this paper, a dyamic logic multiband flexible Fig. 1. Proposed dynamic logic multiband flexible divider integer-N divider based on pulse-swallow topology is proposed which uses a low-power wideband 2/3 prescaler [10] and a wideband multimodulus 32/33/47/48 prescaler as shown in Fig. 1. The divider also uses an improved low-power loadable bit-cell for the Swallow S-counter.
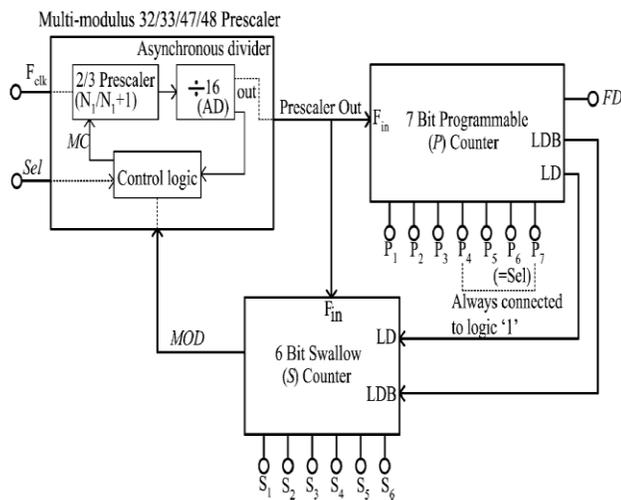

Fig.1. Proposed dynamic logic multiband flexible divider.

DESIGN CONSIDERATIONS

The key parameters of high-speed digital circuits are the propagation delay and power consumption. The maximum operating frequency of a digital circuit is calculated by the method described in [11] and is given by

$$Fmax = \frac{1}{Tplh + Tphl} \qquad (1)$$

where Tplh and Tphl are the propagation delays of the low-to-high and high-to-low transitions of the gates, respectively. The total power consumption of the CMOS digital circuits is determined by the switching and short circuit power.

The switching power is linearly proportional to the operating frequency and is given by the sum of switching power at each output node as in

$$Pswitch = \sum_{l=1}^{n} Fclk\ Cli\ Vdd^2 \qquad (2)$$

Where n is the number of switching nodes, Fclk is the clock frequency, Cli is the load capacitance at the output node of the ith stage, and Vdd is the supply voltage. Normally, the short-circuit power occurs in dynamic circuits when there exists direct paths from the supply to ground which is given by

$$Psc = Isc*Vdd \qquad (3)$$

Where Isc is the short-circuit current. The analysis in [12] shows that the short-circuit power is much higher in E-TSPC logic circuits than in TSPC logic circuits. However, TSPC logic circuits exhibit higher switching power compared to that of E-TSPC logic circuits due to high load capacitance. For the E-TSPC logic circuit, the short-circuit power is the major problem. The E-TSPC cicuit has the merit of higher operating frequency than that of the TSPC circuit due to the reduction in load capacitance, but it consumes significantly more power than the TSPC circuit does for a given transistor size. The following analysis is based on the latest design using the popular and low-cost 0.18um CMOS process.

WIDEBAND E-TSPC 2/3PRESCALER

The E-TSPC 2/3 prescaler reported in [12] consumes large shortcircuit power and has a higher frequency of operation than that of TSPC 2/3 prescaler. The wideband single-phase clock 2/3 prescaler used in this design was reported in [10] which consists of two D-flip-flops and Fig. 2. Wideband single-phase clock 2/3 prescaler. Two NOR gates embedded in the flip-flops as in Fig. 2. The first NOR gate is embedded in the last stage of

DFF1, and the second NOR gate is embedded in the first stage of DFF2 . Here, the transistors M2, M25, M4, andM8 in DFF1 helps to eliminate the short-circuit power during the divide-by-2 operation. The switching of division ratios between 2 and 3 is controlled by logic signal MC.

When MC switches from "0" to "1," transistors M2, M4, and M8 in DFF1 turns off and nodes S1, S2 and S3 switch to logic "0." Since node S3 is "0" and the other input to the NOR gate

embedded in DFF2 is Qb, the wideband prescaler operates at the divide-by-2 mode. During this mode, nodes S1, S2 and S3 switch to logic "0" and remain at "0" for the entire divide-by-2 operation, thus removing the switching power contribution of DFF1. Since one of the transistors is always OFF in each stage of DFF1, the short-circuit power in DFF1 and the first stage of DFF2 is negligible. The total power consumption of the prescaler in the divide-by-2 mode is equal to the switching power in DFF2 and the short-circuit power in second and thirrd stages of DFF2 and is given by

$$Pswittch\_divided\_by\_2 = \sum_{i=1}^{4} Fclk\, CLi\, Vdd^{2} + Psc1 + Psc2$$

Where CLi is the load capacitance at the output node of the ith stage of DFF2, and Psc1 and Psc2 are the short-circuit power in the second and third stages of DFF2. When logic signal MC switches from "1" to "0," the logic value at the input of DFF1 is transferred to the input of DFF2 as one of the input of the NOR gate embedded in DFF1 is "0" and the wideband prescaler operates at the divide-by-3 mode. During the divide-by-2 operation, only DFF2 actively participates in the operation and contributes to the total power consumption since all the switching activities are blocked in DFF1. Thus, the wideband 2/3 prescaler has benefit of saving more than 50% of power during the divide-by-2 operation. The measured results shows that the wideband 2/3 prescaler has the maximum operating frequency of 6.5 GHz. Fig. 3 shows the simulated and measured power consumption of the wideband 2/3 prescaler at different frequencies for a supply voltage of 1.8 V.

MULTIMODULUS 32/33/47/48 PRESCALER

The proposed wideband multimodulus prescaler which can divide the input frequency by 32, 33, 47, and 48 is shown in Fig. 4. It is similar to the 32/33 prescaler used in [7], but with an additional inverter and a multiplexer. The proposed prescaler performs additional divisions (divide-by-47 and divide-by-48) without any extra flip-flop, thus saving a considerable amount of power and also reducing the complexity of Fig. 3. Post layout and measured power consumption results of 2/3 prescaler.
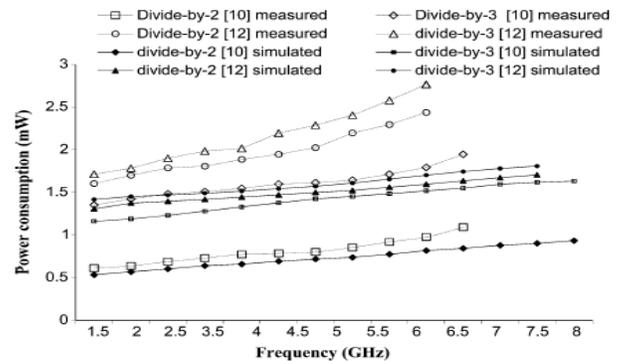

Fig.2. post layout and measured power consumption results of 2/3 prescaler.

Fig. 2. Proposed multimodulus 32/33/47/48 Prescaler. Multiband divider which will be discussed in Section V. The multimodulus prescaler consists the wideband2/3(N1/(N1+1))prescaler[10],four asynchronous TSPC divide-by-2 circuits (AD=16) and combinational logic circuits to achieve multiple division ratios. Beside the usual MOD signal for controlling (N1/N1+1) divisions, the additional control signal Sel is used to switch the prescaler between 32/33 and 47/48 modes.
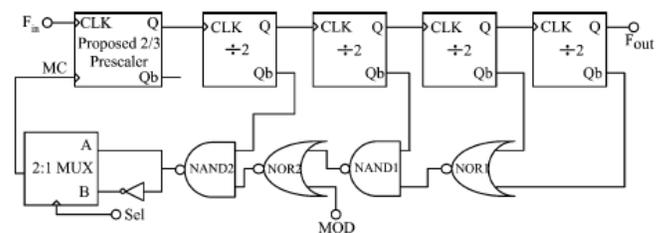

Fig.3.Proposed mltimodulus 32/33/47/48 prescaler.

A. Case 1: Sel='0'

When Sel=0 , the output from the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as the normal 32/33 prescaler, where the division ratio is controlled by the logic signal MOD. If MC=1, the 2/3 prescaler operates in the divide-by-2 mode and when MC=0 , the 2/3 prescaler operates in the divide-by-3 mode. If MOD=1, the NAND2 gate output switches to logic "1" (MC=1) and the wideband prescaler operates in the divide-by-2 mode for entire operation. The division ratio N performed by the multimodulus prescaler is

$$N=(AD*N1)+(0*(N1+1))=32 \quad (6)$$

Where N1=1 and AD=16 is fixed for the entire design. If MOD=0 , for 30 input clock cycles MC remains at logic "1", where wideband prescaler operates in divide-by-2 mode and, for three input clock cycles, MC remains at logic "0" where the wideband prescaler operates in the divide-by-3 mode. The division ratio N+1 performed by the multimodulus prescaler is

$$N+1=((AD-1)*N1)+(1*(N1+1))=33 \quad (7)$$

B. Case 2: Sel=1

When Sel=1, the inverted output of the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as a 47/48 prescaler, where the division ratio is controlled by the logic signal MOD. If MC=1, the 2/3 prescaler operates in divide-by-3 mode and when Sel=1, the 2/3 prescaler operates in divide-by-2 mode which is quite opposite to the operation performed when Sel=0. If MOD=1, the division ratio N+1 performed by the multimodulus prescaler is same as (6) except that the wideband prescaler operates in the divide-by-3 mode for the entire operation given by

$$N+1=(AD*(N1+1))+(0*N1)=48 \quad (8)$$

If MOD=1, the division ratio N performed by the multimodulus prescaler is
$$N=((AD-1)*(N1+1))+(1*N1)=47 \quad (9)$$

MULTIBAND FLEXIBLE DIVIDER

The single-phase clock multiband flexible divider which is shown in Fig. 1 consists of the multimodulus 32/33/47/48 prescaler, a 7-bit programmable P-counter and a 6-bit swallow S-counter. The multimodulus 32/33/47/48 prescaler is briefly discussed in Section IV. The control signal Sel decides whether the divider is operating in lower frequency band (2.4 GHz) or higher band (5–5.825 GHz).

A. Swallow ___ Counter

The 6-bit S-counter shown in Fig. 5 consists of six asynchronous loadable bit-cells, a NOR-embedded DFF and additional logic gates to allow it to be programmable from 0 to 31 for low-frequency band and from 0 to 47 for the high-

frequency band. The asynchronous bit-cell used in this design shown in Fig. 6 is similar to the bit-cell reported in [13], except it uses two additional transistors M6 and M7 whose inputs are controlled by the logic signal MOD. If MOD is logically high, nodes S1 and S2 switch to logic "0" and the bit-cell does not perform any function. The MOD signal goes logically high only when the S-counter finishes counting down to zero. If MOD and LD are logically low, the bit-cell acts as a divide-by-2 unit. If MOD is logically low and LD is logically high, the input bit PI is transferred to the output.

In the initial state, MOD, the multimodulus prescaler selects the divide-by-(N+1) mode (divide-by-33 or divide-by-48) and P,S counters start down counting the input clock cycles. When the S-counter finishes counting, MOD switches to logic "1" and the prescaler changes to the divide-by-N mode (divide-by-32 or divide-47) for the remaining (P-S)clock cycles. During this mode, since S-counter is idle, transistors M6 and M7 which are controlled by MOD, keep the nodes S1 and S2 at logic "0," thus saving the switching power in S-counter for a period of (N*(P-S)) clock cycles. Here, the programmable input (PI) is used to load the counter to a specified value from 0 to 31 for the lower band and 0 to 48 for the higher band of operation.

B. Programmable (P) Counter

The programmable P-counter is a 7-bit asynchronous down counter which consists of 7 loadable bit-cells [13] and additional logic gates as in [7]. Here, bit P7 is tied to the Sel signal of the multimodulus prescaler and bits P4 and P7 are always at logic "1." The remaining bits can be externally programmed from 75 to 78 for the lower frequency band and from 105 to 122 for the upper frequency band. When the S-counter finishes counting down to zero, LD switches to logic "1" during which the output of all the bit-cells in S-counter switches to logic "1" and output of the NOR embedded DFF switches to logic "0" (MOD=0)where the programmable divider get reset to its initial state and thus a fixed division ratio is achieved. If a fixed dual-modulus prescaler is used, a 7-bit _-counter is needed for the low-frequency band (2.4 GHz) while an 8-bit P-counter would be needed for the high-frequency band (5–5.825 GHz) with a fixed 5-bit S-counter. Thus, the multimodulus 32/33/47/48 prescaler eases the design complexity of the P-counter.

1) Sel=0 (2.4–2.484 GHz): When logic signal Sel=0, the multimodulus prescaler acts as a 32/33 prescaler, the S-counter is programmable from 64 to 127 (bit Pt of the P-counter always remains at logic "1"), and the P-counter is programmable from 0 to 31 to accommodate division ratios from 2048 to 4095 with finest resolution of 1 MHz However, since we are interested in the 2.4-GHz band, bit Po of the P-counter always remains at logic "0," since it is tied to the logic signal Sel, allowing it to be programmable from 75 to 78. Bit S6 of the S-counter is kept at logic '0' (to satisfy the conditions N>S), allowing a programmable division from 0 to 31 for the low-frequency Fig. 7. Die photograph of the proposed multiband divider. band of operation to accommodate division ratios between 2400 and 2484 with a resolution of 1 MHz for Bluetooth and Zigbee applications [7] and 5 MHz for the IEEE 802.15.4 frequency synthesizer [8] with a fixed reference frequency of 1 MHz Since the finest resolution and reference frequency is 1 MHz; different channel spacing can be achieved by programming S-counter in steps of 1. For example, a 5-MHz channel spacing is achieved by programming S-counter in steps of "5" keeping the flexible divider resolution and reference frequency to 1 MHz The frequency division (FD) ratio of the multiband divider in this mode is given by

$$FD=(N+1)*S+N*(P-S)=NP+S \text{ (10)}$$

2) Sel= (5–5.825 GHz): When logic signal Sel=1 , the multimodulus prescaler acts as a 47/48(N/(N+1)) prescaler, the P-counter is programmable from 64 to 127 (bit P7 of the P-counter always remains at logic "1"), and the S-counter is programmable from 0 to 48 to accommodate division ratios from 3024 to 6096 with finest resolution of 1 MHz However, since we are interested in 5–5.825 GHz band, bit P6 of the P-counter always remains at logic "1," allowing it to be programmable from 105 to 122. The S-counter is programmable from 0 to 48 for the high frequency band of operation to accommodate division ratios between 5000 and 5825 with a resolution of 5 MHz, 10 MHz or 20 MHz for IEEE 802.11a/b/g synthesizers [1]–[3], [6],[9].Since finest resolution and reference frequency is 1 MHz, S-counter is programmed in steps of '5', '10' or '20', and _-counter programmed from 105 to 122 in steps of '1' to provide channel spacing of 5 MHz, 10MHz or 20 MHz The frequency division (FD) ratio of the multiband divider in this mode is given by $FD=(N*S)+(N+1)*(P-S)=(N+1)P-S$ (11)

SIMULATIONS AND SILICON VERIFICATIONS

The simulations of the designs are performed using Cadence SPECTRE RF for a 0.18um CMOS process. The simulation results show that the wide band 2/3 prescaler has the maximum operating frequency of 8 GHz with a power consumption of 0.92 and 1.73 mW during the divide-by-2 and divide-by-3 modes, respectively. The proposed wide band multimodulus prescaler has the maximum operating frequency of 7.2 GHz (simulation) with power consumption of 1.52, 1.60, 2.10, and 2.13 mW during the divide-by-32, divide-by-33, divide-by-47 and divide-by-48, respectively. For silicon verification, the multiband divider is fabricated using the Global Foundries 1P6M 0.18-m CMOS process and the die photograph is shown in Fig. 7. On-wafer measurements are carried out using an 8 inch RF probe station. The input signal for the measurement is provided by the 83650B 10 MHz-50 GHz HP signal generator and the output signals are captured by the Lecroy Wavemaster 8600A 6G oscilloscope. The measurement results shows that the wideband 2/3 prescaler has a maximum operating frequency of 6.5 GHz [10] and the multimodulus.

Design Parameters	[6]	[12]	This work
Process (μm)	0.18	0.18	0.18
supply voltage (V)	1.8	1.8	1.8
Max.Frequency (GHz) (Sim/Measured)	6.7 / -	7.5 / 6	8 / 6.5
Power(mW) (sim/measured) Divide-by-2 mode	1.88 / -	1.63 / 2.2	0.82 / 0.97
Power(mW) (sim/measured) Divide-by-3 mode	2.18 / -	1.85 / 2.62	1.61 / 1.78

Table I Performance of different 2/3 prescalers at 2.5 GHz.

(a)
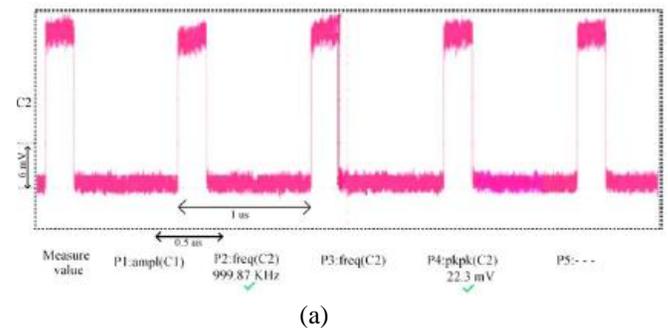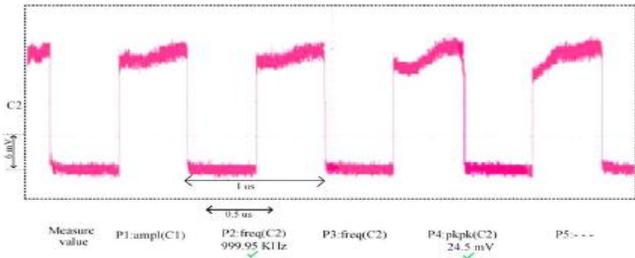
(b)

Fig. Measured results of a dual-band divider. (a) 2.4-GHz band. (b) 5-GHz band.

32/33/47/48 prescaler designed using wideband 2/3 prescaler has maximum operating frequency of 6.2 GHz. However, the maximum operating frequency that can be achieved by the multimodulus 32/33/47/48 prescaler is limited by the wideband 2/3 prescaler. Table I shows the performance of proposed 2/3 prescaler and prescalers reported in [6] and [12] (resimulated). The performance of the multiband flexible divider is measured in both the lower frequency and higher frequency bands by programming the P- and S-counters. Fig. 8(a) shows the measured output waveform of the multiband divider at an input frequency of 2.47 GHz where P,S-counters are programmed to have values 77 and 6 respectively (FD=2470). Fig. 8(b) shows the measured output waveform of the multiband divider at an input frequency of 5.818 GHz where P-counters are programmed to have values 122 and 38, respectively (FD=5818). The proposed multiband flexible divider consumes an average power of 0.96 mW during lower frequency band (2.4–2.484 GHz), while it consumes 2.2 mW during the high-frequency band (5–5.825 GHz) of operation compared to the dual-band divider reported in [9], which consumes 2.7 mW at 1-V power supply. The proposed multiband divider has a variable resolution of K-MHz for lower frequency band (2.4–2.484 GHz) and for the higher frequency

Band (5–5.825 GHz), where K is integer from 1 to 5 for 2.4-GHz band and 5, 10, and 20 for WLAN applications. Table II shows the performance of different dividers.

Reference	[9]	[6]	This work
process (μm)	0.18	0.25	0.18
supply voltage (V)	1.0	1.8	1.8
Frequency range (GHz)	2.4-2.7 / 5.14-5.7	5.14-5.7	2.4-2.484 / 5-5.825
Resolution (MHz)	9.375 / 20	20	1,2,5,10,20
Power(mW)	2.7	6.25	0.96 / 2.2

Table. II. Performance of different dividers.

CONCLUSION

In this paper, a wideband 2/3 prescaler is verified in the design of proposed wide band multimodulus 32/33/47/48 prescaler. A dynamic logic multiband flexible integer-N divider is designed which uses the wideband 2/3 prescaler, multimodulus 32/33/47/48 prescaler, and is silicon verified using the 0.18um CMOS technology. Since the multimodulus 32/33/47/48 prescaler has maximum operating frequency of 6.2 GHz, the values of P- and S-counters can actually be programmed to divide over the whole range of frequencies from 1 to 6.2 GHz with finest resolution of 1 MHz and variable channel spacing. However, since interest lies in the 2.4- and 5–5.825-GHz bands of operation, the P- and S-counters are programmed accordingly. The proposed multiband flexible divider also uses an improved loadable bit-cell forSwallow _-counter and consumes a power of 0.96 and 2.2 mW in 2.4- and 5-GHz bands, respectively, and provides a solution to the low power PLL synthesizers for Bluetooth, Zigbee, IEEE 802.15.4, and IEEE 802.11a/b/g WLAN applications with variable channel spacing.

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