ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

Design and Performance analysis of Reversible logic multiplexer using Nano-scale Technology

Jasmine
M.Tech (VLSI System Design),
Department of Electronics and Communication Engineering,
Institute of Aeronautical Engineering.

P.S.Krishna
Assistant Professor,
Department of Electronics and Communication Engineering,
Institute of Aeronautical Engineering.

Abstract:

Reversible logic has emerged as one of the most important approaches and more prominent technology having its applications in Low Power CMOS, Quantum Computing, Garbage inputs/outputs, Cryptography, Communication, nanotechnology, Optical Computing and Computer graphics. This paper presents a novel reversible multiplexer gate is proposed and the design of differential reversible multiplexer using the proposed reversible gate is discussed. The results of the proposed design show that the circuits are more optimized in terms of delay, power supply (0.7V) and voltage gain (0.76V). The power dissipation, power-delay and propagation delay produced using the new design are analyzed and compared with those of other design simulations. The results show that the proposed Reversible multiplexer has both lower power consumption and a lower Power-Delay Product (PDP) value (2.384×10-25 joule), frequency response 50.0 MHz's .The transistor implementation of the proposed gates is done by using Virtuoso tool of cadence.

INTRODUCTION:

An integrated circuit is an electronic circuit in which many devices such as transistors, diodes, resistors, capacitors etc., are fabricated on a single small silicon chip. It is different from a discrete circuit, which is built by connecting separated devices. In this case each device is fabricated separately and then all the devices are assembled together to make an electronic circuit. Integrated circuits are produced by using the same processes as those for manufacturing transistors and diodes etc.

The different components in an IC are isolated from each other by isolation diffusion with in the silicon chip and are interconnected by an aluminum layer that serves as a wire.In integrated circuit design, physical design is a step in the standard design cycle which follows after the circuit design. At this step, circuit representations of the components (devices and interconnects) of the design are converted into geometric representations of shapes which, when manufactured in the corresponding layers of materials, will ensure the required functioning of the components. This geometric representation is called integrated circuit layout.

This step is usually split into several sub-steps, which include both design and verification and validation of the layout.The rapid technology advances in Integrated circuits (ICs) technology accelerated during and after 1980's and one of the most influential factors for such a rapid advance in technology scaling, that is, the reduction in MOS transistor feature size. The MOS feature size is typically measured by the MOS transistor channel length. During the last 24 years the minimum features size has evolved from 6 to 0.35μm by the year 2000, the minimum feature size is 0.18 μm after the year 2010 the size has evolved from nano meter technology.

REVERSIBLE CIRCUIT TYPES:

To implement reversible computation, estimate its cost, and to judge its limits, it is formalized it in terms of gate-level circuits. For example, the inverter (logic gate) (NOT) gate is reversible because it can be undone.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

The exclusive or (XOR) gate is irreversible because its inputs cannot be unambiguously reconstructed from an output value. However, a reversible version of the XOR gate—the controlled NOT gate (CNOT)—can be defined by preserving one of the inputs. The three-input variant of the CNOT gate is called the Toffoli gate. It preserves two of its inputs a,b and replaces the third c by . With , this gives the AND function, and with this gives the NOT function. Thus, the Toffoli gate is universal and can implement any reversible Boolean function (given enough zero-initialized ancillary bits).

More generally, reversible gates have the same number of inputs and outputs. A reversible circuit connects reversible gates without fan-outs and loops. Therefore, such circuits contain equal numbers of input and output wires, each going through entire circuit Reversible logic circuits have been first motivated in the 1960s by theoretical considerations of zero-energy computation as well as practical improvement of bit-manipulation transforms in cryptography and computer graphics. Since the 1980s, reversible circuits have attracted interest as components of quantum algorithms, and more recently in photonic and nano-computing technologies where some switching devices offer no signal gain.

The basic building blocks of the adder circuits that are designed are initially coded and simulated to verify its functionality. The ripple carry adder is designed, simulated and synthesized. The circuit delay, number of gates, garbage output and power dissipation is found out. The comparison of ripple carry adder designed using basic gates and the ripple carry adder designed using reversible gates, with respect to power dissipation and delay is done.

EXISTING METHOD:

Reversible multiplexer using passes transistor:

A. Designing reversible Multiplexer using pass Transistor which has two inputs A,B and one select input S, the output of the circuit is Y as shown in below figure 3. We can implement many combination circuits using this 2:1 reversible multiplexer, adder, Subtractor, multiplier, etc. Pass transistors are used to design the circuit voltage reduction in present circuit. Functionality of two transistor multiplexer shown below.

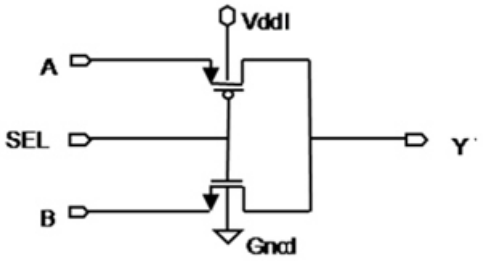

Fig. Multiplexer uses pass transistor

Select	Output
0	A
1	B

Table: Functional Table of reversible 2:1 Multiplexer

Drawbacks:

In order to discuss new trends and projects in the area of reversible logic one must first have an understanding of what this is. First of all, we'll restrict our discussion of logic functions to two-valued functions describing switching logic. Energy loss is an important consideration in digital circuit design, also known as circuit synthesis. Higher levels of integration and the use of new fabrication processes have dramatically reduced the heat loss over the last decades.

Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces the number of active devices, but has the disadvantage that the difference of the voltage between high and low logic levels decreases at each stage. Each transistor in series is less saturated at its output than at its input. This can be overcome by using logic gates in which also power dissipation decreases.

PROPOSED METHOD:

The key components of communication systems are a multiplexer (Mux, parallel-to-serial converter) and a Demultiplexer (DeMux, serial-to-parallel converter). In conventional computers, the computation carrying out is irreversible i.e. once logic block generates the output bits, the input bits are lost. But it is not in the case of reversible logic circuits. The classical set of gates such as AND, OR, and EXOR are not reversible as they are all multiple-input single output logic gates.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

A gate is reversible if the gate's inputs and outputs have a one-to-one correspondence, i.e. there is a distinct output assignment for each distinct input. Therefore, a reversible gate's inputs can be uniquely determined from its outputs. Reversible logic gates must have an equal number of inputs and outputs. Then the output rows of the truth table of a reversible gate can be obtained by permutation of the input rows. Reversible logic circuits have emerged as a promising technology in the field of information processing.

Irreversible hardware computation results in energy dissipation due to information loss. According to the Landauer , traditional irreversible hardware computation inevitably leads to energy dissipation due to the loss of each one bit of information which dissipates an amount of KT ln(2) joules of energy, where K is the Boltzmanns constant and T is the absolute temperature at which computation is performed. This erasure is not done significantly and more power is dissipated for each erased bit. Power dissipation which leads to overheating is one of the major concerns in modern technologies. Thus, an alternative logic operation known as reversible logic came into existence, which does not erase information and also dissipate arbitrarily less heat.

Charles Bennett proposed a theoretical background which proved that reversible general purpose computing device scan be built. This gave rise to reversible logic circuits. Logical reversibility means that after finishing a computation, it is possible to retrace every step and reconstruct data which was used in every step. Thus, reversible logic circuits offer an alternative that allows computation with very small energy dissipation .There is number of existing reversible gates in literature like Fredkin, Feynman and Toffoli gates etc.

Experimental reversible chips and arithmetic circuits have been developed recently as well as magnetic, Josephson junction, nano-electronic and quantum implementations of reversible logic circuits have been proposed in different literatures. Photon being the ultimate unit of information with unmatched speed and with data package in a signal of zero mass, the techniques of computing with light may provide a way out of the limitations of computational speed and complexity inherent in electronics computing. Different optical logic gates have already been proposed to perform irreversible logic function.

But, reversible computation in a system can be performed if the system is composed of reversible gates. The well known 2x2 Feynman gate operates as a controlled NOT (CNOT) if the control input of CNOT is set ,,0, the gate acts as a BUFFER gate; else, it acts as a NOT gate. The Feynman gate can be used as fan-out gate to copy a signal. Toffoli and Fredkin gates are 3x3reversible gates. Each of these gates is universal, i.e. any logical reversible circuit can be implemented using these gates.

BASIC REVERSIBLE LOGIC GATE:

A set of reversible logic gates is needed to design reversible logic circuits. An N*N reversible logic gate can be represented as:

IV = (I1, I2……., IN) (1)

OV = (O1, O2……., ON)

Where, Iv and Ov are inputs and output vectors. Consider following issues to perform synthesis of reversible gates and obtain optimization

DESIGN OF REVERSIBLE MULTIPLEXER:

We design the reversible circuit using dual-line pass-transistor logic [1] and monotone circuit. Boolean values X=1 and X=0 are denoted by (X,X)=(1,0) and (X,X)=(0,1), respectively. For example, an inverter is shown in Fig 1. It consists of a metal cross-over. Because of the monotone circuit, we set all initial values (X, X) = (0, 0).

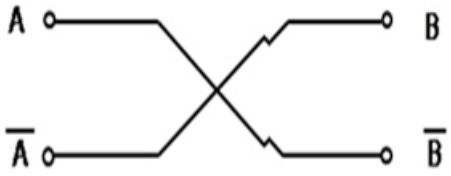

Figure.3.1 Reversible inverter

Transmission gate:

For the implementation of an on-off switch, we use a CMOS transmission gate which is a two-way switch shown in Figure. It is possible to compute logic functions without making logic gates – networks of MOS transistors can be connected together directly. These are known as transmission gates. (Of course, the transistors still have gates, but that is a different use of the word, as also would be logic gates!).

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

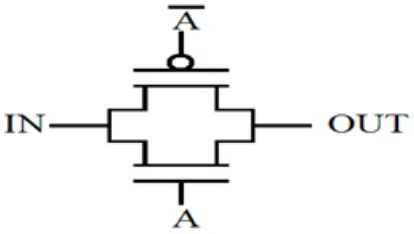

Figure3.2.CMOS Transmission gate

With CMOS, the nMOS transistors are good at conducting low signals and the pMOS transistors are good at conducting high signals, so transmission gates are often made from a pair of complementary transistors. When the control signal S is high, the transmission gate conducts logic signals of either sense in either direction. A special symbol is used for the CMOS transmission gate which is shown below The equivalence with the original equations is easily verified.

The corresponding adder design, using complementary static CMOS and the gate level implementation is shown in Fig It requires 28transistors. In addition to consuming a large area, this circuit is slow. The Proposed reversible is realized using transistor implementation as described previously. The required output Y can be obtained using only two transistors however, the three transistors are required for calculating garbage outputs. To obtain output G1, a Pass Transistor is used for passing the selection input S (select) to the output G1 as shown below.

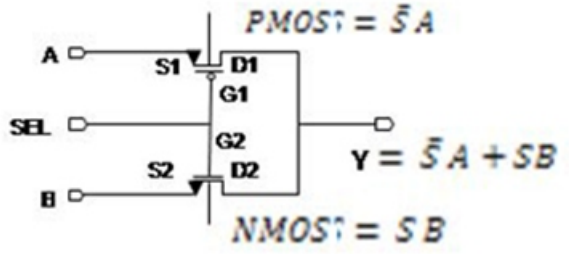

Fig. Circuit diagram for multiplexed output Y.

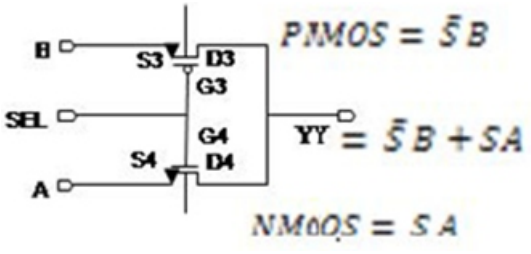

Fig. circuit diagram for output G2.

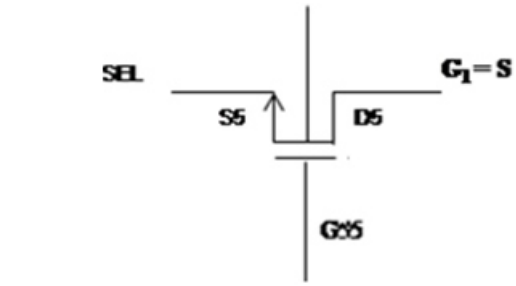

Fig. Circuit diagram for output G1.

RESULTS:

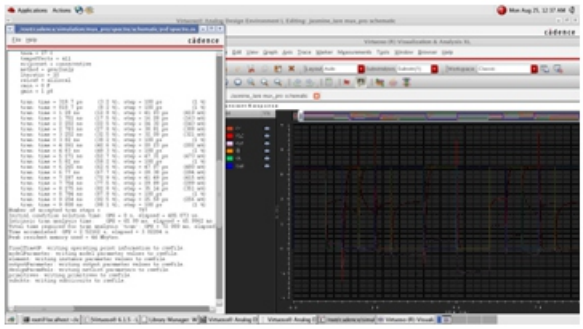

Fig: Shows the without compensated circuit voltage drop for selected s.

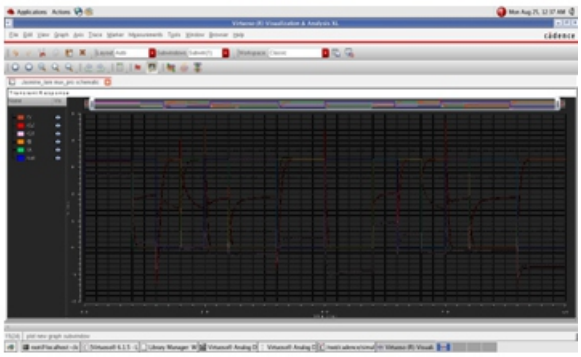

Fig: Shows the without compensated circuit voltage drop for pass transistor.

Fig: shows the response of particular mux_pass transistors.

ISSN No: 2348-4845
International Journal & Magazine of Engineering, Technology, Management and Research
A Peer Reviewed Open Access International Journal

CONCLUSION:

By adopting the proposed System the Multiplexer by using the pass transistor in which the impact of delay of the normal logic gates and also requires the large area. The proposed system is implemented by using CADENCE VIRTUOSO tool with 45nm CMOS TECHNOLOGY. This project elucidate a novel reversible gate and the design of reversible multiplexer like 2:1 using the proposed reversible gate is discussed. The result of circuits is more optimized in terms of delay, power supply, power and delay product and voltage gain. This project worked and calculates the result in two technologies 180 and 45 nm and compared leakage power, decrease delay in 45 nm in comparison 180 nm.

REFERENCES:

[1]. T. Toffoli., "Reversible Computing," in Automata, Languages and Programming, J. W. Bakker and J. van Leeuwen, ED. Springer Verlag, 1980, pp. 632-644.

[2]. H. Bennett, "Logical reversibility of computation," IBM J. Research and Development, vol. 17, pp. 525-532, 1973

[3]. Landauer, R., 1961. Irreversibility and heat generation in the computing process, IBM J.Research and Development, 5 (3): 183191.

[4]. M. P Frank, "Introduction to reversible computing: motivation, progress, and challenges", Proceedings of the 2nd Conference on Computing Fron-tiers, 2005, pages 385–390.

[5].VlatkoVedral, Adriano Bareno and ArturEkert, "Quantum Networks for Elementary Arithmetic Operations", arXiv: quantph/ 9511018 v1, Nov 1995.

[6].Perkowski.M,Jozwiak.L,Kerntopf.P,Mishchenko.A, Al-Rabadi.A, Coppola.A, Buller.A, Song. X, Khan. M.M.H.A, Yanushkevich.S, Shmerko.V, and Chrzanowska-Jeske.M.2001. "A general decomposition for reversible logic", In 5th International Reed-Muller Workshop,Starwille, pp. 119-138.

[7]. Hafiz Md. Hasan Babu and Chowdhury.A.R, 2005. "Design of Reversible Binary coded Decimal adder by using Reversible 4- bit parallel Adder",VLSI Design 2005, pp. 255-260.

[8].W.N. N. Hung, X. Song, G. Yang, J. Yang, and M. Perkowski, "Optimal Synthesis of Multiple Output Boolean Functions Using a Set of Quantum Gates by-Symbolic Reachability Analysis", IEEE Trans. Computer-Aided Design, Vol. 25, No. 9,pp.1652-1663,Sep 2006.