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A New Advanced 9-Level Multi-Level Topology Fed Induction Machine Drive Application

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Abstract: ***Multilevel inverter utilization has been increased since the last decade. These new type of inverters are suitable in various high voltage and high power applications due to their ability to synthesize waveforms with better harmonic spectrum and faithful output. Among the three topologies, the cascaded multilevel inverter has the potential to be the most reliable and achieve the best fault tolerance owing to its modularity, a feature that enables the inverter to continue operating at lower power levels after cell failure. Modularity also permits the cascaded multilevel inverter to be stacked easily for high power and high-voltage applications. Cascaded H-Bridge Seven & Nine level inverter fed Induction machine drive using low frequency transformer with single DC Source is proposed. This paper is particularly focused on the 9-level inverter with the requirement of low switching components. In the proposed topology only 7 switches were used. The harmonic reduction is achieved by selecting appropriate switching angles. It shows hope to reduce initial cost and complexity hence it is apt for industrial applications.***

Keywords **–** ***Multilevel Inverter, MATLAB, THD and RV Technique, Induction Motor Drive.***

I INTRODUCTION

Large electric drives and utility applications require advanced power electronics inverter to meet the high power demands. As a result, power inverter structure has been introduced as an alternative in high power and medium voltage situations. Basically Inverter is a device that converts DC power to AC power at desired output voltage and frequency. Demerits of inverter are less efficiency, high cost, and high switching losses. To overcome these demerits, we are going to multilevel inverter. The term Multilevel began with the three-level converter. The concept of multilevel converters has been introduced since 1975. The cascade multilevel inverter was first proposed in1975 [1]. Multilevel inverter output voltage produce a staircase output waveform, this waveform look like a sinusoidal waveform.

The multilevel inverter output voltage having less number of harmonics compare to the conventional bipolar inverter output voltage. If the multilevel inverter output increase to N level, the harmonics reduced to the output voltage value to zero. The multi level inverters are mainly classified as Diode clamped, Flying capacitor inverter and cascaded multi level inverter. The cascaded multilevel control method is very easy when compare to other multilevel inverter because it doesn't require any clamping diode and flying capacitor [2]. The term multilevel began with the three level converters [3]-[5]. Subsequently, several multilevel converter topologies have been developed [6]. However, the elementary concept of a multilevel converter to achieve higher power is to use a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a stair case voltage waveform. Capacitors, batteries and renewable voltage sources can be used as the multiple dc voltage sources.

The most common initial application of multilevel converters has been in traction, both in locomotives and track -side static converters. More recent applications have been for power system converters for VAR compensation and stability enhancement, active filtering, high-voltage motor drive, high-voltage dc transmission, and most recently for medium voltage induction motor variable speed drives. As alternatives to effectively solve the above -mentioned problems, several circuit topologies of multilevel inverter and

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converter have been researched and utilized. The output voltage of the multilevel inverter has many levels synthesized from several DC voltage sources. The quality of the output voltage is improved as the number of voltage levels increases, so the quantity of output filters can be decreased. A multilevel converter can be implemented in many different ways. The simplest techniques involve the parallel or series connection of conventional converters to form the multilevel waveforms. More complex structures effectively insert converters within converters. The voltage or current rating of the multilevel converter becomes a multiple of the individual switches, and so the power rating of the converter can exceed the limit imposed by the individual switching devices.

In this paper, a novel cascaded H- bridge multilevel inverter has been proposed using less number of switches. A standard cascaded multilevel inverter requires 4h number of switches for (2h + 1) levels whereas h is the number of dc sources. Multilevel inverters supplied from equal and constant dc sources almost don't exist in practical applications. The variation of the dc sources affects the values of the switching angles required for each specific harmonic profile, as well as increases the difficulty of the harmonic elimination's equations. The emergence of multilevel inverters has been in increase since the last decade. These new types of converters are suitable for high voltage and high power application due to their ability to synthesize waveforms with better harmonic spectrum. Finally the proposed topology is implemented with SHE [7] [8]. The THD values for the Traditional, Conventional and Proposed inverters are compared and analyzed.

II. H-BRIDGE MULTILEVEL INVERTER

The traditional two or three levels inverter does not completely eliminate the unwanted harmonics in the output waveform. Therefore, using the multilevel inverter as an alternative to traditional PWM inverters is investigated. In this topology the number of phase voltage levels at the converter terminals is 2N+1, where N is the number of cells or dc link voltages.

In this topology, each cell has separate dc link capacitor and the voltage across the capacitor might differ among the cells. So, each power circuit needs just one dc voltage source. The number of dc link capacitors is proportional to the number of phase voltage levels .Each H bridge cell may have positive, negative or zero voltage. Final output voltage is the sum of all H-bridge cell voltages and is symmetric with respect to neutral point, so the number of voltage levels is odd.

Cascaded H-bridge multilevel inverters typically use IGBT switches. These switches have low block voltage and high switching frequency. Consider the seven level inverter; it requires 12 IGBT switches and three dc sources. A cascaded H-bridge multilevel inverter is simply a series connection of multiple H-bridge inverters. Each H-bridge inverter has the same configuration as a typical single-phase full-bridge inverter. The cascaded H-bridges multilevel inverter introduces the idea of using Separate DC Sources (SDCSs) to produce an AC voltage waveform. Each H-bridge inverter is connected to its own DC source Vdc. By cascading the AC outputs of each H bridge inverter, an AC voltage waveform is produced.

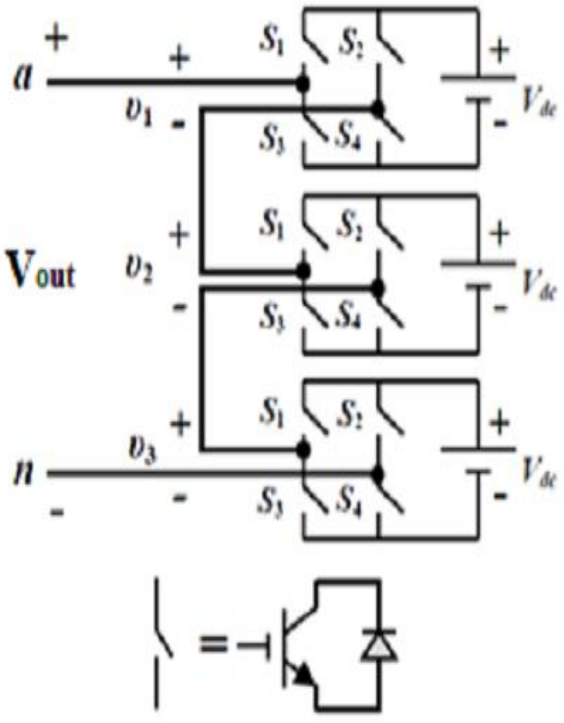

Fig 1. Cascaded H-bridge 7-level Inverter

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By closing the appropriate switches, each H-bridge inverter can produce three different voltages: +Vdc, 0 and -Vdc.

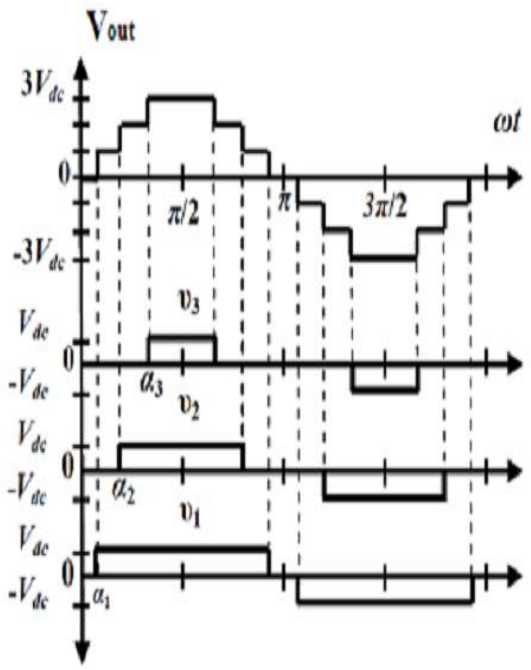

Fig 2. Output Voltage of cascaded H-bridge seven level inverter

It is also possible to modularize circuit layout and packaging because each level has the same structure, and there are no extra clamping diodes or voltage balancing capacitors. The number of switches is reduced using the new topology.

This circuit is simulated using the MATLAB software. The results are shown in the later sections in detail.

III.PROPOSED TOPOLOGY

The main objective is to improve the quality output voltage of the multilevel inverter with reduced number of switches. An important issue in multilevel inverter design is that to generate nearly sinusoidal output voltage waveform and to eliminate lower order harmonics. A key concern in the fundamental switching scheme is to determine the switching angles in order to produce the voltage with fundamental frequency.

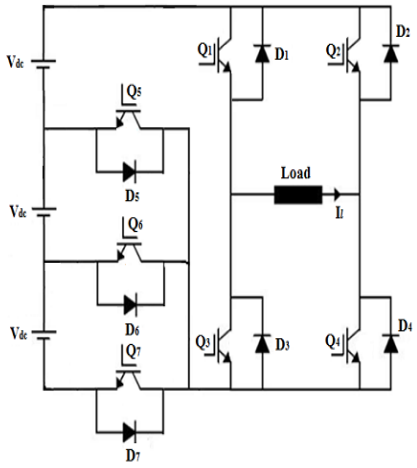

Fig 3 Proposed Power circuit for 7-level output.

There are three modes of operation for the proposed 7-level multilevel inverter. These modes are explained as below. Powering Mode: This occurs when both the load current and voltage have the same polarity. In the positive half cycle, when the output voltage is V_{dc}, the current pass comprises; the lower supply, D6, Q1, load, Q4, and back to the lower supply. When the output voltage is 2Vdc, current pass is; the lower source, Q5, the upper source, Q1, load, Q4, and back to the lower source. When the output voltage is 3Vdc, the current pass comprises: upper supply, Q1, load, Q4, Q7, lower supply. In the negative half cycle, Q1 and Q4 are replaced by Q2 and Q3 respectively. Free-Wheeling Mode Free-wheeling modes exist when one of the main switches is turned-off while the load current needs to continue its pass due to load inductance. This is achieved with the help of the anti-parallel diodes of the switches, and the load circuit is disconnected from the source terminals. In this mode, the positive half cycle current pass comprises; Q1, load, and D2 or Q4, load, and D3, while in the negative half cycle the current pass includes Q3, load, and D4 or Q2, load, and D1.Regenerating Mode In this mode, part of the energy stored in the load inductance is returned back to the source. This happens during the intervals when the load current is negative during the positive half cycle and vice-versa, where the output voltage is zero. The positive current pass comprises; load, D2, Q6, the lower source, and D3, while the negative current pass comprises; load, D1, Q6, the lower source, and D4. From the figure 4 switching pattern for the various switches are explained. In this paper fundamental frequency switching scheme is employed which reduces the

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switching losses. Because the switching frequency is less in this method when compared to the other methods. Switching losses are directly proportional to the switching frequency.

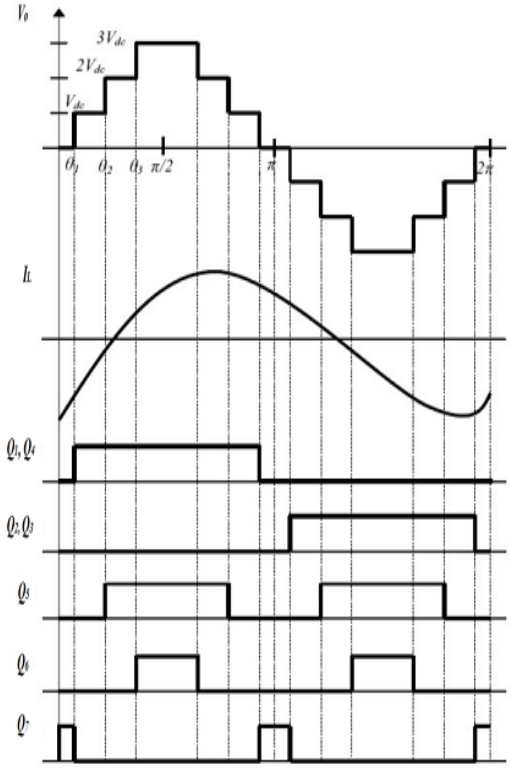

Fig 4 Waveforms of the proposed seven level inverter

IV.SELECTIVE HARMONICS ELIMINATION

The Selective Harmonic Elimination Stepped-Waveform (SHESW) technique is very suitable for a multilevel inverter circuit. Employing this technique along with the multilevel topology, the low Total Harmonic Distortion THD output waveform without any filter circuit is possible.

A. Fourier Series and Harmonics Elimination Theory

After applying Fourier theory to the output voltage waveform of multilevel converters, which is odd quarter-wave symmetric, we can find the Fourier expression of the multilevel output voltage as (1). If the DC voltages are equal in the multilevel converter, the equation for the fundamental frequency switching control method can be expressed as:

$$V(t) = \sum_{n=1,3,5.....}^{\infty} \frac{4V_{dc}}{n\pi} (\cos(n\theta_1)(\cos(n\theta_2) + cos(n\theta_3) + \cdots + (\cos(n\theta_s)) \sin(nwt) \quad (1)$$

From the equation, it can be seen that the output voltage has no even harmonics because the output voltage waveform is odd quarter-wave symmetric. It also can be seen from (2) that the peak values of these odd harmonics are expressed in terms of the switching angles θ_1, θ_2, and θs. Furthermore, the harmonic equations produced from (2) are transcendental equations. Based on the harmonic elimination theory, if one wants to eliminate the nth harmonic, then

$$\text{Cos } (n\theta_1) + \text{Cos } (n\theta_2) + ... + \text{Cos } (n\theta_s) = 0 \quad (2)$$

That means to choose a series of switching angles to let the value of the nth harmonic be zero. Therefore, an equation with s switching angles will be used to control the s different harmonic values. Generally, an equation with s switching angles is used to determine the fundamental frequency value, and to eliminate s-1 low order harmonics. For an equation with three switching angles, (2) becomes

$$V(t) = \sum_{n=1,3,5.....}^{\infty} \frac{4V_{dc}}{n\pi} (\cos(n\theta_1)(\cos(n\theta_2) + (\cos(n\theta_s)) \sin(nwt) \quad (3)$$

B. Transcendental Equations to Solve

In this paper we derived harmonic equations for eliminating the 3rd and 5th order harmonics. The resulting harmonic equations are:

$$\text{Cos } (n\theta_1) + \text{Cos } (n\theta_2) + \text{Cos } (n\theta_3) = \frac{\pi V_l}{4V_{dc}} \quad (4)$$

$$\text{Cos } (3\theta_1) + \text{Cos } (3\theta_2) + \text{Cos } (3\theta_3) = 0 \quad (5)$$

$$\text{Cos } (5\theta_1) + \text{Cos } (5\theta_2) + \text{Cos } (5\theta_3) = 0 \quad (6)$$

To simplify the expression, (4) can be written as

$$\text{Cos } (\theta_1) + \text{Cos } (\theta_2) + \text{Cos } (\theta_3) = m \quad (7)$$

Where

$$M = \frac{\pi V_l}{4V_{dc}} \quad (8)$$

These harmonic equations (4)-(6) are transcendental equations. They are difficult to solve without using some sort of numerical iterative technique. Here Newton Raphson method is employed for solving these equations.

C. Solving the Harmonic Equations using Newton Raphson Method

To solve the harmonic equations by resultant theory, they must be changed into polynomials. First, change the variables,

$$X_1 = \text{Cos } (\theta_1) \quad (9)$$

$$X_2 = \text{Cos } (\theta_2) \quad (10)$$

And

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$$X_3 = \text{Cos}(\theta_3) \quad (11)$$

Also, use the following trigonometric identities:

$$\text{Cos}(3\theta) = 4\cos^2(\theta) - 3\cos(\theta) \quad 12)$$

$$\text{Cos}(3\theta) = 3\cos(\theta) - 20\cos^2(\theta) + 10\cos^3(\theta) \quad (13)$$

Then, apply them to the transcendental harmonic equations above, and the following polynomial harmonic Equations can be found. For the fundamental frequency harmonic:

$$P_1(x_1, x2, x3) = \sum_{n=1}^{s} X_n - m = 0 \quad (14)$$

For the 3rd harmonic:

$$P_1(x_1, x2, x3) = \sum_{n=1}^{s} (4X_n^2 - 3X_n) = 0 \quad (15)$$

For the 5th harmonic:

$$P_1(x_1, x2, x3) = \sum_{n=1}^{s} 3X_n - 20X_n^2 + 20X_n^2 = 0 \quad (16)$$

The polynomial equations can be solved by using the Newton Raphson method. The following are steps for solving the equations. Substitute the initial guesses for variables. Then form the jacobian matrix with Newton's formula. Repeat the same steps until the solutions to converge. Thus the solutions obtained are given below

$$\theta_1 = 8.70033^0$$
$$\theta_2 = 28.0880^0$$
$$\theta_3 = 34.9895^0$$

V. MATLAB/SIMULINK RESULTS

Here simulation is carried out in different cases in that 1). Conventional Cascaded H-Bridge Multilevel Inverter 2). Proposed Symmetrical H-Bridge Multilevel Inverter 3). Proposed Advanced Multilevel Inverter Topology Fed Induction Machine Drive.

Case 1: Conventional Cascaded H-Bridge Multilevel Inverter

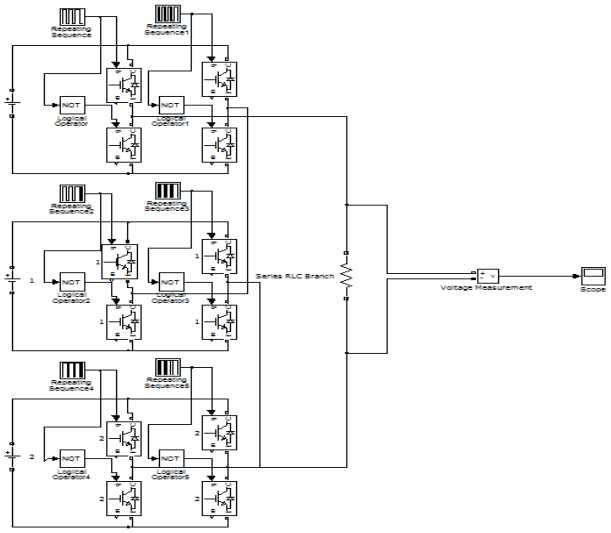

Fig.5 Matlab/Simulink Model of Conventional Cascaded H-Bridge Multilevel Inverter

Fig.5 shows the Matlab/Simulink Model of Conventional Cascaded H-Bridge Multilevel Inverter using Matlab/Simulink platform.

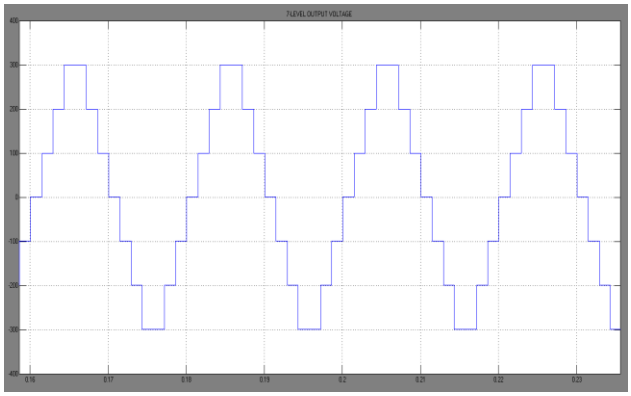

Fig.6 Seven Level Output Voltage

Fig.6 shows the Seven Level Output Voltage of Conventional Cascaded H-Bridge Multilevel Inverter.

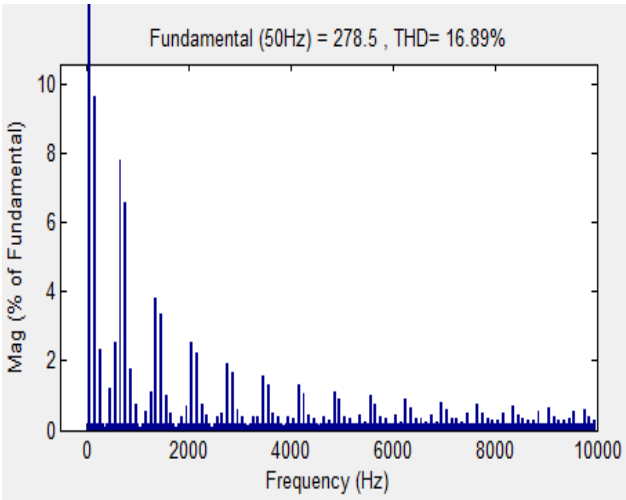

Fig.7 FFT Analysis of 7-Level Output Voltage

Fig.7 shows the FFT Analysis of 7-Level Output Voltage of Conventional Cascaded H-Bridge Multilevel Inverter, attains 16.89%.

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Case 2: Proposed Symmetrical H-Bridge Multilevel Inverter

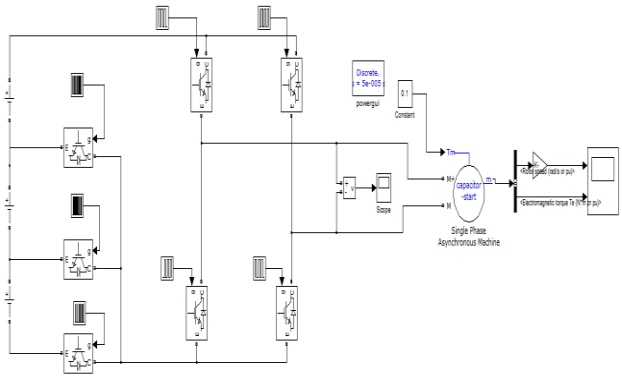

Fig.8 Matlab/Simulink Model of Proposed Symmetrical H-Bridge Multilevel Inverter

Fig.8 shows the Matlab/Simulink Model of Proposed Symmetrical H-Bridge Multilevel Inverter Fed Induction machine Drive application by using Matlab/Simulink platform.

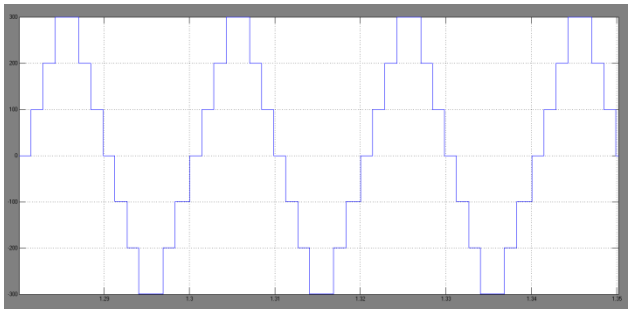

Fig.9 Seven Level Output Voltage

Fig.9 shows the Seven Level Output Voltage of Proposed Symmetrical H-Bridge Multilevel Inverter.

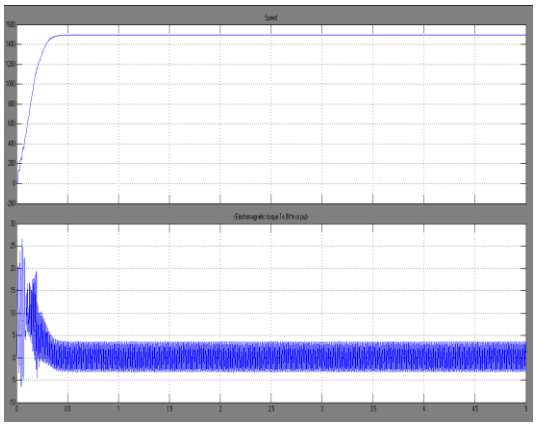

Fig.10 Speed & Torque

Fig.10 Speed & Torque of Proposed Symmetrical H-Bridge Multilevel Inverter Fed Induction machine Drive application.

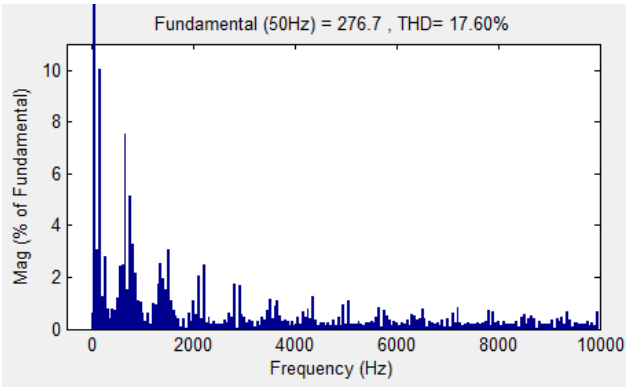

Fig.11 FFT Analysis of 7-Level Output Voltage

Fig.11 shows the FFT Analysis of 7-Level Output Voltage of Proposed Symmetrical H-Bridge Multilevel Inverter, attains 16.89%. Here THD response is near to formal one, but operating under low active switches, commercially so perfect.

Case 3: Proposed Advanced Multilevel Inverter Topology Fed Induction Machine Drive

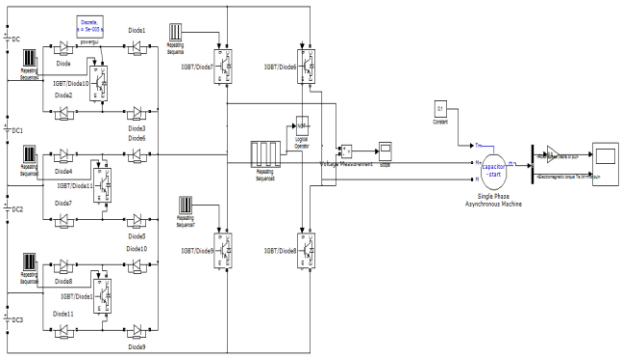

Fig.12 Matlab/Simulink Model of Proposed Advanced

Multilevel Inverter Topology Fed Induction Machine Drive

Fig.12 shows the Matlab/Simulink Model of Proposed Advanced Multilevel Inverter Topology Fed Induction Machine Drive application by using Matlab/Simulink platform.

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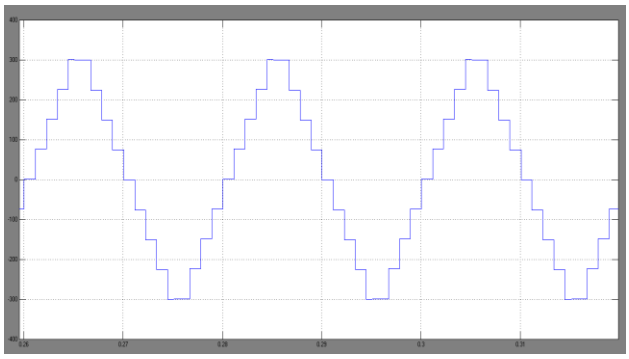

Fig.13 Nine Level Output Voltage

Fig.13 shows the 9-Level Output Voltage of Proposed Advanced Multilevel Inverter Topology Fed Induction Machine Drive.

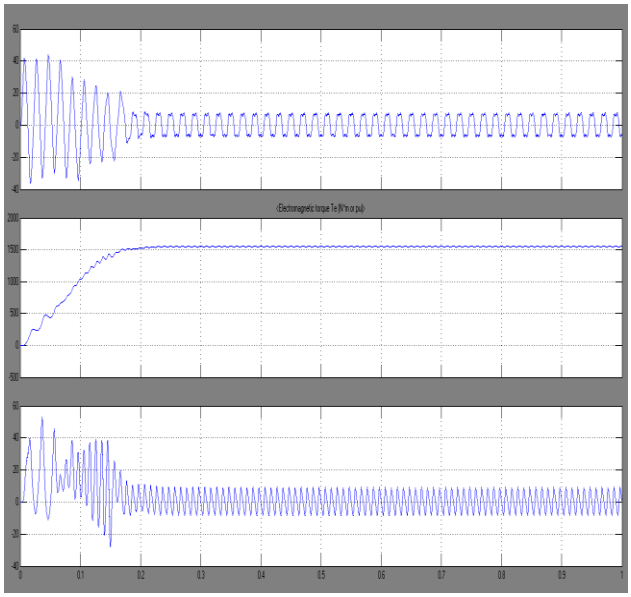

Fig.14 Speed & Torque and Stator Current

Fig.14 Speed & Torque, Stator Current of Proposed Advanced Multilevel Inverter Topology Fed Induction Machine Drive application.

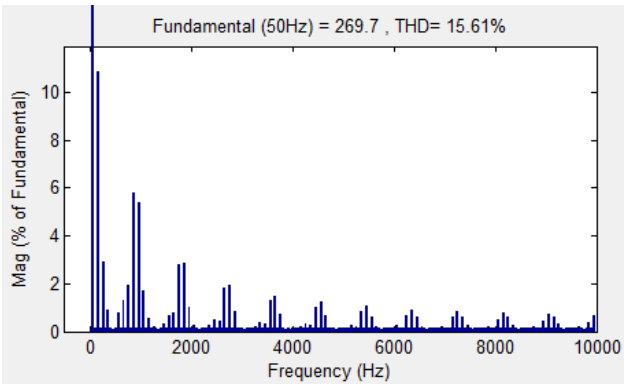

Fig.15 FFT Analysis of 9-Level Output Voltage

Fig.15 shows the FFT Analysis of 9-Level Output Voltage of Proposed Advanced Multilevel Inverter Topology Fed Induction Machine Drive, attains 15.61%. Here THD response is near to IEEE standards, no need of large size filter at output terminals. It is most advanced multilevel converter with low active switches and low THD values.

VI.CONCLUSION

In this paper, a new converter topology has been proposed which has superior features over conventional topologies in terms of the required power switches and isolated dc supplies, control requirements, cost, and reliability. This will add up to the efficiency of the converter as well as reducing the size and cost of the final prototype. Multi-level inverter technology has emerged recently as a very important alternative in the area of high-power high-voltage energy control. Multi-level inverters have been widely used for high-power high-voltage industrial applications. In this paper three different topologies of cascaded Multilevel Inverter has been simulated .Out of the above three topologies Existing Topology of advanced Multilevel Inverter is best based on the FFT analysis observed from the Simulation of all the Above Topologies. H-bridge MLI With single DC source is best if we consider Cost, switching Losses.

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