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Design of Low Power CMOS Comparator in UDSM Technology

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Abstract:

In modern digital VLSI design, domino logic style circuits are widely used. The CMOS domino logic circuit dissipates very low standby power and exhibits less area. We design a comparator circuit which uses footed domino logic and also implement a current mirror circuit in the design, to enhance the speed of the comparator. This paper emphasizes a CMOS comparator design to detect full match or mismatch of the binary input. The proposed design consumes low leakage power and had a higher speed, than other circuit. The delay, leakage power and average power of the proposed CMOS Comparator circuit have also been calculated and then it is compared with the Footed Domino Logic Comparator circuit with same parameter. The circuit has been simulated in 45nm CMOS technology on Cadence Tool for high fan-ins (4, 8, 16, 32& 64 bits).

INTRODUCTION:

An integrated circuit is an electronic circuit in which many devices such as transistors, diodes, resistors, capacitors etc., are fabricated on a single small silicon chip. It is different from a discrete circuit, which is built by connecting separated devices. In this case each device is fabricated separately and then all the devices are assembled together to make an electronic circuit. Integrated circuits are produced by using the same processes as those for manufacturing transistors and diodes etc. The different components in an IC are isolated from each other by isolation diffusion with in the silicon chip and are interconnected by an aluminum layer that serves as a wire.

In integrated circuit design, physical design is a step in the standard design cycle which follows after the circuit design. At this step, circuit representations of the components (devices and interconnects) of the design are converted into geometric representations of shapes which, when manufactured in the corresponding layers of materials, will ensure the required functioning of the components. This geometric representation is called integrated circuit layout. This step is usually split into several sub-steps, which include both design and verification and validation of the layout.

The rapid technology advances in Integrated circuits (ICs) technology accelerated during and after 1980's and one of the most influential factors for such a rapid advance in technology scaling, that is, the reduction in MOS transistor feature size. The MOS feature size is typically measured by the MOS transistor channel length. During the last 24 years the minimum features size has evolved from 6 to 0.35µm By the year 2000, the minimum feature size is 0.18 µm after the year 2010 the size has evolved from nano meter technology.

Current mirror circuit :

A current mirror is a circuit designed to copy a current through one active device by controlling the current in another active device of a circuit, keeping the output current constant regardless of loading. The current being 'copied' can be, and sometimes is, a varying signal current. Conceptually, an ideal current mirror is simply an ideal inverting current amplifier that reverses the current direction as well or it is a current-controlled current source (CCCS). The current mirror is used to provide bias currents and active loads to circuits.

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Basic MOSFET current mirror:

The basic current mirror can also be implemented using MOSFET transistors, as shown in Figure 2. Transistor M1 is operating in the saturation or active mode, and so is M2. In this setup, the output current IOUT is directly related to IREF, as discussed next. The drain current of a MOSFET ID is a function of both the gate-source voltage and the drain-to-gate voltage of the MOSFET given by ID = f (VGS, VDG), a relationship derived from the functionality of the MOSFET device. In the case of transistor M1 of the mirror, ID= IREF. Reference current IREF is a known current, and can be provided by a resistor as shown, or by a "threshold-referenced" or "self-biased" current source to ensure that it is constant, independent of voltage supply variations.

Using VDG=0 for transistor M1, the drain current in M1 is ID = f (VGS,VDG=0), so we find: f(VGS, 0) = IREF, implicitly determining the value of VGS. Thus IREF sets the value of VGS. The circuit in the diagram forces the same VGS to apply to transistor M2. If M2 is also biased with zero VDG and provided transistors M1 and M2 have good matching of their properties, such as channel length, width, threshold voltage etc., the relationship IOUT = f (VGS,VDG=0) applies, thus setting IOUT = IREF; that is, the output current is the same as the reference current when VDG=0 for the output transistor, and both transistors are matched.The drain-to-source voltage can be expressed as VDS=VDG +VGS. With this substitution, the Shichman-Hodges model provides an approximate form for function f (VGS,VDG):[2].

$$I_d = f(V_{GS}, V_{DG})$$

$$= \frac{1}{2}K_p\left(\frac{W}{L}\right)(V_{GS} - V_{th})^2(1 + \lambda V_{DS})$$

$$= \frac{1}{2}K_p\left[\frac{W}{L}\right](V_{GS} - V_{th})^2[1 + \lambda(V_{DG} + V_{GS})]$$

where, K_p is a technology related constant associated with the transistor, W/L is the width to length ratio of the transistor, VGS is the gate-source voltage, Vth is the threshold voltage, λ is the channel length modulation constant, and VDS is the drain source voltage.

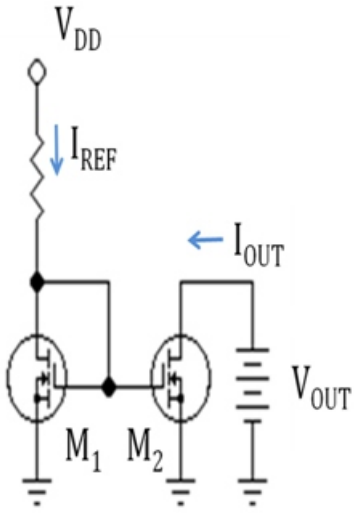

Figure 1 MOSFET Current Mirror

Mirror characteristics:

There are three main specifications that characterize a current mirror. The first is the transfer ratio (in the case of a current amplifier) or the output current magnitude (in the case of a constant current source CCS). The second is its AC output resistance, which determines how much the output current varies with the voltage applied to the mirror. The third specification is the minimum voltage drop across the output part of the mirror necessary to make it work properly. This minimum voltage is dictated by the need to keep the output transistor of the mirror in active mode. The range of voltages where the mirror works is called the compliance range and the voltage marking the boundary between good and bad behavior is called the compliance voltage. There are also a number of secondary performance issues with mirrors, for example, temperature stability.

Current Mirrors and Biasing Networks:

One of the most important parts of an analog design is the biasing circuitry. The purpose of the bias circuitry is establish an appropriate DC operating point for the transistor. With the correct DC operating point established a stable and predictable DC drain current ID and a DC drain-source voltage ensures operation in the saturation region for all input signals that may be encountered. This component forms the basis for an operational amplifier whereby various circuits like the differential pair, gain stage and output stage rely on its °flawless stable operation.

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For the Operational Amplifier design five different types of current mirrors were examined; Basic Current Mirror, Cascade/Cascode Current Mirror, Wilson Current Mirror, Modified Wilson Current Mirror and Reduced Cascade/Cascode Current Mirror. The advantages and disadvantages of each type of current mirror will be outlined later.

The five current mirrors which were examined were designed in Cadence and were placed into a standard test circuit consisting of a basic differential pair with active load and basic common-source amplifier output stage with a 10K load. These current mirrors were then subjected to several tests including; DC Sweep, current mirror output impedance and stability of current supplied across dynamic voltage range.

The ability of a current mirror to hold current constant, the number of transistors used and their sizes are the general defining factors on whether a current mirror is "Good" or not. These factors were considered when deciding on the current mirror to be used in the Op-Amp DesignIdeal Characteristics of a Current Mirror

- Output current linearly related to the input current. I_out= A ¢ I_in
- Input Resistance is zero.
- Output resistance is infinity.

Basic Current Mirror Derivation
Below is the derivation of the simple current mirror.

Q_1 Is operating in the saturation region since its drain is shorted to its gate.

Thus,

$$I_{D_1} = \frac{1}{2} K_{n^1} \left(\frac{W}{L}\right)_1 (V_{GS} - V_t)^2$$

Note we neglect channel-length modulation and assume $\lambda = 0$.

The drain current of Q_1 is supplied by V_{DD} through a resistor, R. Assuming gate currents to be approximately 0.

$$I_{D_1} = I_{ref} = \frac{V_{GS} - V_t}{R}$$

IMPLEMENTATION:
Proposed comparator:

Our proposed Comparator circuit is implemented in 45nm CMOS technology, with a supply voltage of 0.7V due to which the circuit exhibits low leakage, less average power dissipation, than other works. The schematic of high speed and a leakage tolerant CMOS comparator based on Footed Domino Logic comparator shown in figure 2.This proposed comparator indicates the full match or mismatch of the two binary inputs A and B of 4, 8, 16, 32 or 64 bits applied to the circuit. Basically, this circuit operates on two modes, one is pre-charge mode and another is evaluation mode.

In pre-charge phase, the clock is low, which makes transistor T1 ON and T2 OFF, then the pre-charge node is pre-charge to high and the output goes low and T2 turns ON. This PMOS transistor T2 keep providing the supply to the pull down network, hence it is known as Keeper Transistor, and Transistor T1 is known as Pre-charge transistor.

During the evaluation mode, when the clock is high, if the corresponding bits of A and B inputs are same than there is no conduction path from pre-charge node to ground, hence the output remains low. But, if any position of input A and B are differ than there will exists a conduction path from pre-charge node to ground, which causes the discharging of that node and hence the output goes high.

So, when the output become high, then the keeper transistor T2 turns OFF, this makes the output high. To provide stacking effect for leakage reduction in evaluation phase transistor T7 is added, but due to this there is an increase in delay, so for reducing the delay in evaluation phase, a current mirror (T8) is added in parallel with evaluation network.

The T9 transistor is used to provide feedback from the output to dynamic node, to avoid short circuit current on static inverter. This additional circuit in proposed comparator work in such a way that, in pre-charge phase, the pre-charge node is high, then the footer transistor T6 is OFF, therefore the current mirror (T8) is also OFF, and then there is no path for the discharging of pre-charge node.

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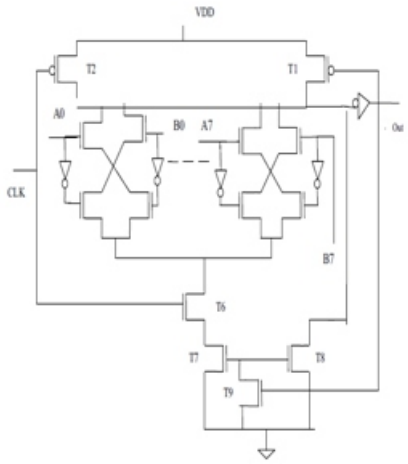

Figure 2: Proposed Comparator with current mirror

In case of evaluation phase, if all inputs are same then stacking effect offered by transistor T7 reduces the leakage of evaluation network [13] [14]. However, when the one of input bit is differ, T8 mirror transistor pulls large current from precharge node, since the output goes to high T9 transistor gets ON to discharge the precharge node completely. So T7 and T8 transistor makes the circuit faster in evaluation phase.

RESULTS

Timing Analysis

Conventional Comparator :

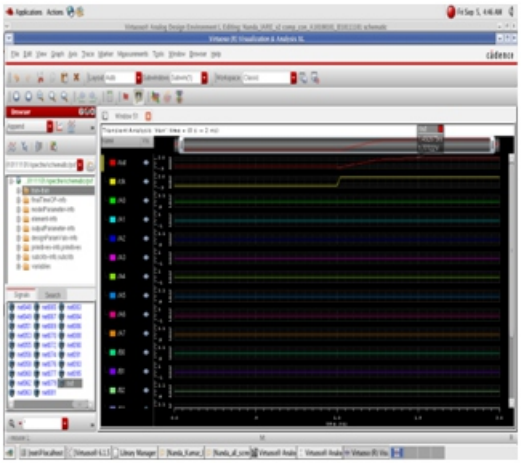

Figure 3 Shows the inputs and outputs with clock of conventional comparator when mismatch occurs.

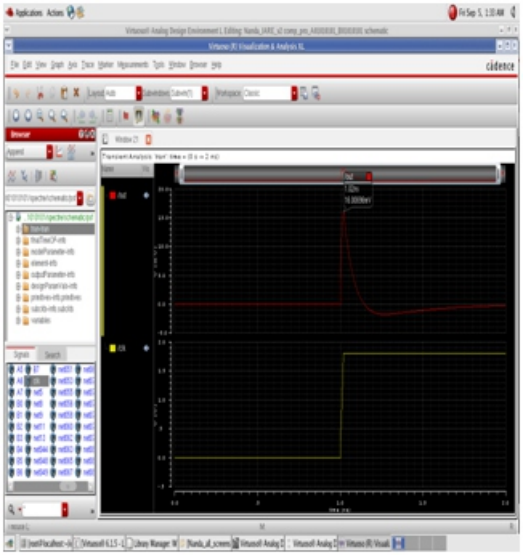

Figure 4 Shows the output of conventional comparator when the inputs match

POWER ANALYSIS

Conventional Comparator

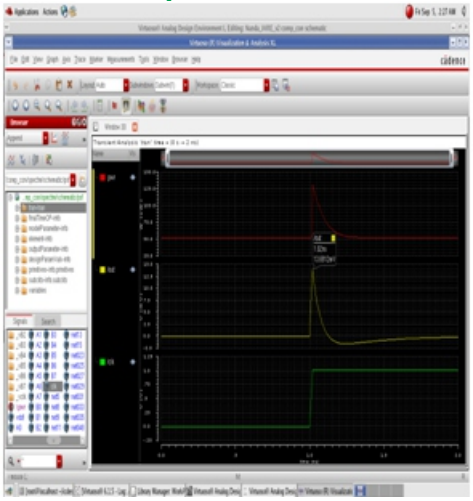

Figure 5 shows the voltage drop for matched inputs on conventional comparator.

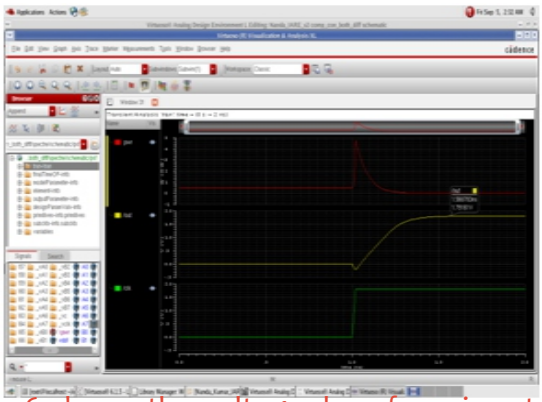

Figure 6 shows the voltage drop for mismatched inputs on conventional comparator

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Figure 7 shows the voltage drop for mismatched inputs on proposed comparator.

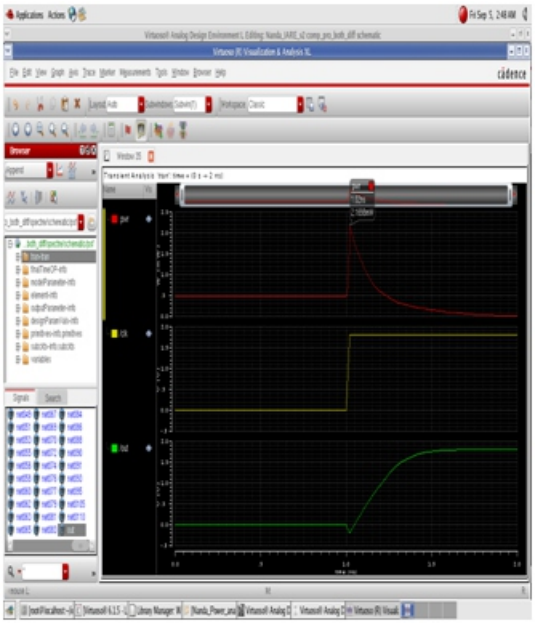

Figure 8 shows the power values of Proposed Comparator with mismatched inputs.

4.3 LEAKAGE ANALYSIS

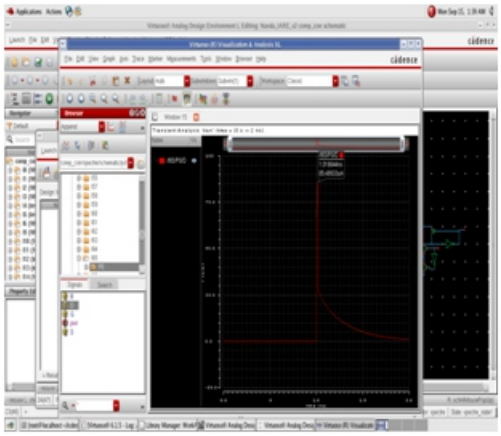

Figure 9 shows the leakage values of conv. Comparator with matched inputs.

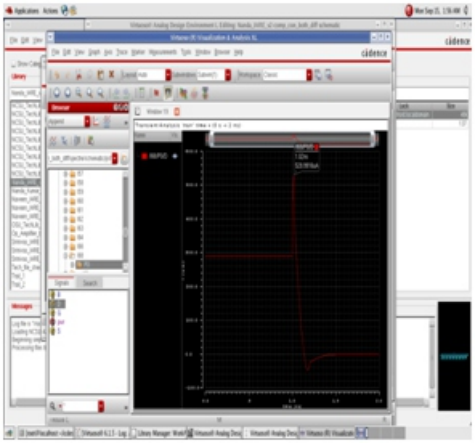

Figure 10 shows the leakage values of conv. Comparator with mismatched inputs.

	FDLC CIRCUIT			PROPOSED Comparator		
8-bit	Leakage current (uw)	Average power (uw)	Output Voltage (mv)	Leakage current (uw)	Average power (uw)	Output Voltage (mv)
Matched inputs	85.46933	129.57	13.6912	62.9105	71.07	12.063
Mismatched inputs	944.163	477.265	1791.6	505.2591	216.96	1792.0

Table 1. Simulation Results of FDLC Circuit And Proposed Comparator Circuit

CONCLUSION:

Power and speed being a limiting factor for high performance and high density integrated chips, without affecting the performance of the circuit, a great effort has been put to explore low leakage power and high speed.

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Domino CMOS logic dissipates very low standby power compare to static CMOS logic, in our proposed circuit we use footed domino logic comparator circuit and proposed comparator in terms of leakage power and Average power for high fan in 8-bits. It has been found from the simulation result that the leakage power and Average power of the proposed comparator reduces as compare to Footed Domino Logic Comparator circuit. These comparisons of the comparator design are based upon 45nm CMOS technology in Cadence tool.

FUTURE SCOPE:

The design system open new research problems such as

- We can Reduce the size of the chip.
- We can Reduce the leakage of the comparator.
- We can Reduce delay and increase the speed of the comparator.

In Future by adopting other methods we can resolve above problems.

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