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Fuzzy Based DSTATCOM for Power Quality Improvement in Distribution System

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Abstract:

This paper deals with the improvement of dc link capacitor voltage during transient conditions using fuzzy based logic and power quality improvement using DSTATCOM. In general Dc link capacitor is regulated using a PI controller when various control algorithms are used for load compensation. In this work, a fuzzy logic based supervisory method is implemented to improve transient performance of DSTATCOM. The fuzzy logic based supervisor varies the proportional and integral gains of the PI controller during the transient period immediately after a load change. In fuzzy a considerable reduction in the %THD of the source current compared to a normal PI controller is obtained. The performance of the FUZZY strategy is proved using detailed simulation studies.

Index Terms:
DSTATCOM, DC-link, Fuzzy, load compensation, PI controller.

I. INTRODUCTION:

Now a day's the usage of power converters and other nonlinear loads in industry and by consumers have increased extensively. This increases the sensitiveness of the loads and deterioration of power system (PS) voltage and current waveforms (such as magnitude, phase and harmonics). The presence of harmonics in the power lines results in greater power losses in distribution, interference problems in communication systems, in operation failures of electronics equipments, which are more and more sensitive. To cope with these difficulties, extensive research work is going on to improve power quality (PQ) for mitigating the harmonics. However, most of the methods use PI controller to improve transient state of the error signal.

In this area some more controllers are also FUZZY such as, RST Controller and Fuzzy Logic. In this paper we discuss about The Distribution Static Compensator or the D-STATCOM is a shunt connected custom power device [2] which injects current at the point of common coupling (PCC) used to control the terminal voltage and improve the power factor. Various control algorithms have been FUZZY in literature [3]-[5] to extract the reference currents of the compensator. The theory of instantaneous symmetrical components [6] has been used because of its simplicity in formulation and ease of calculation. The source voltages are assumed to be balanced sinusoids and stiff. In a D-STATCOM, generally, the DC capacitor voltage is regulated using a PI controller when various control algorithms areused for load compensation. However, during load changes, there is considerable variation in DC capacitor voltage which might affect compensation.

In this work, a fuzzy logic based supervisory method is FUZZY to improve transient performance of the DC link. The fuzzy logic based supervisor varies the proportional and integral gains of the PI controller during the transient period immediately after a load change. An improvement in the performance of the controller is obtained because of appropriate variation of PI gains using expert knowledge of system behavior and higher sampling during the transient period. The voltage waveform also has a faster settling time. The efficiency of the FUZZY strategy is proved using detailed MATLAB simulation studies.The DSTATCOM improves the voltage sags, swell conditions and the ac output voltage at the customer points, thus improving the PQ at the distribution side. In this the voltage controller technique (also called as decouple technique) is used as the control technique for DSTATCOM. This control strategy uses the dq0 rotating reference frame, because it offers higher accuracy than stationary frame-based techniques.

In this Vabc are the three-phase terminal voltages, Iabc are the three-phase currents injected by the DSTATCOM into the network, Vrms is the rms terminal voltage, Vdc is the dc voltage measured in the capacitor, and the superscripts indicate reference values. Such a controller employs a phase-locked loop (PLL) to synchronize the three phase voltages at the converter output with the zero crossings of the fundamental component of the phase-A terminal voltage. The block diagram of a FUZZY control technique is shown in Figure 2. Therefore, the PLL provides the angle f to the abc-to-dq0 (and dq0-to-abc) transformation. There are also four proportional integral (PI) regulators. The first one is responsible for controlling the terminal voltage through the reactive power exchange with the ac network.

This PI regulator provides the reactive current reference Iq*, which is limited between +1pu capacitive and -1pu inductive. Another PI regulator is responsible for keeping the dc voltage constant through a small active power exchange with the ac network, compensating the active power losses in the transformer and inverter. This PI regulator provides the active current reference Id*. The other two PI regulators determine voltage reference Vd *, and Vq*, which are sent to the PWM signal generator of the converter, after a dq0-to-abc transformation. Finally, Vab* are the three-phase voltages desired at the converter output.

2. DSTATCOM TOPOLOGY IN DISTRIBUTION SYSTEM:

DSTATCOM topology in distribution power sys-tem is shown in Fig. 1. It consists of interfacing inductance (Lf), resistance (Rf), and two equal dc link capacitor (Cdc1, Cdc2) and VSI. The three-phase distribution system is connected to non-linear diode rectifier load or controlled bridge rectifier load and unbalanced RL-load. The source neutral point (N) is connected to load common point (n), in order to provide path for unbalanced current. In Fig. 1, the source connected to the load and DSTATCOM is connected in shunt with the load to mitigate current harmonics and load reactive power compensation. Here vsa,vsb,vscare the source voltages, isa, isb,iscare currents drawn from source, ila,ilb,ilc are load currents and ifa,ifb,ifc are filter currents injected by DSTATCOM at the Point of Common Coupling (PCC). The capacitance values of two dc-link capacitors are equal.

These two dc-link capacitors are charged to equal value through an anti-parallel diodes of IGBT switches without applying gate signals. Designing of DSTATCOM parameters like dc link voltage, interfacing inductor and dc link capacitor are required for proper tracking of reference filter currents. The design process of DSTATCOM is explained in section-III.

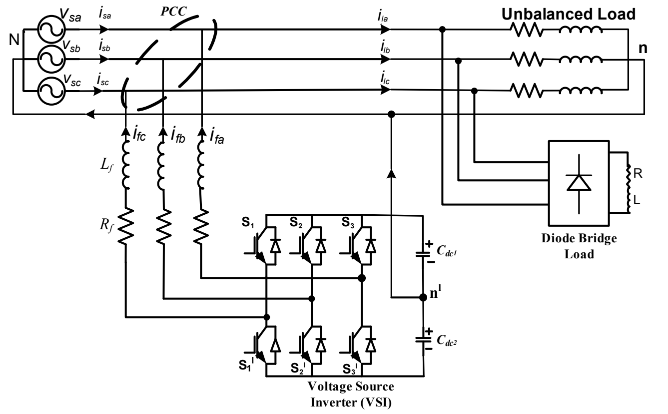

Fig. 1. Topology of DSTATCOM in three-phase four-wire distribution system

DESIGN OF DSTATCOM PARAMETERS :

Design of DSTATCOM parameters: dc-link voltage, dc-link capacitor, interfacing inductor is discussed below.

A.DC-link voltage:

In literature, dc-link voltage is maintained constant to reference dc voltage with voltage regulation loop. Here reference dc voltage is taken as 2 times of peak of the phase voltage of source. i.e.

$$V_{dc} = \frac{2\sqrt{2}V_{LL}}{\sqrt{3}m}, \quad (1)$$

where, V_{dc} = dc-link voltage, $V_{LL}$is line-line voltage, m is modulation index and is consider as 1.

B.DC-link capacitor:

In existing methods, dc link capacitor value is calculated from the equation given below.

$$C_{dc} = \frac{2pST}{(1.8V_m)^2 - (1.2V_m)^2} \quad (3)$$

Where, C_{dc} is dc link capacitor, S is kVA required by load, p is number of cycles required to control the dc voltage and T is system period. The design of dc

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capacitor value with this method gives better compensation but, the dc link capacitor value is high, leads to slow transient response.

C.Interfacing Inductor:

The value of the interfacing inductance is selected on the basis of proper shaping of compensating current. With higher value of inductance, compensating current will not follow the reference currents, with the lower value of inductance there are large ripple in the compensating current. In designing

$$L_f = \frac{mV_{dc}}{4hf_{swmax}}, \quad (4)$$

where, m is modulation index, h is hysteresis band width and f_{swmax} is maximum switching frequency.

of interface inductance, hysteresis band width and maximum switching frequency of compensator plays an important role. The maximum switching frequency occurs when the instantaneous supply voltage is around its peak value. The value of interface inductance (Lf) is obtained from

$$L_f = \frac{mV_{dc}}{4hf_{swmax}}, \quad (4)$$

where, m is modulation index, h is hysteresis band width and f_{swmax} is maximum switching frequency.

D.Hysteresis band:

Hysteresis controller is a non-linear current controller [18]. The hysteresis control scheme is based on non-linear feedback loop with two level hysteresis comparators. When error exceeds given tolerance band (h), switching pulses are produced. In this paper, variable switching frequency hysteresis current controller is used. The controlling of switching frequency results in complex control of voltage source inverte. The main advantages of hysteresis current controller are simplicity, outstanding robustness, no tracking errors.

2.1.PROBLEM OF DC LINK PI CONTROL:

At steady state, the average power is updated at every half cycle during this time period, the power to the load is supplied temporarily from the DSTATCOM. This leads to a decrease in dc link voltage, if load is increased or an increase in capacitor voltage, if the load is reduced. For good compensation, it is important that the capacitor voltage remains as close to the reference value as possible.

After a load change has occurred, depending on the values of Kp and Ki the capacitor voltage takes 6-8 cycles to settle. However during transient operation, it is possible to improve the performance of the dc link by varying the gains of the PI controller using a set of heuristic rules based on expert knowledge. Also, improvements in technology such as faster Digital Signal Processing allow us to increase the sampling rate for better feedback as to how the system responds to changes. For nonlinear systems, fuzzy based control has been proved to work well .Fuzzy logic based supervision of the dc link PI controller gains improves the transient and settling performance of the dc link voltage control. Hence, the use of fuzzy logic for this application is justified.

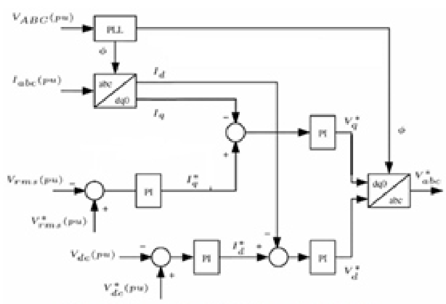

Figure 2: Proposed control technique of DSTATCOM

2.2.DC LINK PI CONTROL AND FUZZY CONTROL

The source voltages are assumed to be balanced sinusoids and stiff. The reference currents based on this theory are given in (1) below.

$$i^*_{fa} = i_{la} - i_{sa} = i_{la} - \frac{V_{sa} - \gamma(V_{sb} - V_{sc})}{\Delta}(P_{lavg} + P_{loss})$$

$$i^*_{fb} = i_{lb} - i_{sb} = i_{lb} - \frac{V_{sb} - \gamma(V_{sc} - V_{sa})}{\Delta}(P_{lavg} + P_{loss})$$

$$i^*_{fc} = i_{lc} - i_{sc} = i_{lc} - \frac{V_{sc} + \gamma(V_{sa} - V_{sb})}{\Delta}(P_{lavg} + P_{loss})$$

where $\Delta = \sum_{j=a,b,c} V_{sj}^2$ and $\gamma = \tan\varphi / \sqrt{3}$

For obtaining unity power factor at the source, φ = 0 and thus γ = 0. The term Plavg is the average value of load power which would be a constant value if there is no load change. This is computed using a moving average filter for half cycle. Ploss is the amount of power that is required to be drawn from the source to compensate for the losses which occur in the inverter. If this term is not included, then these losses will be supplied by the dc capacitor and dc link voltage will fall. It is however extremely difficult to compute the exact losses that occur in the inverter. Thus, Ploss is obtained using a PI controller. At steady state, the Ploss value is updated every half cycle. The sum of Ploss and Plavg terms determines the amount of power drawn from the source.

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The moving average filter used to calculate Plavg takes half a cycle to settle to the new value of average power. During this time, the power to the load is supplied temporarily from the DSTATCOM. This leads to a decrease in dc link voltage if the load is increased or an increase in capacitor voltage if the load is reduced. For good compensation, it is important that the capacitor voltage remains as close to the reference value as possible.After a load change has occurred, depending on the values of Kp and Ki, the capacitor voltage takes 6-8 cycles to settle. Most of the times, the gains are chosen by trial and error. A method to obtain good Kp and Ki values for the DSTATCOM application is given in [7]. This has been used as the base values during steady operation. However, during transient operation, it is possible to improve the performance of the dc link by varying the gains of the PI controller using a set of heuristic rules based on expert knowledge.

Also, improvements in technology such as faster DSPs allow us to increase the sampling rate for better feedback as to how the system responds to changes. For nonlinear systems, like the DSTATCOM, fuzzy based control has been proved to work well [8]. In this paper, it has been shown that fuzzy logic based supervision of the dc link PI controller gains improves the transient and settling performance of dc link voltage control. Hence, the use of fuzzy logic for this application is justified. This paper has been organized in the following manner. First an explanation of the VSI topology for the DSTATCOM used is given and then the state space modelling used to simulate the working of the DSTATCOM is explained. The design of the fuzzy supervisor for this system is elucidated. The methodology and results of the simulation are shown in the final section, proving improved dc link performance. During load changes, there is some active power exchange between the DSTATCOM and the load.

The input to the PI controller is the error in the dc link voltage and the output is the value of Ploss. The value of Ploss depends on the value of Kp, Ki and the error in dc link voltage. Thus, it is important to tune Kp and Ki properly. Because of the inherent non-linearity and complexity of the system, it is difficult to tune the gains of the controller. It is usually done by trial and error. The base values of Kp and Ki have been designed using the energy concept proposed in [7]. Also, it has been shown in literature that fuzzy supervision can improve the performance of PID controllers in nonlinear systems [10]-[12].However, these mostly deal with set-point changes in control applications.

The derivative control term is not used because improvement in stability may or may not be obtained when used only with proportional control and if it is used with integral control as well, tuning for good performance is difficult [13]. The design of a fuzzy system is highly system specific and requires in-depth knowledge of the system and the various parameters that can be controlled for good performance. The design of a fuzzy supervisor for dc link PI control in a DSTATCOM is given in the next section.

2.3 DESIGN OF THE FUZZY LOGIC SUPERVISOR FOR PI CONTROLLER:

PID controllers are extensively used in industry for a wide range of control processes and provide satisfactory performance once tuned when the process parameters are well known and there is not much variation. However, if operating conditions vary; further tuning may be necessary for good performance. Since many processes are complicated and nonlinear, fuzzy control seems to be a good choice. Literature shows many approaches where the PI controller has been replaced by a fuzzy controller [14]-[15]. However, instead of completely modifying the control action, it is sufficient to use an additional level of control by supervising the gains using fuzzy techniques to improve the performance of the system [16].A PI controller is preferred to regulate the dc link voltage as the presence of the integral term ensures zero steady state error. The dc link capacitor voltage waveform contains a ripple because according to the instantaneous symmetrical component theory, which is used in this work, the compensator supplies the oscillating part of the active power also.

Thus there is always a zero average oscillating power exchange between the compensator and the load. This ripple can be seen in the simulation results in Fig. 9. The fuzzy controller scaling has been designed to give a good output irrespective of the presence of the ripple during the transient period. Some of the main aspects of fuzzy controller design are choosing the right inputs and outputs and designing each of the four components of the fuzzy logic controller shown in Fig. 2. 2 Each of these will be discussed in the subsections below: Also, the fuzzy controller is activated only during the transient period and once the value of the dc link voltage settles down, the controller gains are kept constant at the steady state value. A detailed description of the design of a fuzzy logic controller has been given in [17].

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2.4 INPUTS AND OUTPUTS:

The inputs of the fuzzy supervisor have been chosen as the error in dc link voltage and the change in error in dc link voltage.

$$\mathrm{err}(i) = V^{ref} - V(i) \qquad (3)$$
$$\mathrm{derr}(i) = \mathrm{err}(i) - \mathrm{err}(i-1) \qquad (4)$$

In (3) and (4) above, e (i) is the error and (i) is the change in error in the ith iteration. is the reference dc link voltage and Vdc (i) is the dc link voltage in the ith iteration. The outputs of the fuzzy supervisor are chosen as the change in Kp value and the change in Ki value.

KP = Kpref+ΔKp, Ki = Kiref+ΔKi

Kpref andKiref are the steady state values determined by the method specified in [7] and ΔKp and ΔKiare the outputs of the fuzzy logic supervisor.

2.5 FUZZIFICATION:

The fuzzification interface modifies the inputs to a form in which they can be used by the inference mechanism. It takes in the crisp input signals and assigns a membership value to the membership function under whose range the input signal falls. Typical input membership functions are triangular trapezoidal or exponential. Seven triangular membership functions have been chosen: NL (Negative Large), NM (Negative Medium), NS (Negative Small), Z (Zero), PS (Positive Small), PM (Positive Medium) and PL (Positive Large) for both error (err) and change in error (derr) . The input membership functions are shown in Fig-4. The tuning of the input membership function is done based on the requirement of the process. Each membership function has a membership value belonging to [0 1]. It can be observed that for any value of error or change in error, either one or two membership functions will be active for each.

2.6 INFERENCE MECHANISM:

The two main functions of the inference mechanism are:
a) Based on the active membership functions in error and the change in error inputs, the rules which apply for the current situation are determined.
b) Once the rules which are on are determined, the certainty of the control action is ascertained from the membership values.

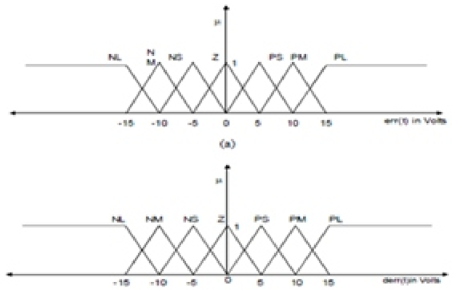

Figure.2.1 Membership functions for error input and (b) Membership functions for change in error input

This is known as premise quantification. Thus at the end of this process, we shall have a set of rules each with a certain certainty of being valid. The database containing these rules is present in the rule base from which the control action is obtained. The rule base will be discussed in the next section. An example of a rule is given in (7). The terms PL and PM are the membership functions for error and for change in error respectively. IF "error" is PL (positive large) "change in error" is PM (positive medium) THEN "ΔKp"is L (Large Kp) "ΔKi" is SKi (Small Ki) The minimum operation is used to determine the certainty called μ premise of the rule formed by their combination.

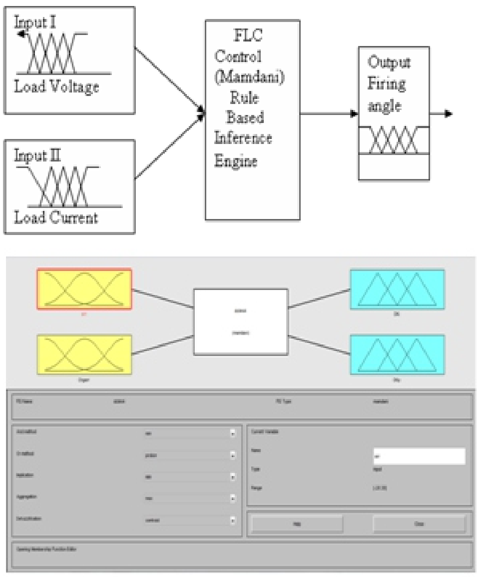

Figure.2.2 MATLAB Fuzzy logic controller design

	Load voltage					
Load current		NL	NM	P	PM	PB
	NL	PB	PB	NM	NM	NL
	NM	PB	PB	NM	P	NL
	P	P	PM	NM	NM	P
	PM	NM	P	NM	NM	PM
	PB	NL	NM	NM	NL	NL

Figure.2.3 FUZZY Rules

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SIMULATION STUDIES

The control scheme is implemented using MATLAB simulation software. Simulation parameters are given in Table I.

TABLE I

Sl.n	System Parameter	Simulation values
1	System voltage	400 V rms
2	Frequency	50 Hz
3	Non-linear load	50 Ω, 20 mH
4	Linear load (R & L)	30+j62.8 Ω 40+j78.5 Ω 50+j50.24 Ω
5	Interfacing inductor (L_f)	22 mH
6	dc-link voltage (V_{dc})	650 V
7	dc-link capacitor (C_{dc})	2600 µF

Terminal voltages and source currents before compensation are shown in Fig. 4 and Fig. 5 respectively. It is observed, due to distorted and unbalanced source currents flowing through the feeder make terminal voltages unbalanced and distorted. Two conditions, namely, nominal operation and operation during sag are compared between the traditional and proposed method.

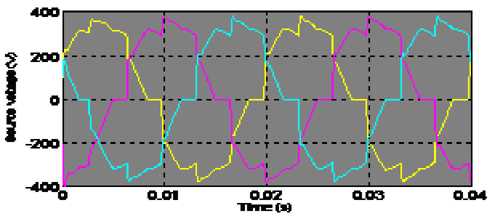

Fig. 4 Three phase source voltages before compensation.

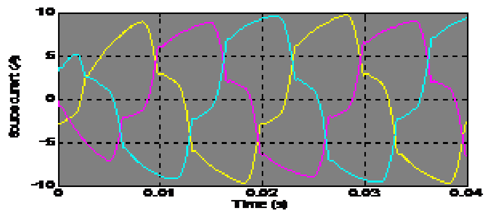

Fig. 5 Three phase source currents before compensation

A. Nominal Operation of DSTATCOM:

Initially, the traditional method is considered. Fig. 6(a)–(c) shows the regulated terminal voltages and corresponding source currents in phase a, b and c, respectively. These waveforms are balanced and sinusoidal. However, source currents lead respective terminal voltage switch show that the compensator supplies reactive current to the source to overcome feeder drop, in addition to supplying load reactive and harmonic currents.

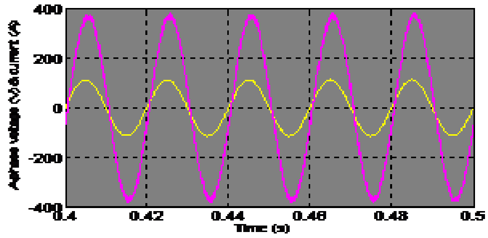

Fig. 6-(a) A-phase source voltage and current with traditional method.

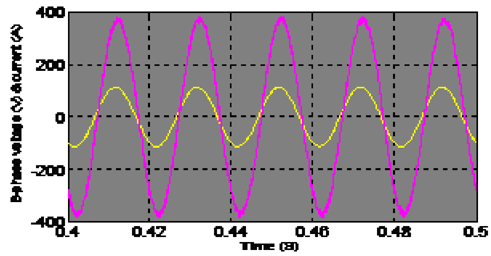

Fig. 6-(b) B-phase source voltage and current with traditional method

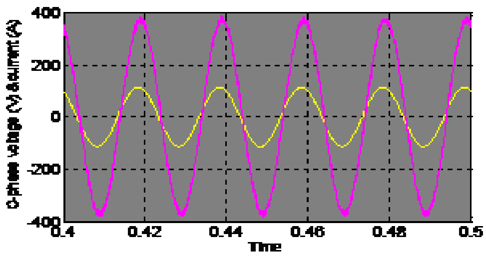

Fig. 6-(c) C-phase source voltage and current with traditional method.

The dc bus traditional load voltage, Fuzzy load voltage and load angle dynamics are shown in Fig. 7(a), 7(b) and 7(c) respectively. Fig. 7(a) shows the dc bus voltage regulated at a nominal voltage of 1300V. Fig.7(b) shows the discharging dc link voltage where sag was occurred, 7(c) shows the load angle settled around 8.50¬.

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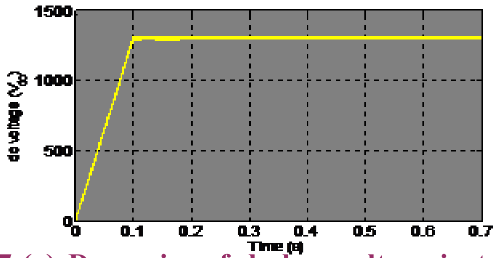

Fig. 7-(a) Dynamics of dc bus voltage in traditional method

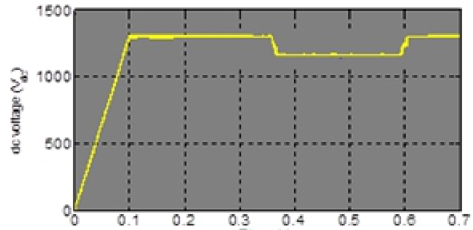

Fig. 7-(b) Dynamics of dc bus voltage in traditional method

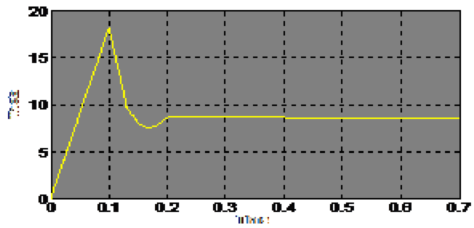

Fig. 7-(c) Dynamics of load angle in traditional method

Using the proposed method, terminal voltages and source currents are in phase and are shown in Fig. 8(a)–(c), respectively. It can be seen that the respective terminal voltages and source currents are in phase with each other, in addition to being balanced and sinusoidal. Therefore, Unity Power Factor (UPF) is achieved at the load terminal.

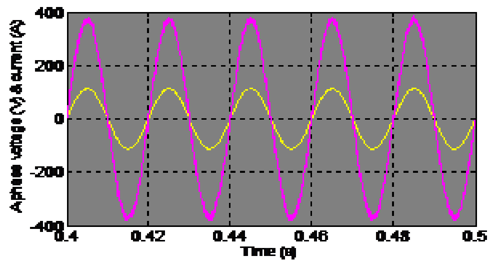

Fig.8-(a) A-phase source voltage and current with proposed method.

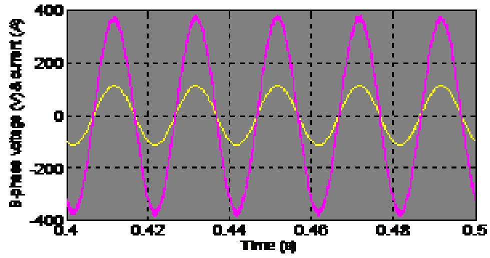

Fig.8-(b) B-phase source voltage and current with proposed method.

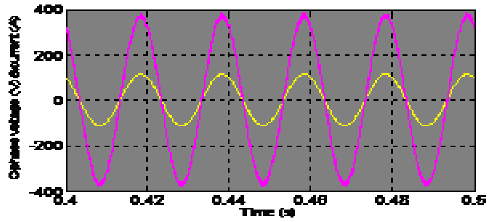

Fig.8-(c) C-phase source voltage and current with proposed method.

For the considered system, waveforms of load reactive power (Qload), compensator reactive power (Qvsi), and reactive power at the PCC (Qpcc) in the traditional and proposed methods are shown in Fig. 9(a) and (b), respectively. In the traditional method, the compensator needs to overcome voltage drop across the feeder by supplying reactive power into the source. As shown in Fig. 9(a), reactive power that is supplied by the compensator is significantly more than the load reactive power demand. This additional reactive power goes into the source. This confirms that significant reactive current flows along the feeder in the traditional method. However, in the proposed method, UPF is achieved at the PCC by maintaining suitable voltage magnitude. Thus, the reactive power supplied by the compensator is the same as that of the load reactive power demand. Consequently, reactive power exchanged by the source at the PCC is zero. These waveforms are shown in Fig. 9(b).

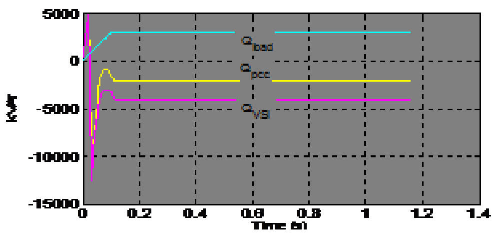

Fig. 9-(a) Reactive powers in traditional method.

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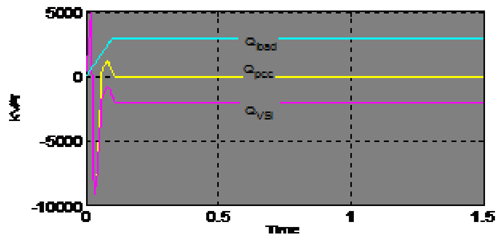

Fig. 9-(b) Reactive powers in proposed method.

Fig. 10(a) and (b) shows the source rms currents in phase for the traditional and proposed methods, respectively. The source current has decreased from 12 to 10.5 A in the proposed method.

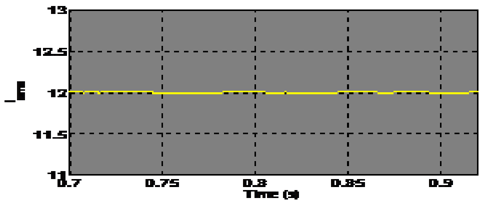

Fig. 10-(a) Rms source current with traditional method.

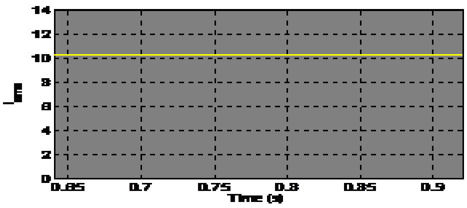

Fig. 10-(b) Rms source current with proposed method.

B. Operation during Sag:

To create sag, source voltage is lowered by 20% from its nominal value at t= 0.6 s as shown in Fig. 11(a). Since voltage regulation capability does not depend upon reference voltage, it is not shown separately for the traditional method.

Fig. 11(b) shows the load voltage from normal to sag regulated at their reference value. The controller provides a fast voltage regulation at the load terminal.

During sag to normal the source voltage and load voltage are shown in Fig. 12(a) and (b) respectively.

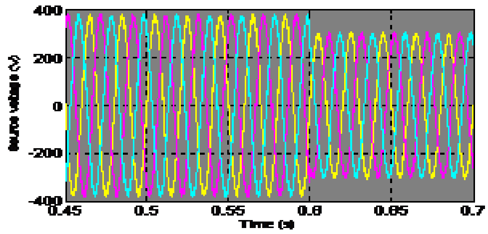

Fig. 11-(a) Sag at t = 0.6 in source voltage.

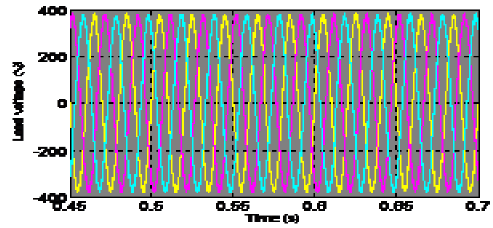

Fig. 11-(a) Load voltage during normal to sag.

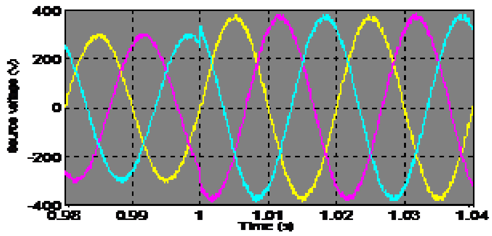

Fig. 12-(a) Source voltage during sag to normal voltage.

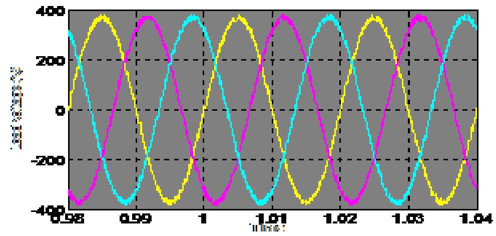

Fig. 12-(b) Load voltage during sag to normal.

The harmonic spectrum of the A-phase source current without compensator and with compensator in conventional and fuzzy is shown in below Figs.13-16. The %THD of source current within the limits (%5).

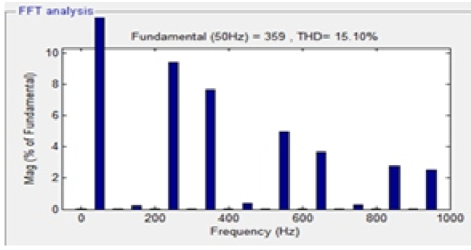

Fig.13Harmonic spectrum of A-phase current without compensation.

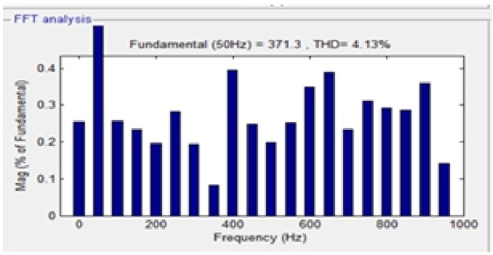

Fig.14 Harmonic spectrum of A-phase current with conventional method.

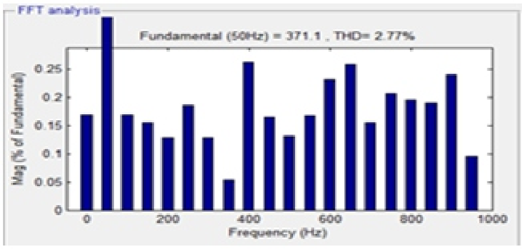

Fig.15 Harmonic spectrum of A-phase current with proposed method.

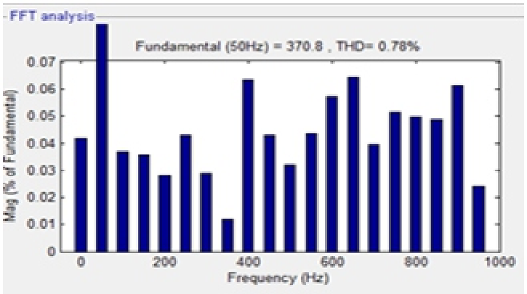

Fig.16Harmonic spectrum of A-phase current with fuzzy method.

CONCLUSION:

A fuzzy logic supervisory control to the DC link PI controller in a D-STATCOM has been proposed. The supervisor varies the gain of the PI controller during the transient period in a way that improves performance. The system has been modeled and simulated in the MATLAB technical environment with a case study.

Instantaneous symmetrical component theory has been used for load compensation. Good compensation has been observed as source current %THD is reduced to 0.78% from 15.10%. Thus, through simulation studies, the implementation of a fuzzy supervisor for DC link voltage control in a DSTATCOM using instantaneous symmetrical component theory for load compensation has been demonstrated.

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