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Design and Implementation of High Performance 64 bit MAC Unit

Anjaiah
M.Tech VLSI IInd year,
LORDS Institute of Engg & Technology,
Hyderabad, India.

R.Surender Reddy
Assistant Professor,
LORDS Institute of Engg & Technology,
Hyderabad, India.

Abstract:

Design of high performance 64 bit Multiplier-and-Accumulator (MAC) is implemented in this paper. MAC unit performs important operation in many of the digital signal processing (DSP) applications. The multiplier is designed using modified Wallace multiplier and the adder is done with carry save adder. The total design is coded with Verilog-HDL and the synthesis is done using Cadence RTL complier using typical libraries of TSMC O.18um technology. The total MAC unit operates at 217 MHz. The total power dissipation is 177.732 mW.

Keywords:
Modified Wallace multiplier, Carry save adder, multiplier and accumulator (MAC)

I. INTRODUCTION:

MAC unit is an inevitable component in many digital signal processing (DSP) applications involving multiplications and/or accumulations.MAC unit is used for high performance digital signal processing systems. The DSP applications include filtering, convolution, and inner products. Most of digital signal processing methods use nonlinear functions such as discrete cosine transform (DCT) or discrete wavelet transforms (DWT). Because they are basically accomplished by repetitive application of multiplication and addition, the speed of the multiplication and addition arithmetic determines the execution speed and performance of the entire calculation [1] Multiplication and accumulate operations are typical for digital filters. Therefore, the functionality of the MAC unit enables high-speed filtering and other processing typical for DSP applications. Since the MAC unit operates completely independent of the CPU, it can process data separately and thereby reduce CPU load. The application like optical communication systems which is based on DSP, require extremely fast processing of huge amount of digital data. The Fast Fourier Transform (FFT) also requires addition and multiplication. 64 bit can handle larger bits and have more memory.

A MAC unit consists of a multiplier and an accumulator containing the sum of the previous successive products. The MAC inputs are obtained from the memory location and given to the multiplier block. The design consists of 64 bit modified Wallace multiplier, 128 bit carry save adder and a register.

II. MAC OPERATION:

The Multiplier-Accumulator (MAC) operation is the key operation not only in DSP applications but also in multimedia information processing and various other applications. As mentioned above, MAC unit consist of multiplier, adder and register/accumulator. In this paper, we used 64 bit modified Wallace multiplier. The MAC inputs are obtained from the memory location and given to the multiplier block. This will be useful in 64 bit digital signal processor. The input which is being fed from the memory location is 64 bit. When the input is given to the multiplier it starts computing value for the given 64 bit input and hence the output will be 128 bits. The multiplier output is given as the input to carry save adder which performs addition. The function of the MAC unit is given by the following equation [4]:

$$F = IPjQj \quad \text{---------- (1)}$$

The output of carry save adder is 129 bit i.e. one bit is for the carry (128bits+ 1 bit). Then, the output is given to the accumulator register.

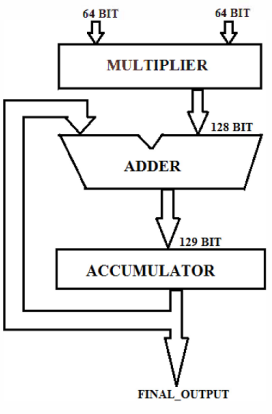

Figure 1[4]: Basic architecture of MAC unit

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The accumulator register used in this design is Parallel In Parallel Out (PIPO). Since the bits are huge and also carry save adder produces all the output values in parallel, PIPO register is used where the input bits are taken in parallel and output is taken in parallel. The output of the accumulator register is taken out or fedback as one of the input to the carry save adder. The figure 1 shows the basic architecture of MAC unit. Modern computers may contain a dedicated MAC, consisting of a multiplier implemented in combinational logic followed by an adder and an accumulator register that stores the result. The output of the register is fed back to one input of the adder, so that on each clock cycle, the output of the multiplier is added to the register.

III. TYPES OF MULTIPLIERS:

Multipliers are categorized relative to their applications, architecture and the way the partial products are produced and summed up. Based on all these, a designer might find following types of multipliers.

A)Array multipliers:

In array multipliers, the counters and compressors are connected in a serial fashion for all bit slices of the Partial Product parallelogram. As can be seen in Figure 2.1, the array topology is a two-dimensional structure that fits nicely on the VLSI planar process. There are several possible array topologies including simple, double and higher order arrays.

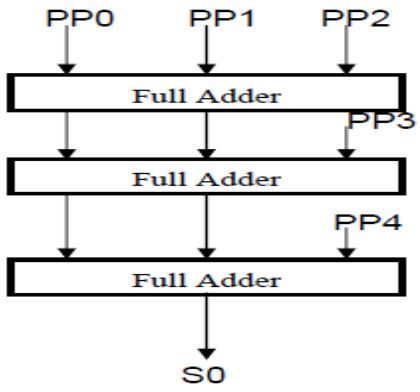

Figure 3.1 Array multiplier mechanisms

B) Simple array multiplier:

In this type of array, the output of each row of counters (3:2 compressors) is the input to the next row of counters.

In the simple array, each row of [3:2] compressors adds a partial product to the partial sum, generating a new partial sum and a sequence of carries. The delay of the array depends on the depth of the array. Therefore, the summing time for the simple array is N-2 [3:2] compressor delays, where N is the number of partial products. The drawback of this type of array is the hardware is underutilized. The counters are used only once in the calculation of the result, for the remaining time, they are idle. This drawback can be diminished by pipelining the array so that several multiplications can occur simultaneously. Pipelining would increase the throughput of the multiplier, but would also increase the latency and area of the multiplier. A fully pipelined array is normally avoided, since the array would be faster than the clock of processor. Figure 22 depicts the layout of a simple array topology. The dots represent the partial products.

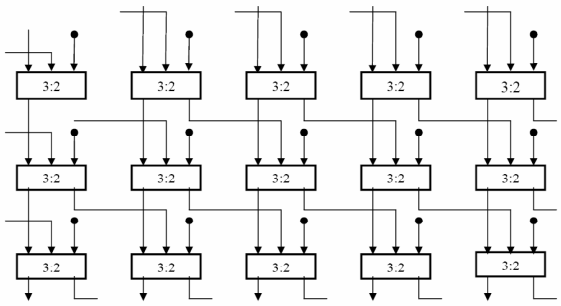

Figure3.2: Simple array layouts

C) Double array multiplier:

The double array design is faster than a simple array one. In this type of array, the delay required to produce the result for the simple array can be halved by adding partial products in two parallel rows. The odd-numbered PPs are added in one row while the other row adds the even-numbered PPs. When all the Partial products are accumulated, the two partial sums are combined using a [4:2] compressor.

The double array also consists of rows of [3:2] compressors. However, the output of the counter is the input to the row after the next one. The delay required to reduce the partial products is [N/2 -2] [3:2] compressors + 1 [4:2] compressorFigure shows clearly explains the basic idea of adding PPs using double array.

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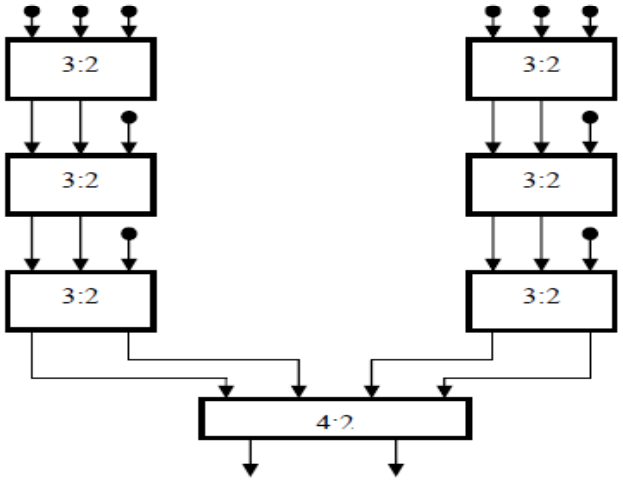

Figure3.3: Partial products addition using Double array

D) Binary Trees:

The [4:2] compressor designed by Shen and Weinberger in 1978, is the basis for binary tree multipliers. [4:2] compressor can be designed by connecting two [3:2] compressors in series. Although it can also be built in a smart and fast way by using 3 XORs in the critical path. This reduces the [4:2] compressor delay by approximately 25 %. Figure 26 shows a 2-dimensional view of a bit slice of the 16-bit binary tree. The [4:2] compressor reduces the PPs in logarithmic time, because of its 2-to-1 reduction ratio.

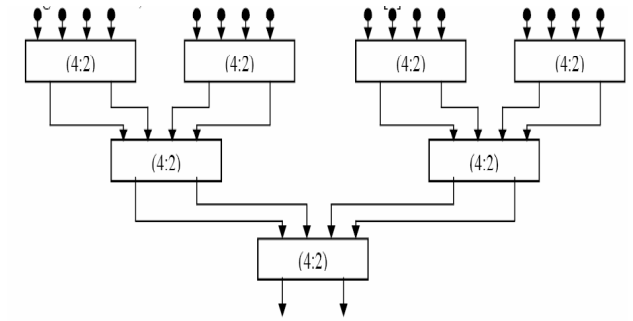

Figure 3.4 Binary tree formed by 4:2 compressors

IV. MODIFIED WALLACE MULTIPLIER:

A modified Wallace multiplier is an efficient hardware implementation of digital circuit multiplying two integers. Generally in conventional Wallace multipliers many full adders and half adders are used in their reduction phase. Half adders do not reduce the number of partial product bits.

Therefore, minimizing the number of half adders used in a multiplier reduction will reduce the complexity Hence, a modification to the Wallace reduction is done in which the delay is the same as for the conventional Wallace reduction. The modified reduction method greatly reduces the number of half adders with a very slight increase in the number of full adders. Reduced complexity Wall ace multiplier reduction consists of three stages [2]. First stage the N x N product matrix is formed and before the passing on to the second phase the product matrix is rearranged to take the shape of inverted pyramid. During the second phase the rearranged product matrix is grouped into non-overlapping group of three as shown in the figure, single bit and two bits in the group will be passed on to the next stage and three bits are given to a full adder. The number of rows in the in each stage of the reduction phase is calculated by the formula

$$r_{i+1} = 2[r_i/3] + r_i \bmod 3$$

$$\text{If } r_i \bmod 3 = 0, \text{ then } r_{i+1} = 2r_i/3$$

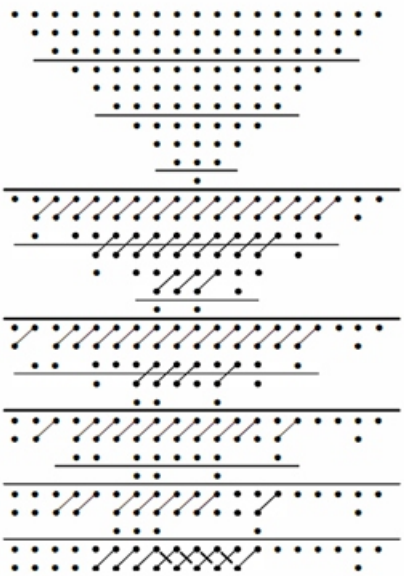

Figure 4.1: Modified Wallace multiplier

If the value calculated from the above equation for number of rows in each stage in the second phase and the number of row that are founded in each stage of the second phase does not match, only then the half adder will be used. The final product of the second stage will be in the height of two bits and passed on to the third stage. During the third stage the output of the second stage is given to the carry propagation adder to generate the final output.

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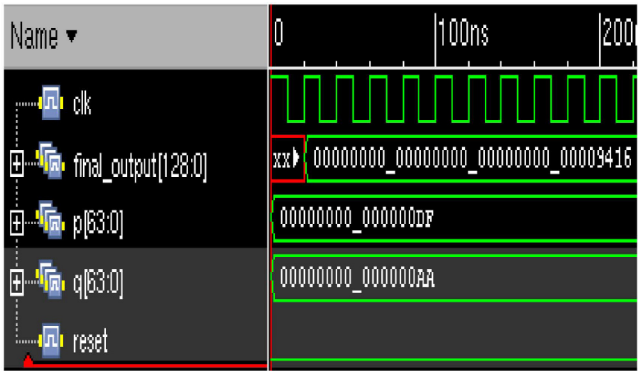
V. RESULT:

The design is developed using Verilog-HDL and synthesized in Encounter RTL compiler using typical libraries of TSMC 180nm technology. As a previous work, 8 bit MAC unit is designed using different multipliers and adders. The multipliers used for comparative study are: (i) Modified Booth Aigorithm (ii) Dadda Multiplier (iii) Wallace multiplier. The different adders used in the study are: (i) Carry Look Ahead (ii) Carry Select Adder (iii) Carry Save adder. The area, delay and power dissipation comparative table are shown in the Table:1 and Table:2 respectively. The graphs are plotted against the different type of 8 bit MAC unit.



Simulation Waveform of 64 bit MAC unit

Instance	Cells	Cell area(um2)	Delay (ps)
MAC Unit	11916	542177	4900

Table shows the various types of power Dissipation in the mac unit design.

VI. CONCLUSION:

Hence a design of high performance 64 bit Multiplier-and-Accumulator (MAC) is implemented in this paper. The total MAC unit operates at a frequency of 217 MHz. The total power dissipated by 64 bit MAC unit is 177.732 mW. The total area occupied by it is 542177 11m2. Since the delay of 64 bit is less, this design can be used in the system which requires high performance in processors involving large number of bits of the operation. The MAC unit is designed using Verilog-HDL.

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