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A CSC Converter for BLDC Motor Operating In DICM for Power Factor Correction

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ABSTRACT:

This (PFC) based approved switching (CSC) advocate fed brushless DC motor (BLDCM) drive for low applications. The acceleration of BLDCM is controlled by the DC bus voltage of voltage source inverter (VSI). The BLDCM is electronically commutated for switching losses in VSI due to low abundance switching. A front-end CSC operating in alternate inductor accepted approach (DICM) is acclimated for DC bus voltage ascendancy with accord ability at AC mains. A individual sensor for DC bus voltage analysis is acclimated for the development of proposed drive which makes it a amount able solution. the proposed agreement is developed and its achievement is accurate with analysis after-effects for acceleration over a advanced ambit with accord ability at accepted AC mains. The Brushless Direct Current (BLDC) motors have been widely used in applications such as industrial automation and applications because of their advantages such as high efficiency, compact form, reliability, and low maintenance. This paper presents a sensor less operation of Brushless Direct Current (BLDC) motor. Sensor reduction for any motor drive plays a major role in selection of drive system. For reduction of sensor, the DC -DC converter operates in discontinuous inductor current mode in order to achieve unity power factor at ac mains. The BLDC motor is electronically commutated for reducing the switching losses in VSI due to low frequency switching.

KEYWORDS:
Brushless dc motor, canonical switching cell converter, discontinuous inductor current mode, power factor correction, power quality.

I.INTRODUCTION:

Among numerous motors, brushless dc motor (BLDCM) is favorite in many low and medium power applications including household appliances, industrial tools, heating ventilation and air conditioning (HVAC), medical equipment, and precise motion control systems [1]–[7]. BLDCM is preferred because of its high torque/inertia ratio, high efficiency, ruggedness, and low-electro-magnetic interference (EMI) problems [1], [2]. The stator of the BLDCM comprises of three-phase concentrated windings and rotor has permanent magnets [1], [2]. It is also recognized as an electronically commutated motor (ECM) since an electronic commutation created on rotor position via a three-phase voltage source inverter (VSI) is used [8], [9]. Thus, the problems associated with brushes, such as sparking, and wear and tear of the commutator assembly are excluded. Fig. 1 shows a conventional arrangement of BLDCM drive fed by an uncontrolled rectifier and a dc-link capacitor followed by at three-phase VSI, which is based on pulse width modulation (PWM), is used for feeding the BLDCM [10]. This type of arrangement draws peaky, harmonic rich current from the supply and leads to a high value of total harmonic distortion (THD) of supply current and very low power factor at its supply mains. A very high THD of supply current of 65.3% and a very poor power factor of 0.72 is realized.

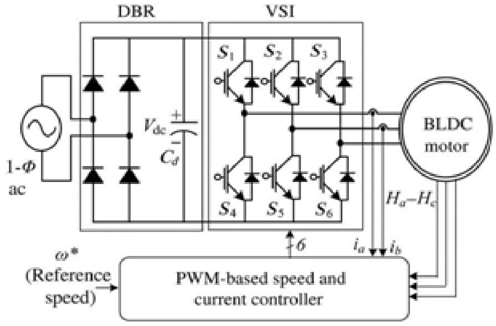

Fig 1: Conventional BLDCM drive

A front-end power factor correction (PFC) converter is used after the diode bridge rectifier (DBR) for refining the quality of power and attaining a near unity power factor at ac supply mains.

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The continuous inductor current mode (CICM) and the dis-continuous inductor current mode (DICM) are the two basic modes of operation of a PFC converter. A control of current multiplier is normally used for PFC converter operating in CICM and requires three sensors (2-V, 1-C) for the operation which is not cost-effective for low-power applications, whereas, a PFC converter operating in DICM uses a voltage follower control which requires sensing of dc-link voltage for voltage control and natural PFC is attained at ac mains [13], [14].Many topologies of a PFC-based BLDCM drives have been stated in the literature [10], [15]–[23].

A boost PFC converter has been the most popular arrangement for feeding BLDCM drive as shown in Fig. 2 [16]–[18]. A constant dc-link voltage is conserved at the dc-link capacitor and a PWM-based VSI is used for the speed control. Hence, the switching losses in VSI are very high due to high switching PWM signals and require huge quantity of sensing for its operation. Cheng [19] has proposed an active rectifier-based BLDC motor drive fed which requires complex control and is suitable for higher power applications.

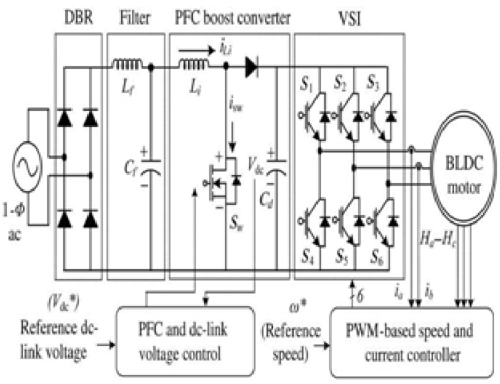

Fig 2: Conventional BLDCM drive with PFC Converter.

Lee et al. [20] have discovered numerous reduced parts formations for PFC operation which also uses a PWM-based VSI and have high switching losses in it. A buck chopper operating as a front-end converter for feeding a BLDC motor drive has been projected by Barkley et al. [21]. It also has greater switching losses associated with it due to high- frequency switching. Madani et al. have suggested a boost half bridge PFC-based BLDCM drive using four switch VSI. This also necessary PWM operation of VSI and PFC half bridge boost converter, which presents high switching losses in the whole system.

These switching losses are condensed by using an idea of variable dc-link voltage for speed control of BLDC motor [24]. This exploits the VSI to operate in low-frequency switching mandatory for electronic commutation of BLDC motor, therefore condenses the switching losses related with it. The front-end SEPIC and Cuk converter serving a BLDC motor using a variable voltage control have been offered in [10] and [23], but at the cost of two current sensors. This paper presents the development of a reduced sensor-based BLDC motor drive for low-power application.

II.PROPOSED DRIVE USING IMPROVED DC CONVERTER:

Fig. 3 shows the proposed BLDCM drive with improved dc converter which includes a front-end PFC-based canonical switching cell (CSC) converter. A CSC converter working in DICM acts as an inherent power factor pre-regulator for attaining a unity power factor at ac mains.

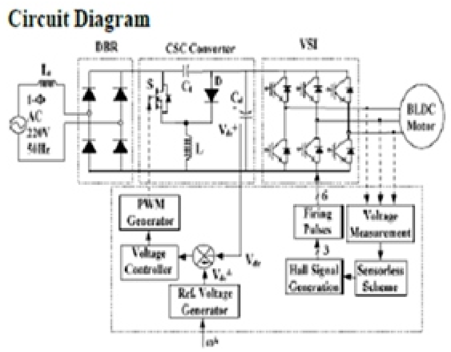

Fig 3: Proposed BLDCM drive fed from CSC Converter.

An adjustable dc-bus voltage of the VSI is used for controlling the speed of the BLDCM. This operates the VSI in low- frequency switching by electronically commutating the BLDCM for reducing the switching losses in six insulated gate bipolar transistor's (IGBT's) of VSI which share the major portion of total losses in the BLDCM drive. The front-end CSC converter is designed and its parameters are selected to operate in a DICM for obtaining a high-power factor at wide range of speed control.

III.OPERATING PRINCIPLE OF PROPOSED DC CONVERTER:

The proposed BLDCM drive uses a CSC converter working in DICM. In DICM, the current in inductor

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Li becomes discontinuous in a switching period ( ). Three states of CSC converter are shown in Fig. 4(a)–(c). Three modes of operation are described as follows.Mode I: As shown in Fig. 4(a), when switch is turned ON, the energy from the supply and stored energy in the intermediate capacitor1 are moved to inductor Li. In this process, the voltage across the intermediate capacitor reduces, while inductor current iLi and dc-link voltage are augmented. The designed value of intermediate capacitor is large enough to hold enough energy such that the voltage across it does not become discontinuous.

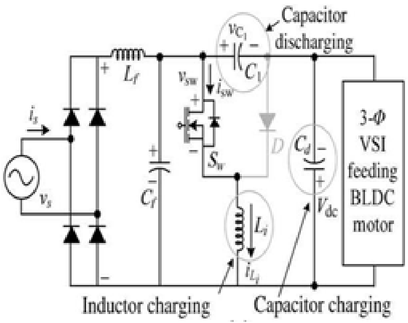

Fig.4 (a): Operation of CSC converter in Mode I

Mode II: The switch is turned OFF in this mode of operation as shown in Fig. 4(b). The intermediate capacitor 1 is charged through the supply current whereas inductor Li starts discharging hence voltage 1 starts growing, while current iLi falls in this mode of operation. Furthermore, the voltage across the dc-link capacitor continues to rise due to discharging of inductor Li.

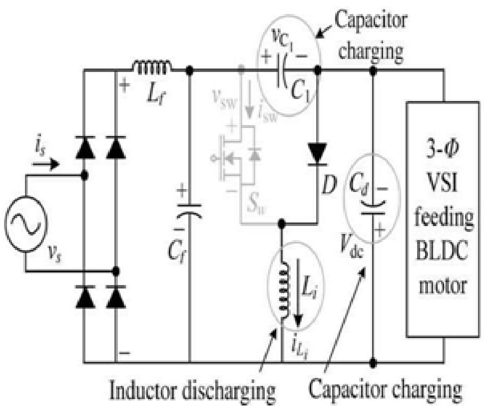

Fig.4 (b): Operation of CSC converter in Mode II

Mode III: This is the discontinuous conduction mode of operation as inductor Li is entirely discharged and current iLi becomes zero as shown in Fig. 4(c). The voltage across intermediate capacitor 1 remains to increase, while dc-link capacitor supplies the essential energy to the load, hence starts falling.

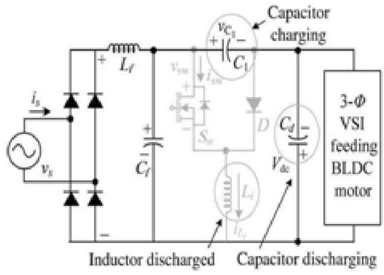

Fig.4 (c): Operation of CSC converter in Mode III

IV.DESIGN OF IMPROVED VARIABLE DC CONVERTER:

The proposed BLDCM drive uses a PFC-based CSC converter operating in DICM. The voltage appearing after the DBR is given as
Vin=2√2Vs/∏
A nominal duty ratio (dn) corresponding to Vdcn is as
Dn=Vdcn/Vdcn+vin
The design of a CSC converter is very similar to a non-isolated CUK converter with a single inductor and a switching cell which is a combination of a switch Sw diode D and an intermediate capacitor C1 . The critical value of inductance Lic to operate at boundary condition is give as
Lic=dnomvin/2IinfS
Where Iin is inductor (Li) current and fs switching frequency .now to operate this converter for power factor correction even very low duty ratio, the value of inductor Li is taken around 1/10th
OF the critical value . hence it is as,
LI<LIC/10
An intermediate capacitor C is designed for permitted ripple voltage of ΔVc1 across it and it is taken as 10% of Vc where vc is the voltage across intermediate capacitor .
C1=Vdcnomdnom/fsRLΔVC1
Where RL is the equivalent emulated load resistance which is give as Vdcn2 /p . now for a permitted ripple of 1% of the nominal dc link voltage across the dc link capacitor (cd) ,the value of dc link capacitor is calculated as.
Cd=Id/2ωlΔvdc
Where ωL is line frequency in rad/sec and Id is dc link current .hence the dc link capacitor of 220µF is selected.
To avoid the reflection of high order harmonics in supply system a low pass LC filter is designed whose maximum value CMax calculated as.

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Cmax=IPEAK/ωLVPEAK tan(θ)
Where Ipeak and Vpeak are amplitudes of supply current.

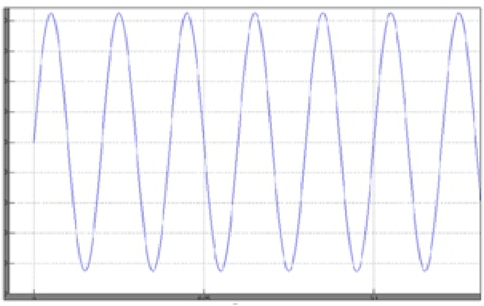
V.SIMULATION MODEL OF IMPROVED VARIABLE DC CONVERTER FED BLDCM DRIVE:

The control of the proposed drive is classified into control of DC converter and BLDCM. The improved DC converter operating in DICM is organized via a control of voltage follower. It produces PWM pulses for maintaining the required dc-link voltage at the input of VSI. A single-voltage sensor is used for the control of the improved DC converter operating in DICM. The control of BLDCM is accomplished with an electronic commutation, which includes proper switching of VSI in such a way that a symmetrical dc current is drawn from the dc-link capacitor for 120 and placed symmetrically at the centre of back electro-motive force (EMF) of each phase. A Hall-Effect position sensor is used to sense the rotor position on a span of 60 °, which is required for the electronic commutation of BLDCM.

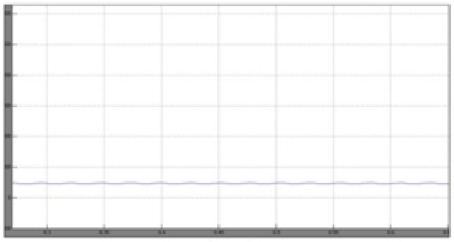
VI.SIMULATED PERFORMANCE OF PROPOSED BLDCM DRIVE:

The performance of the proposed BLDCM drive is simulated in MATLAB/Simulink results of the proposed BLDCM drive as follow.

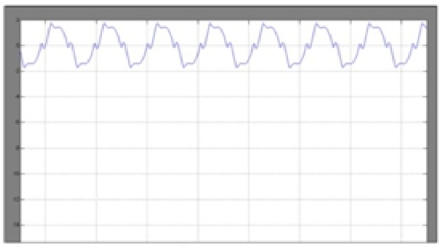
A. Performance of proposed BLDCM drive at loading on BLDCM.



(a)



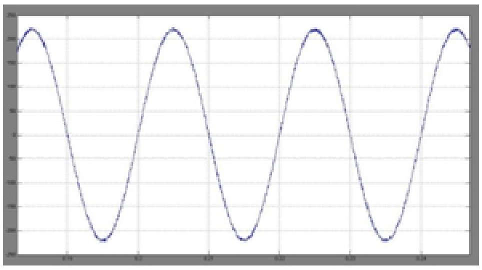
(b)



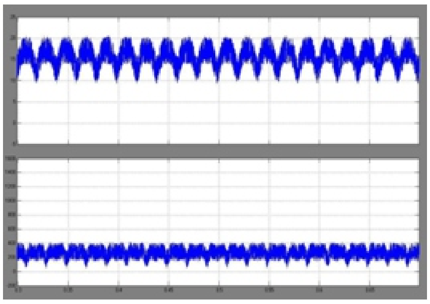
(c)

Fig 5: wave forms of proposed BLDCM drive at rated load on BLDCM with supply voltage as220v and DC bus voltage as (a) and (b), (c) 200v.

B.Simulation results performance of PFC based CSC converter.



(a)



(b)

Fig 6: Inductor current and intermediate capacitor (a) and (b).

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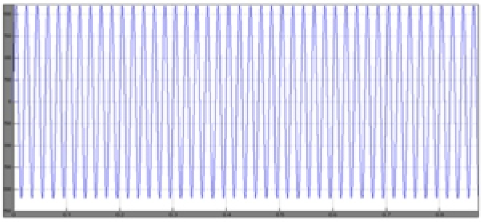
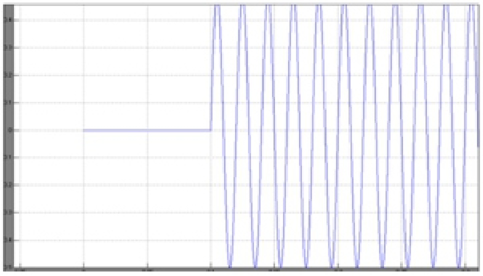
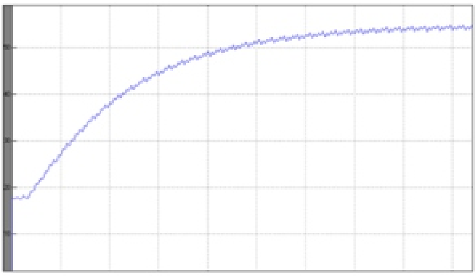
C. Dynamic performance of proposed BLDCM drive:



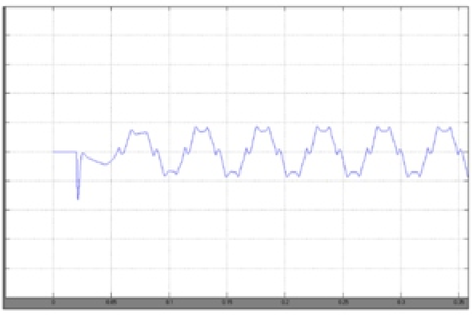
(a)



(b)



(c)



(d)

Fig 7: Dynamic performances of proposed BLDCM drive system during (a) (b) and (c) (d).

The simulation parameters are listed in table I. The performance evaluation of the proposed drive is categorized in terms of the performance of the BLDC motor and improved variable DC converter and the achieved power quality indices obtained at ac mains.

The parameters associated with the BLDC motor such as speed (N), electromagnetic torque and stator current (ai) are analyzed for the proper functioning of the BLDC motor. Parameters such as supply voltage ( ), supply current dc link voltage of improved DC converter are evaluated to demonstrate its proper functioning. Moreover, power quality indices such as power factor (PF) total harmonic distortion (THD) are analyzed for determining power quality at ac mains.

VII.CONCLUSION:

PFC Based DC Variable Voltage Converter fed BLDC drive has been proposed for targeting low-power domestic applications. An adjustable voltage of dc bus has been used for controlling the speed of BLDCM which ultimately has given the freedom to operate VSI in low-frequency switching mode for reduced switching losses. A front-end CSC converter operating in DICM has been used for dual objectives of dc-link voltage control and realizing almost unity power factor at ac mains. The performance of the proposed drive has been found quite well for its operation at variation of speed over a wide range and also variable loading conditions. A prototype of the CSC-based BLDCM drive has to be implementing with satisfactory test results for its operation over complete speed range and its operation at universal ac mains in future.

TABLE I SIMULATION PARAMETERS

Symbol	Quantity	Parameter
	Supply Voltage	200 V, 50Hz
	Nominal Voltage	120V
L	Filter Inductance	3.77mH
	Filter Capacitance	330nF
*iLi*1	Initial Current Inductance	924.75µH
	Resistance	100Ω
1	Intermediate Capacitance	494.49nF
	Capacitance (DC Link Voltage)	2211.6µF
	Stator resistance	0.2 ohms
L	Stator inductance	8.5 mH
	Number of poles	4
P	Rated power	314.16 w
	Rated dc bus voltage	220v
N	Rated speed	200 rpm
	Filter Capacitance	330nF
*iLi*1	Initial Current Inductance	924.75µH
	Resistance	100Ω
1	Intermediate Capacitance	494.49nF

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