

## Nine-level Diode Clamped Asymmetric Dual converter Based STATCOM with DC- Link Voltage Control



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### Abstract:

In this project a nine level diode clamped asymmetric dual converter is proposed based on STATCOM with DC link voltage control, supplying/absorbing reactive power to/from the grid. Reduced component count, simpler layout for switches, and smaller dc-link capacitor values are the attractive features of the proposed topology, the diode clamped and cascaded multilevel converters. This paper suggests further improvements in this topology. The proposed nine level diode clamped asymmetric dual converter mainly used to decrease the total harmonic distortion of a proposed system. Suitable selection of the dc-link voltage values reduces distortion in the current fed to the grid. In addition, circuit topology is modified to avoid the split-capacitor dc links. This reduces the number of independent dc capacitor voltages to be controlled and eliminates the flow of third-harmonic current through the transformer. In order to improve the performance, a phase-shifted carrier-based pulse width modulation technique is used. The Proposed conversion system can be analyzing and implementing by using MATLAB/SIMULINK software.

### Index Terms:

DC voltage regulation, harmonic suppression, multilevel operation, pulse width modulation (PWM), static compensator (STATCOM).

### I. Introduction:

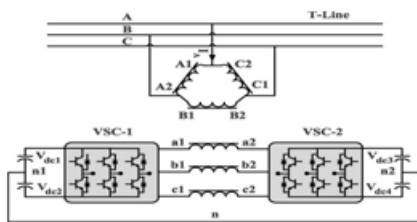
The static synchronous compensator (STATCOM) is a flexible ac transmission system device, which is connected as a shunt to the power system, for generating or absorbing reactive power. A STATCOM works in the capacitive mode if it injects reactive power to the power system.

A multi pulse converter uses more than one voltage source converter (VSC), with common dc link, operating with nearly fundamental switching frequency, and the output of each module is connected in series through the multi pulse transformer. By adjusting the triggering pulses of different VSCs, specified total harmonic distortion (THD) of the injected current is achieved with reduced switching losses as compared to that of single-VSC-based solution. The major drawback of this scheme is that high cost and complex structure of the bulky multi pulse transformer. Multilevel converter technology is a very efficient alternative for medium-voltage and high-power applications and also for other applications where high quality voltages and currents are required. Multi-level diode clamped voltage fed inverters are recently becoming very popular for multi-megawatt power applications with available switching devices. The topologies of multilevel converters and application. The main advantage of such an inverter topology is voltage division, i.e., the output voltage is produced through small steps of voltage and the individual switches are submitted only to these small voltage steps. The other commonly used multilevel topology, i.e., cascaded converter topology, comprises several single-phase H-bridge/full-bridge converters, with separate dc links. The following are the two associated problems of this topology:

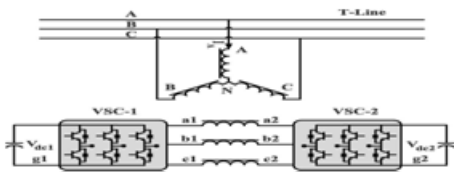
- 1) The size of the dc-link capacitor required is high because the instantaneous power involved with each module varies at twice the fundamental frequency,
- 2) Regulating voltage across a large number of self-supported dc-link capacitors makes the controller design complex

To address some of the aforementioned limitations in multilevel converters, a four-level open-ended-transformer-based multilevel converter, shown in Fig. 1, is proposed. This topology uses a reduced number of components (12 controlled switches with anti parallel diodes) as

compared to the diode clamped topology (18 controlled switches with anti parallel diodes plus 18 diodes). Moreover, in this case, semiconductor switches are arranged as VSC, which enables easier structural layout and reduced driver circuit complexity. Therefore, standard VSC power modules [include six insulated-gate bipolar transistors (IGBTs) and their driver circuits in one package] can be used instead of discrete components. Moreover, this topology utilizes cascade connection of three-phase VSCs, and hence, the size of the dc-link capacitor is less as compared to that in cascaded H-bridge multilevel converter. The reduced number of dc links makes voltage regulation easier as compared to that in an equivalent cascaded converter. Comparison of diode clamped converter, cascaded converter, and open ended transformer topologies for various parameters.



**Fig1: Open-ended-transformer-based four-level STATCOM**

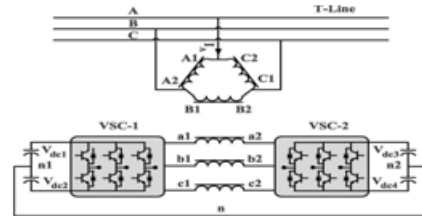


**Fig2: Conventional Asymmetric-twin-converter-topology-based STATCOM**

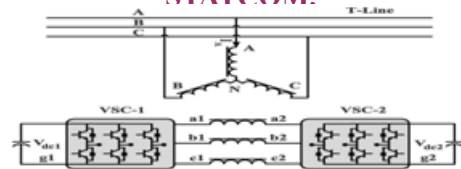
## II. Proposed multilevel circuit topology:

The proposed asymmetric-twin-converter-based multilevel topology, comprising two VSCs, is shown in Fig.3 & 4. Low voltage (LV) windings of the transformer are connected differentially between two 2-level VSCs such that the voltage appearing on the LV side is the difference of the output voltages of two VSCs. High-voltage (HV) windings, arranged in a star configuration, are connected to the three-phase grid. Leakage inductances of the transformers act as input filter inductances of the STATCOM. Both VSCs operate with separate dc links to produce two-level individual output. Voltages appearing on the LV windings of the transformer are written in terms of output voltages of VSCs as

$$\begin{aligned} e_a &= e_{a1}g_1 - e_{a2}g_2 + e_{g1}g_2 \\ e_b &= e_{b1}g_1 - e_{b2}g_2 + e_{g1}g_2 \\ e_c &= e_{c1}g_1 - e_{c2}g_2 + e_{g1}g_2 \end{aligned} \quad (1)$$



**Fig3: Block diagram of a nine level diode clamped Asymmetric-twin-converter-topology-base STATCOM.**



**Fig 4: Proposed conversion VSC-1 and VSC-2 circuit diagram**

where  $e_a$ ,  $e_{a1}g_1$ ,  $e_{a2}g_2$ , and  $e_{g1}g_2$  are the voltages across the LV winding of phase-a, the pole voltage of VSC-1, the pole voltage of VSC-2, and the voltage difference between negative dc-link terminals of the two VSCs, respectively. Since both VSCs have separate dc links, the sum of the LV winding phase currents should be zero.

$$i_a + i_b + i_c = 0. \quad (2)$$

Furthermore, the sum of instantaneous values of grid voltages is equal to zero

$$v_A + v_B + v_C = 0. \quad (3)$$

The sum of the LV winding voltages is given by

$$e_a + e_b + e_c = NLV/NHV(v_A + v_B + v_C) - r(i_a + i_b + i_c) - L \frac{d(i_a + i_b + i_c)}{dt} \quad (4)$$

Where  $r$  and  $L$  are the resistance and leakage inductance as measured from the LV side, respectively, and  $NLV/NHV$  is the turns ratio. Substituting (2) and (3) into (4) gives

$$e_a + e_b + e_c = 0. \quad (5)$$

Substituting LV voltages from (1) in (5) results in

$$\begin{aligned} e_{g1}g_2 &= -1/3(e_{a1}g_1 - e_{a2}g_2) - 1/3(e_{b1}g_1 - e_{b2}g_2) \\ &\quad - 1/3(e_{c1}g_1 - e_{c2}g_2) \end{aligned} \quad (6)$$

Substituting the value of  $e_{g1}g_2$  in (1) yields

$$\begin{pmatrix} e_a \\ e_b \\ e_c \end{pmatrix} = \frac{1}{3} \begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{pmatrix} \begin{pmatrix} e_{a1}g_1 - e_{a2}g_2 \\ e_{b1}g_1 - e_{b2}g_2 \\ e_{c1}g_1 - e_{c2}g_2 \end{pmatrix} \quad (7)$$

### III. DEVELOPMENT OF THE CONTROLLER:

The proposed nine level diode clamped asymmetric twin-converter-based STATCOM has two dc-link voltages vdc1 and vdc2. The controller should regulate these two dc-link voltages and govern the total reactive power flowing to/from the STATCOM. The total active power required to overcome losses and regulate dc-link voltages is drawn by STATCOM from the grid. This active power needs to be redistributed among the two dc links. The distribution should ensure that the two dc-link voltages vdc1 and vdc2 are maintained equal to their corresponding reference values. The suitable controller to achieve these objectives is discussed in this section.

#### A. Current Control:

The overall system is represented by two coupled differential equations, as depicted from

$$s \begin{pmatrix} i_d \\ i_q \end{pmatrix} = \begin{pmatrix} -\frac{r\omega_b}{L} & \omega \\ \omega & -\frac{r\omega_b}{L} \end{pmatrix} \begin{pmatrix} i_d \\ i_q \end{pmatrix} + \frac{\omega_b}{L} \begin{pmatrix} -e_{d1} + e_{d2} + |V| \\ -e_{q1} + e_{q2} \end{pmatrix} \quad (8)$$

The above equation is the system variables in the dq0 frame are expressed. To decouple them, two variables x1 and x2 are defined such that

$$-e_{d1} + e_{d2} = L/\omega_b(x_1 - \omega i_q) - |V| \quad (9)$$

$$-e_{q1} + e_{q2} = L/\omega_b(x_2 + \omega i_d). \quad (10)$$

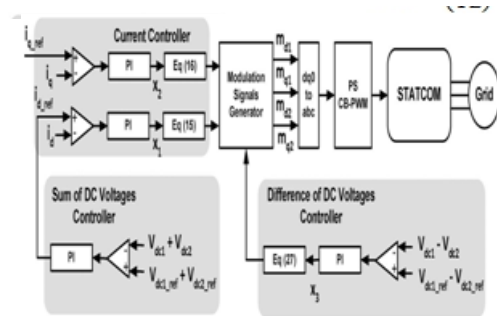
By combining (8) with (9) and (10), the decoupled system equations are obtained as follows

By combining (8) with (9) and (10), the decoupled system equations are obtained as follows

$$s \begin{pmatrix} i_d \\ i_q \end{pmatrix} = \begin{pmatrix} -\frac{r\omega_b}{L} & 0 \\ 0 & -\frac{r\omega_b}{L} \end{pmatrix} \begin{pmatrix} i_d \\ i_q \end{pmatrix} + \frac{\omega_b}{L} \begin{pmatrix} x_1 \\ x_2 \end{pmatrix} \quad (11)$$

Applying small-signal analysis on the decoupled system of (4), the small-signal plant transfer function is derived as

$$G(s) = \frac{\Delta i_d}{\Delta x_1} = \frac{\Delta i_q}{\Delta x_2} = \frac{1}{s + \frac{r\omega_b}{L}} \quad (12)$$



**Fig5: Controller for STATCOM.**

Control variables x1 and x2 govern the system currents id and iq, respectively, as per the differential equation (4). Therefore, current control is achieved by controlling variables x1 and x2 using the errors between reference values and actual currents, as given by

$$x_1 = k_{p1}(i_{d\_ref} - i_d) + k_{i1} \int (i_{d\_ref} - i_d) dt \quad (6)$$

$$x_2 = k_{p2}(i_{q\_ref} - i_q) + k_{i2} \int (i_{q\_ref} - i_q) dt \quad (7)$$

The inner current controller generates the modulating waveforms of LV voltages (md1vdc1 – md2vdc2) and (mq1vdc1 – mq2vdc2). However, modulating waveforms for individual VSCs md1, md2, mq1, and mq2 have to be derived from these LV voltages. This distribution is used to regulate real power exchange between the two VSCs. Furthermore, the current controller requires the reference current signals id\_ref and iq\_ref as inputs. The phase-locked loop is synchronized with the grid voltage such that q component of the grid voltage is kept equal to zero. Therefore, the total active and reactive powers absorbed or supplied by the STATCOM are proportional to id\_ref and iq\_ref, respectively. The outer cascaded controller generates the reference current signals id\_ref and iq\_ref such that the system variables (total reactive power and two dc-link voltages) are maintained at their respective reference values.

#### B. Reactive Power Control:

STATCOMs are commonly used either for transmission line voltage support or for reactive power compensation of load. For voltage support of the transmission line, the reactive current reference iq\_ref is controlled by the deviation of the transmission-line voltage from its nominal value. On the other hand, for load compensation operation, the reactive current reference iq\_ref is controlled by



the deviation of source power factor from its required value. In both the aforementioned cases,  $i_{q\_ref}$  will be supplied to the current controller by a higher level controller.

### C. DC Voltage Control:

A dc voltage controller should ensure that the two dc-link voltages  $v_{dc1}$  and  $v_{dc2}$  are regulated at their reference values. This problem is divided into two separate control objectives: first, to maintain the sum of two dc-link voltages ( $v_{dc1} + v_{dc2}$ ) that is equal to the sum of their reference values ( $v_{dc1-ref} + v_{dc2-ref}$ ) and, second, to maintain the difference of the two dclink voltages ( $v_{dc1} - v_{dc2}$ ) that is equal to the difference of their reference values ( $v_{dc1-ref} - v_{dc2-ref}$ ). The sum of the dc voltages ( $v_{dc1} + v_{dc2}$ ) increases with the net real power flow from grid to STATCOM and vice versa. In other words, the error in the sum of dc-link voltages ( $v_{dc1} + v_{dc2} - v_{dc1-ref} - v_{dc2-ref}$ ) indicates the amount of real power to be absorbed from the grid. Hence, the d-axis reference current  $i_{d\_ref}$  is controlled by the error existing between reference and actual dc-link voltages of VSCs, as shown in Fig. 5.

### Pulse width modulation Technique:

The pulse width modulation (PWM) concept is borrowed from communication systems, wherever an indication is modulated before its transmission, and so demodulated at the receiving terminal to recover the initial signal. Constant idea may be applied to an influence convertor. In an exceedingly power convertor, the switch network has associate on/off nonlinear nature. The desired continuous wave form is modulated and reborn to digitized signals to management the switch network. The performance of a modulation scheme can be evaluated based on the following five aspects: (1) distortion of the output voltage or current; (2) power losses; (3) harmonic spectrum and EMI; (4) dynamic range; and (5) complexity. It is always desirable to minimize the distortion of the output voltage or current. It may change with the modulation index in a nonlinear curve. The power losses are related to the total number of switching actions in one switching cycle, and the current level at switching. Therefore, different modulation schemes may result in different efficiencies. A PWM scheme with minimized switching losses is desirable especially for high power applications. Harmonic spectrum of the output voltage or current is related to the EMI issue and acoustic noise.

It is desirable to minimize the EMI and acoustic noise. Dynamic range refers to the maximum possible control level in steady state or during transient. It can also be interpreted as the ratio between the maximum possible output and the input. It is desirable to have a higher ratio. It means a better DC link voltage utilization, which is crucial for high voltage applications. It is preferable to have a PWM scheme that can be implemented easily, by either an analog means or digital means.

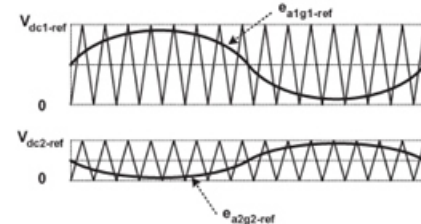


Fig.6: Comparison of modulating and carrier waveforms for PS CB-PWM

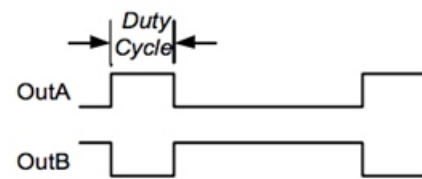


Fig 7: PWM waveforms

### IV. Simulation Results:

This section details about the analyzing and implementation of a proposed conversion system features by using MATLAB/Simulink software. The below figure shows the simulation circuit diagram of a nine level diode clamped asymmetric dual converter based STATCOM and the respective waveforms are followed.



Fig8: Simulation circuit diagram of a proposed conversion system

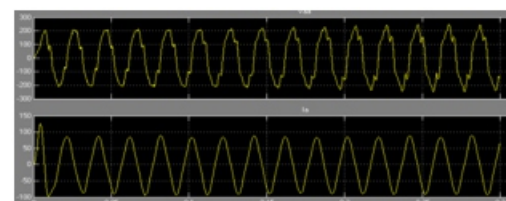
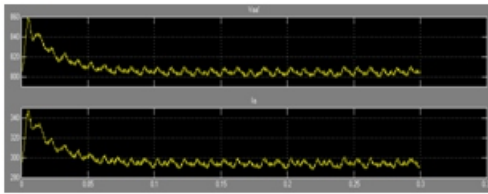
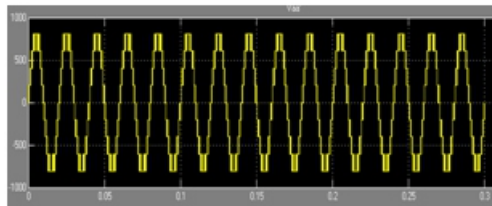


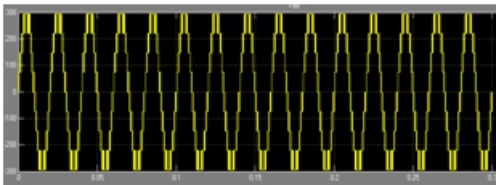
Fig9 : Waveform of source voltage and current



**Fig10: Waveforms of Voltages Vdc1 and Vdc2**



**Fig11: VSC-1 voltage waveform**



**Fig12: VSC-2 voltage waveform**

## V. CONCLUSION:

A high-power STATCOM based on two 9-level VSCs is reported. Which is used mainly to decrease the total harmonic distortion rate and also for power quality improvement. In the proposed topology, only two dc voltages have to be controlled and also in this paper, an effort has been made to improve the performance of open-ended transformer topology presented. Furthermore, the ratio of the dc-link voltages of the two VSCs is selected such that low distortion in current is achieved. A dc-link voltage controller has been proposed to regulate the dc-link voltages of the two converters by drawing requisite amount of real power from the utility and by differentially distributing them between the two converters. The proposed system is simulated by using MATLAB/SIMULINK software.

## REFERENCES:

[1] S. Anand, B. G. Fernandes, and K. Chatterjee, "A new 4-level open-ended transformer based STATCOM for high power applications," in Proc. 36th Annu. IEEE IECON, Nov. 7–10, 2010, pp. 1957–1962.

[2] C. Schauder and H. Mehta, "Vector analysis and control of advanced static VAR compensators," Proc. Inst. Elect. Eng. C—Gener., Transm. Distrib., vol. 140, no. 4, pp. 299–306, Jul. 1993.

[3] E. M. John, A. Oskoui, and A. Petersson, "Using a STATCOM to retire urban generation," in Proc. IEEE Power Syst. Conf. Expo., Oct. 2004, vol. 2, pp. 693–698.

[4] D. Soto and T. C. Green, "A comparison of high-power converter topologies for the implementation of FACTS controllers," IEEE Trans. Ind. Electron., vol. 49, no. 5, pp. 1072–1080, Oct. 2002.

[5] J. Rodriguez, J.-S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," IEEE Trans. Ind. Electron., vol. 49, no. 4, pp. 724–738, Aug. 2002.

[6] Y. Cheng, C. Qian, M. L. Crow, S. Pekarek, and S. Atcitty, "A comparison of diode-clamped and cascaded multilevel converters for a STATCOM with energy storage," IEEE Trans. Ind. Electron., vol. 53, no. 5, pp. 1512–1521, Oct. 2006.

[7] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, "Medium-voltage multilevel converters—State of the art, challenges, and requirements in industrial applications," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2581–2596, Aug. 2010.

[8] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. G. Franquelo, B. Wu, J. Rodriguez, M. A. Pérez, and J. I. Leon, "Recent advances and industrial applications of multilevel converters," IEEE Trans. Ind. Electron., vol. 57, no. 8, pp. 2553–2580, Aug. 2010.

[9] F. Z. Peng, J. W. McKeever, and D. J. Adams, "A power line conditioner using cascade multilevel inverters for distribution systems," IEEE Trans. Ind. Appl., vol. 34, no. 6, pp. 1293–1298, Nov./Dec. 1998.

[10] K. V. Patil, R. M. Mathur, J. Jiang, and S. H. Hosseini, "Distribution system compensation using a new binary multilevel voltage source inverter," IEEE Trans. Power Del., vol. 14, no. 2, pp. 459–464, Apr. 1999.

[11] C. K. Lee, S. Y. Ron Hui, and H. S. Chung, "A 31-level cascade inverter for power applications," IEEE Trans. Ind. Electron., vol. 49, no. 3, pp. 613–617, Jun. 2002.

[12] H. Akagi, S. Inoue, and T. Yoshii, "Control and performance of a transformerless cascade PWM STATCOM with star configuration," *IEEE Trans. Ind. Appl.*, vol. 43, no. 4, pp. 1041–1049, Jul./Aug. 2007.

[13] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.

[14] Y. Fukuta and G. Venkataramanan, "DC bus ripple minimization in cascaded H-bridge multilevel converters under staircase modulation," in *Proc. 37th IEEE IAS Annu. Meeting*, 2002, vol. 3, pp. 1988–1993.

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